TPS56528 4.5-V to 18-V Input, 5-A Synchronous Step-Down Converter With Advanced Eco-Mode™

1 Features
- D-CAP2™ Mode Enables Fast Transient Response
- Low Output Ripple and Allows Ceramic Output Capacitor
- Wide VIN Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.6 V to 7 V
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications –68 mΩ (High-Side) and 37 mΩ (Low-Side)
- High Efficiency, Less Than 10 µA at Shutdown
- High Initial Band-Gap Reference Accuracy
- Prebiased Soft Start
- 650-kHz Switching Frequency (fSW)
- Cycle-By-Cycle Overcurrent Limit
- Advanced Auto-Skip Eco-Mode™ for High Efficiency at Light Load
- Power Good Output
- Fixed Soft Start: 1 ms

2 Applications
- Wide Range of Applications for Low Voltage Systems
  - Digital TV Power Supply
  - High Definition Blu-ray Disc™ Players
  - Networking Home Terminals
  - Digital Set-Top Boxes (STB)

3 Description
The TPS56528 device is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS56528 enables system designers to complete the suite of various end-equipment power bus regulators with a cost-effective, low component count, low standby current solution. The main control loop for the TPS56528 uses the D-CAP2™ mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and advanced Eco-Mode™ operation at light loads. Advanced Eco-Mode™ allows the TPS56528 to maintain high efficiency during lighter load conditions. The TPS56528 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.6 V and 7 V. The device also features a fixed 1-ms soft-start time and power good output. The TPS56528 is available in the 8-pin SO PowerPAD™ package, and designed to operate from –40°C to 85°C.

Device Information(1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS56528</td>
<td>SO PowerPAD (8)</td>
<td>4.89 mm × 3.90 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

Transient Response

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2013) to Revision B

Page

- Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ........................................... 1

Changes from Original (April 2013) to Revision A

Page

- Changed the device From: Product Preview To: Production ................................................................................................. 1
## 5 Pin Configuration and Functions

### DDA Package

8-Pin SO PowerPAD
Top View

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EN</td>
<td>Enable input control. EN is active high and must be pulled up to enable the device.</td>
</tr>
<tr>
<td>2</td>
<td>VFB</td>
<td>Converter feedback input. Connect to output voltage with feedback resistor divider.</td>
</tr>
<tr>
<td>3</td>
<td>VREG5</td>
<td>5.5-V power supply output. A capacitor (0.47 µF typical) must be connected to GND. VREG5 is not active when EN is low.</td>
</tr>
<tr>
<td>4</td>
<td>PG</td>
<td>Open-drain power good output.</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.</td>
</tr>
<tr>
<td>6</td>
<td>SW</td>
<td>Switch node connection between high-side NFET and low-side NFET.</td>
</tr>
<tr>
<td>7</td>
<td>VBST</td>
<td>Supply input for the high-side FET gate drive circuit. Connect 0.1-µF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.</td>
</tr>
<tr>
<td>8</td>
<td>VIN</td>
<td>Input voltage supply pin.</td>
</tr>
<tr>
<td></td>
<td>PowerPAD</td>
<td>Thermal pad of the package. This pad must be soldered to achieve appropriate dissipation and must be connected to GND.</td>
</tr>
</tbody>
</table>

---

Not to scale
PowerPAD

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Submit Documentation Feedback
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted) \(^{(1)}\)

<table>
<thead>
<tr>
<th>Input voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN and EN</td>
<td>−0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>VBST</td>
<td>−0.3</td>
<td>26</td>
<td>V</td>
</tr>
<tr>
<td>VBST (10-ns-transient)</td>
<td>−0.3</td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>VBST (v.out SW)</td>
<td>−0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>VFB and PG</td>
<td>−0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>SW</td>
<td>−2</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>SW (10-ns-transient)</td>
<td>−3</td>
<td>22</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VREG5</td>
<td>−0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>GND</td>
<td>−0.3</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>Voltage from GND to thermal pad, (V_{\text{diff}})</td>
<td>−0.2</td>
<td>0.2</td>
<td>V</td>
</tr>
<tr>
<td>Operating junction temperature, (T_J)</td>
<td>−40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, (T_{\text{stg}})</td>
<td>−55</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Electrostatic discharge</th>
<th>(V_{\text{ESD}})</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrostatic discharge</td>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Electrostatic discharge</td>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101 (^{(2)})</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Input voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{IN}})</td>
<td>4.5</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{I}})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{O}})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{\text{O}})</td>
<td>0</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>(T_A)</td>
<td>−40</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>(T_J)</td>
<td>−40</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>
6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS56528 DDA (SO PowerPAD)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{JA} ) Junction-to-ambient thermal resistance</td>
<td>44.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JCTop} ) Junction-to-case (top) thermal resistance</td>
<td>51.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JUB} ) Junction-to-board thermal resistance</td>
<td>27.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>( \psi_{JT} ) Junction-to-top characterization parameter</td>
<td>8.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>( \psi_{JB} ) Junction-to-board characterization parameter</td>
<td>27.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JCbot} ) Junction-to-case (bottom) thermal resistance</td>
<td>5.3</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range, \( V_{IN} = 12 \) V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SUPPLY CURRENT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I(VIN) ) Operating non-switching supply current</td>
<td>( V_{IN} ) current, ( T_A = 25^\circ C ), ( EN = 5 ) V, ( V_{(FB)} = 0.7 ) V</td>
<td>170</td>
<td>350</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I(VINSDN) ) Shutdown supply current</td>
<td>( V_{IN} ) current, ( T_A = 25^\circ C ), ( EN = 0 ) V</td>
<td>3.8</td>
<td>10</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>LOGIC THRESHOLD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V(EN) ) EN high-level input voltage</td>
<td>EN</td>
<td>1.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V(EN) ) EN low-level input voltage</td>
<td>EN</td>
<td>0.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( R(EN) ) EN pin resistance to GND</td>
<td>( V_{EN} = 12 ) V</td>
<td>180</td>
<td>350</td>
<td>700</td>
<td>kΩ</td>
</tr>
<tr>
<td>( V_{FB} ) VOLTAGE AND DISCHARGE RESISTANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{(FBTH)} ) ( V_{(FB)} ) threshold voltage</td>
<td>( T_A = 25^\circ C ), ( V_O = 1.05 ) V, ( I_O = 10 ) mA, advanced Eco-Mode operation</td>
<td>606</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>( V_{(FBTH)} ) ( V_{(FB)} ) threshold voltage</td>
<td>( T_A = 25^\circ C ), ( V_O = 1.05 ) V, continuous mode operation</td>
<td>593</td>
<td>600</td>
<td>607</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{(FBTH)} ) ( V_{(FB)} ) threshold voltage</td>
<td>( T_A = -40 ) to 85°C, ( V_O = 1.05 ) V, continuous mode operation(1)</td>
<td>588</td>
<td>600</td>
<td>612</td>
<td>mV</td>
</tr>
<tr>
<td>( I(VFB) ) ( V_{(FB)} ) input current</td>
<td>( V_{(FB)} = 0.7 ) V, ( T_A = 25^\circ C )</td>
<td>0</td>
<td>±0.15</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>SW DISCHARGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I(DISCHG) ) SW discharge current</td>
<td>EN = 0 V, SW = 1 V, ( T_A = 25^\circ C )</td>
<td>1</td>
<td>1.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( V(REGS) ) OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| \( V(VREGS) \) \( V_{REGS} \) output voltage | \( T_A = 25^\circ C \), 6.0 V < \( V_{IN} < 18 \) V, 
\( 0 < I(VREGS) < 5 \) mA | 5.2 | 5.5 | 5.7 | V    |
| \( I(VREGS) \) Output current | \( V_{IN} = 6 \) V, \( V_{(REGS)} = 4 \) V, \( T_A = 25^\circ C \) | 20  |     |     | mA   |
| MOSFET                        |                                           |     |     |     |      |
| \( R(DS(on)) \) High-side switch resistance | 25°C, \( V_{(BST)} \) = SW = 5.5 V | 68  |     |     | mΩ   |
| \( R(DS(on)) \) Low-side switch resistance | 25°C                                     | 37  |     |     | mΩ   |
| CURRENT LIMIT                 |                                           |     |     |     |      |
| \( I(ooc) \) Current limit    | \( L_{OUT} = 1.5 \) \( \mu H \) (1)       | 5.5 | 6.2 | 7.8 | A    |
| THERMAL SHUTDOWN              |                                           |     |     |     |      |
| \( T(SDN) \) Thermal shutdown threshold | Shutdown temperature (1) | 165 |     |     | °C   |
| \( Hysteresis \) (1)          |                                           | 35  |     |     |      |
| POWER GOOD                    |                                           |     |     |     |      |
| \( V(THPG) \) PG threshold    | VFB rising (good)                         | 95% | 90% | 95% |      |
| \( V(THPG) \) PG threshold    | VFB falling (Fault)                      | 85% |     |     |      |
| IPG                           | PG sink current                          | 2   | 4   |     | mA   |

(1) Not production tested.
Electrical Characteristics (continued)

over operating free-air temperature range, $V_{IN}=12\, \text{V}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OVP}$</td>
<td>Output OVP threshold</td>
<td>OVP Detect (L&gt;H)</td>
<td>125%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{UVP}$</td>
<td>Output UVP threshold</td>
<td>UVP detect (H&gt;L)</td>
<td>65%</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>UVLO</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UVLO</td>
<td>UVLO threshold</td>
<td>Wake-up $V_{REGS}$ voltage</td>
<td>3.45</td>
<td>3.75</td>
<td>4.05</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hysteresis $V_{REGS}$ voltage</td>
<td>0.13</td>
<td>0.32</td>
<td>0.48</td>
</tr>
</tbody>
</table>

### 6.6 Timing Requirements

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ON-TIME TIMER CONTROL</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{ON}$</td>
<td>On-time</td>
<td>$V_{IN}=12, \text{V}, , V_O=1.05, \text{V}$</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OFF(MIN)}$</td>
<td>Minimum off-time</td>
<td>$T_A=25, \degree\text{C}, , V_{FB}=0.5, \text{V}$</td>
<td>260</td>
<td>310 ns</td>
</tr>
<tr>
<td><strong>SOFT START</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SS}$</td>
<td>Soft-start time</td>
<td>Internal soft-start time</td>
<td>0.7</td>
<td>1</td>
</tr>
<tr>
<td><strong>OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{UVPDEL}$</td>
<td>Output UVP delay</td>
<td>to hiccup state</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>$t_{UVPEN}$</td>
<td>Output UVP enable delay</td>
<td>Relative to soft-start time</td>
<td>×1.7</td>
<td></td>
</tr>
</tbody>
</table>
6.7 Typical Characteristics

$V_{\text{IN}} = 12\, \text{V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

Figure 1. VIN Supply Current vs Junction Temperature

Figure 2. VIN Shutdown Current vs Junction Temperature

Figure 3. EN Current vs EN Voltage

Figure 4. 1.05-V Output Voltage vs Output Current

Figure 5. 1.05-V Output Voltage vs Input Voltage

Figure 6. Switching Frequency vs Input Voltage
Typical Characteristics (continued)

\( V_{IN} = 12 \, \text{V} \) and \( T_A = 25^\circ \text{C} \) (unless otherwise noted)

![Graph](image-url)
7 Detailed Description

7.1 Overview
The TPS5652 is a 5-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low-ESR output capacitors including ceramic and special polymer types. And also PG output can be used for sequence operation.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 PWM Operation

The main control loop of the TPS56528 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the requirement for ESR-induced output ripple from D-CAP2™ mode control.

7.3.2 PWM Frequency and Adaptive On-Time Control

TPS56528 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS56528 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage; therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

7.3.3 Soft Start and Prebiased Soft Start

The TPS56528 has an internal 1-ms soft start. When the EN pin becomes high, internal soft-start function begins ramping up the reference voltage to the PWM comparator.

The TPS56528 contains a unique circuit to prevent current from being pulled from the output during start-up if the output is prebiased. When the soft start commands a voltage higher than the prebias level (internal soft start becomes greater than feedback voltage VFB), the controller slowly activates synchronous rectification by starting the first low-side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the prebias output, and ensure that the out voltage (VOUT) starts and ramps up smoothly into regulation and the control loop is given time to transition from prebiased start-up to normal mode operation.

7.3.4 Power Good

The power good function is activated after soft start has finished. The power good function becomes active after 1.7 × soft-start time. When the output voltage becomes within −10% of the target value, internal comparators detect power good state and the power good signal becomes high. The power good output, PG is an open-drain output. If the feedback voltage goes under 15% of the target value, the power good signal becomes low.

7.3.5 Output Discharge Control

TPS56528 discharges the output through the SW pin when EN is low, or the controller is turned off by the protection functions (UVP, UVLO and thermal shutdown). The internal regular low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

7.3.6 Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by \( I_{OCP} \), \( V_{OUT} \), the on-time and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current, Iout. The TPS56528 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching
Feature Description (continued)

cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of overcurrent protection. The peak current is the average load current plus one half of the peak-to-peak inductor current. The valley current is the average load current minus one half of the peak-to-peak inductor current. Because the valley current is used to detect the overcurrent threshold, the load current is higher than the overcurrent threshold. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This protection is non-latching. When the VFB voltage becomes lower than 65% of the target voltage, the UVP comparator detects it. After 7 µs detecting the UVP voltage, device shut downs and restarts after hiccup time.

When the overcurrent condition is removed, the output voltage returns to the regulated value.

7.3.7 UVLO Protection

Undervoltage lockout protection (UVLO) monitors the voltage of the V_REGS pin. When the V_REGS voltage is lower than UVLO threshold voltage, the TPS56528 is shut off. This protection is non-latching.

7.3.8 Thermal Shutdown

TPS56528 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.

7.4 Device Functional Modes

7.4.1 Advanced Auto-Skip Eco-Mode™ Control

The TPS56528 is designed with advanced auto-skip Eco-Mode™ to increase higher light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced. If the output current is reduced enough, the inductor current ripple valley reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying low-side MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept approximately the same as is in continuous conduction mode. The off-time increases as it takes more time to discharge the output capacitor to the level of the reference voltage with smaller load current. The transition point to the light load operation I_OUT(LL) current can be calculated in Equation 1.

\[
I_{\text{OUT(LL)}} = \frac{1}{2 \cdot L \cdot f_{SW}} \left( V_{\text{IN}} - V_{\text{OUT}} \right) \frac{V_{\text{OUT}}}{V_{\text{IN}}}
\]

(1)
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TPS56528 is a 4.5-V to 18-V input step-down DC-DC converter with an output voltage adjustable from 0.6 V to 7 V and capable of output currents up to 5 A.

8.2 Typical Application

![Typical Application Schematic](image-url)

8.2.1 Design Requirements
Table 1 lists the design parameters for this application example.

Table 1. Design Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range, $V_{IN}$</td>
<td>4.5 to 18 V</td>
</tr>
<tr>
<td>Output voltage, $V_{OUT}$</td>
<td>1.05 V</td>
</tr>
<tr>
<td>Output current, $I_{OUT}$</td>
<td>5 A</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>650 KHz</td>
</tr>
<tr>
<td>Output voltage ripple, $V_{OUT}$</td>
<td>$&lt;$ 20 mV</td>
</tr>
<tr>
<td>Input voltage ripple, $V_{IN}$</td>
<td>$&lt;$ 100 mV</td>
</tr>
</tbody>
</table>
8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends using 1% tolerance or better divider resistors. Start by using Equation 2 to calculate \( V_{\text{OUT}} \).

\[
V_{\text{OUT}} = 0.60 \times \left( 1 + \frac{R_1}{R_2} \right)
\]

(2)

To improve efficiency at light loads, consider using larger value resistors, high resistance is more susceptible to noise, and the voltage errors from the VFB input current are more noticeable.

8.2.2.2 Output Filter Selection

The output filter used with the TPS56528 is an LC circuit. This LC filter has double pole in Equation 3.

\[
F_P = \frac{1}{2\pi \sqrt{L_{\text{OUT}} \times C_{\text{OUT}}}}
\]

(3)

At low frequencies, the overall loop gain is set by the output setpoint resistor divider network and the internal gain of the TPS56528. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement, use the values recommended in Table 2.

<table>
<thead>
<tr>
<th>OUTPUT VOLTAGE (V)</th>
<th>R1 (kΩ)</th>
<th>R2 (kΩ)</th>
<th>C4 (pF)(^{(1)})</th>
<th>L1 (µH)</th>
<th>C7 + C8 (µF)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>1</td>
<td>33.2</td>
<td>49.9</td>
<td>5</td>
<td>33</td>
<td>1</td>
</tr>
<tr>
<td>1.05</td>
<td>37.4</td>
<td>49.9</td>
<td>5</td>
<td>33</td>
<td>1</td>
</tr>
<tr>
<td>1.2</td>
<td>49.9</td>
<td>49.9</td>
<td>5</td>
<td>22</td>
<td>1</td>
</tr>
<tr>
<td>1.5</td>
<td>75.0</td>
<td>49.9</td>
<td>5</td>
<td>15</td>
<td>1</td>
</tr>
<tr>
<td>1.8</td>
<td>100</td>
<td>49.9</td>
<td>5</td>
<td>10</td>
<td>1</td>
</tr>
<tr>
<td>2.5</td>
<td>158</td>
<td>49.9</td>
<td>5</td>
<td>10</td>
<td>1.5</td>
</tr>
<tr>
<td>3.3</td>
<td>226</td>
<td>49.9</td>
<td>2</td>
<td>5</td>
<td>1.5</td>
</tr>
<tr>
<td>5</td>
<td>365</td>
<td>49.9</td>
<td>2</td>
<td>5</td>
<td>2.2</td>
</tr>
<tr>
<td>6.5</td>
<td>487</td>
<td>49.9</td>
<td>2</td>
<td>2</td>
<td>2.2</td>
</tr>
</tbody>
</table>

(1) Optional

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed-forward capacitor (C4) in parallel with R1.

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using Equation 4, Equation 5, and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for \( f_{\text{SW}} \).

Ensure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

\[
I_{P-P} = \frac{V_{\text{OUT}}}{V_{\text{IN(MAX)}} - V_{\text{OUT}}} \times \frac{V_{\text{IN(MAX)}}}{L_{\text{O}} \times f_{\text{SW}}}
\]

\[
I_{\text{PEAK}} = I_{\text{O}} + \frac{I_{P-P}}{2}
\]

(4) (5)
For this design example, the calculated peak current is 5.51 A and the calculated RMS current is 5.01 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS56528 is intended for use with ceramic or other low-ESR capacitors. Recommended values range from 20 µF to 68 µF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

\[ I_{\text{Co(RMS)}} = \sqrt{\frac{V_{\text{OUT}}^2 \cdot (V_{\text{IN}} \cdot V_{\text{OUT}})}{12 \cdot V_{\text{IN}} \cdot L_{\text{O}} \cdot f_{\text{SW}}}} \]  

(7)

For this design, two TDK C3216X5R0J226M 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.284 A and each output capacitor is rated for 4 A.

8.2.2.3 Input Capacitor Selection

The TPS56528 requires an input decoupling capacitor and a bulk capacitor is required depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from pin 8 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating requires greater than the maximum input voltage.

8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends using a ceramic capacitor.

8.2.2.5 VREG5 Capacitor Selection

A 0.47-µF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. TI recommends using a ceramic capacitor.

8.2.3 Application Curves

Figure 11. 1.05-V, Load Transient Response

Figure 12. Start-Up Waveform
9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 4.5 V and 18 V. This input supply must be well regulated. If the input supply is placed more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.
10 Layout

10.1 Layout Guidelines

1. The TPS56528 can supply large load currents up to 5 A, so heat dissipation may be a concern. The top-side area adjacent to the TPS56528 must be filled with ground as much as possible to dissipate heat.

2. The bottom side area directly below the IC must be a dedicated ground area. It must be directly connected to the thermal pad of the device using vias as shown. The ground area must be as large as practical. Additional internal layers can be dedicated as ground planes and connected to vias as well.

3. Keep the input switching current loop as small as possible.

4. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections must be brought from the output to the feedback pin of the device.

5. Keep analog and non-switching components away from switching components.

6. Make a single point connection from the signal ground to power ground.

7. Do not allow switching current to flow under the device.

8. Keep the pattern lines for VIN and PGND broad.

9. Exposed pad of device must be connected to PGND with solder.

10. VREG5 capacitor must be placed near the device, and connected to PGND.

11. Output capacitor must be connected to a broad pattern of the PGND.

12. Voltage feedback loop must be as short as possible, and preferably with ground shield.

13. Lower resistor of the voltage divider which is connected to the VFB pin must be tied to SGND.

14. Providing sufficient via is preferable for VIN, SW, and PGND connection.

15. PCB pattern for VIN, SW, and PGND must be as broad as possible.

16. VIN capacitor must be placed as near as possible to the device.

10.2 Layout Example

![PCB Layout](Figure 17. PCB Layout)
10.3 Thermal Information

This 8-pin SO PowerPAD package incorporates an exposed thermal pad that is designed to be directly to an external heat sink. The thermal pad must be soldered directly to the printed-circuit board (PCB). After soldering, the PCB can be used as a heat sink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, see PowerPAD™ Thermally Enhanced Package (SLMA002) and PowerPAD™ Made Easy (SLMA004).

The exposed thermal pad dimensions for this package are shown in Figure 18.

![Figure 18. Thermal Pad Dimensions (Top View)](image-url)
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer
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CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES
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ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation
For related documentation see the following:
• PowerPAD™ Thermally Enhanced Package (SLMA002)
• PowerPAD™ Made Easy (SLMA004)

11.3 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper
right corner, click on Alert me to register and receive a weekly digest of any product information that has
changed. For change details, review the revision history included in any revised document.

11.4 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective
contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of
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TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration
among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help
solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and
contact information for technical support.

11.5 Trademarks
D-CAP2, Eco-Mode, PowerPAD, E2E are trademarks of Texas Instruments.
Blu-ray Disc is a trademark of Blu-ray Disc Association.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam
during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most
current data available for the designated devices. This data is subject to change without notice and revision of
this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS56528DDA</td>
<td>ACTIVE</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>56528</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS56528DDAR</td>
<td>ACTIVE</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>56528</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD:** The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS56528DDAR</td>
<td>SO Power PAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.8</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>Device</td>
<td>Package Type</td>
<td>Package Drawing</td>
<td>Pins</td>
<td>SPQ</td>
<td>Length (mm)</td>
<td>Width (mm)</td>
<td>Height (mm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-------------</td>
<td>----------------</td>
<td>----------------</td>
<td>------</td>
<td>-----</td>
<td>-------------</td>
<td>------------</td>
<td>-------------</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS56528DDAR</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>366.0</td>
<td>364.0</td>
<td>50.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.
THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

---

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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