Features

- Ultra-small X2SON package (0.8 mm × 0.8 mm × 0.4 mm)
- Tiny 5-pin SOT23 and SC70 packages
- Wide supply voltage range of 1.6 V to 5.5 V
- Quiescent supply current of 5 µA
- Low propagation delay of 260 ns
- Rail-to-rail common-mode input voltage
- Internal hysteresis (4 mV)
- Push-pull and open-drain output options
- No phase reversal for overdriven inputs
- –40°C to 125°C Operating ambient temperature

Applications

- Mobile phones and tablets
- Portable and battery-powered devices
- IR receivers
- Level translators
- Threshold detectors and discriminators
- Window comparators
- Zero-crossing detectors

Description

The TLV7011 and TLV7021 are single-channel, micro-power comparators that feature low-voltage operation with rail-to-rail input capability. These comparators are available in an ultra-small, leadless package measuring 0.8 mm × 0.8 mm, making them applicable for space-critical designs like smartphones and other portable or battery-powered applications.

The TLV7011 and TLV7021 offer an excellent speed-to-power combination with a propagation delay of 260 ns and a quiescent supply current of 5 µA. This combination of fast response time at micropower enables power conscious systems to monitor and respond quickly to fault conditions. With an operating voltage range of 1.6 V to 5.5 V, these comparators are compatible with 3-V and 5-V systems.

These comparators also feature no output phase inversion with overdriven inputs and internal hysteresis. These features make this family of comparators well suited for precision voltage monitoring in harsh, noisy environments where slow-moving input signals must be converted into clean digital outputs.

The TLV7011 has a push-pull output stage capable of sinking and sourcing milliamps of current when controlling an LED or driving a capacitive load. The TLV7021 has an open-drain output stage that can be pulled beyond VCC, making it appropriate for level translators and bipolar to single-ended converters.

<table>
<thead>
<tr>
<th>PART NUMBERS</th>
<th>PACKAGE (PINS)</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV7011, TLV7021</td>
<td>X2SON (5)</td>
<td>0.80 mm × 0.80 mm</td>
</tr>
<tr>
<td></td>
<td>SC70 (5)</td>
<td>2.00 mm × 1.25 mm</td>
</tr>
<tr>
<td></td>
<td>SOT-23 (5)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TLV70x1 Family of Low Power Comparators

<table>
<thead>
<tr>
<th>PART NUMBERS</th>
<th>OUTPUT</th>
<th>SUPPLY CURRENT (TYP)</th>
<th>PROPAGATION DELAY (TYP)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV7011</td>
<td>Push-pull</td>
<td>5 µA</td>
<td>260 ns</td>
</tr>
<tr>
<td>TLV7021</td>
<td>Open-drain</td>
<td>5 µA</td>
<td>260 ns</td>
</tr>
<tr>
<td>TLV7031</td>
<td>Push-pull</td>
<td>335 nA</td>
<td>3 µs</td>
</tr>
<tr>
<td>TLV7041</td>
<td>Open-drain</td>
<td>335 nA</td>
<td>3 µs</td>
</tr>
</tbody>
</table>

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.
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## 4 Revision History

### Changes from Revision C (March 2018) to Revision D Page
- Added leaded package option to features .......................................................... 1
- Deleted preview status of SOT23 package .......................................................... 1
- Deleted preview status of SOT23 package .......................................................... 3

### Changes from Revision B (November 2017) to Revision C Page
- Changed the preview SC70 package to production data .................................... 1

### Changes from Revision A (July 2017) to Revision B Page
- Changed propagation delay from: 200 ns to: 260 ns ........................................... 1
- Added preview SC70 and SOT-23 packages to the data sheet ......................... 1
- Added TLV70x1 Family of Micropower Comparators table per marketing request ................................................... 1
- Changed the key graphic title from: Propagation Delay vs. Overdrive (TLV7011) to: Propagation Delay vs. Overdrive .... 1
- Removed (TLV7011 only) text from several Typical Characteristics graphs ................. 7
- Removed some Typical Characteristics graphs ................................................. 7
- Added Figure 14 ..................................................................................................... 7
- Added Figure 21 ..................................................................................................... 9
- Added content to the Inputs section .................................................................... 13
- Added the IR Receiver Analog Front End section .............................................. 18

### Changes from Original (May 2017) to Revision A Page
- Changed device status from ADVANCED INFO to PRODUCTION DATA .................. 1
5 Pin Configuration and Functions

DPW Package
5-Pin X2SON
Top View

DBV and DCK Package
5-Pin SOT-23 and SC70
Top View

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O/P(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>O</td>
<td>Output</td>
</tr>
<tr>
<td>VCC</td>
<td>P</td>
<td>Positive (highest) power supply</td>
</tr>
<tr>
<td>VEE</td>
<td>P</td>
<td>Negative (lowest) power supply</td>
</tr>
<tr>
<td>IN–</td>
<td>I</td>
<td>Inverting input</td>
</tr>
<tr>
<td>IN+</td>
<td>I</td>
<td>Noninverting input</td>
</tr>
</tbody>
</table>

(1)  I = Input, O = Output, P = Power
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V_S = V_{CC} - V_{EE})</td>
<td></td>
<td>6 V</td>
<td></td>
</tr>
<tr>
<td>Input pins ((N+, N-))(^{(2)})</td>
<td>(V_{EE} - 0.3)</td>
<td>6 V</td>
<td></td>
</tr>
<tr>
<td>Current into Input pins ((N+, N-))(^{(2)})</td>
<td>±10 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output (OUT) (TLV7011)(^{(3)})</td>
<td>(V_{EE} - 0.3)</td>
<td>(V_{CC} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>Output (OUT) (TLV7021)</td>
<td>(V_{EE} - 0.3)</td>
<td>6 V</td>
<td></td>
</tr>
<tr>
<td>Output short-circuit duration(^{(4)})</td>
<td>10 s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction temperature, (T_J)</td>
<td>−65 °C</td>
<td>150 °C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>−65 °C</td>
<td>150 °C</td>
<td></td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to \(V_{EE}\). Input signals that can swing 0.3V below \(V_{EE}\) must be current-limited to 10mA or less.

(3) Output maximum is \((V_{CC} + 0.3V)\) or 6V, whichever is less.

(4) Short-circuit to ground, one comparator per package.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM)</td>
<td>±2000 V</td>
<td></td>
</tr>
<tr>
<td>Charged-device model (CDM)</td>
<td>±1000 V</td>
<td></td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V_S = V_{CC} - V_{EE})</td>
<td>1.6</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Ambient temperature, (T_A)</td>
<td>−40 °C</td>
<td>125 °C</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>THERMAL METRIC(^{(1)})</th>
<th>THERMAL METRIC(^{(1)})</th>
<th>THERMAL METRIC(^{(1)})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
</tr>
<tr>
<td>(497.5)</td>
<td>(306.3)</td>
<td>(278.8)</td>
<td>(°C/W)</td>
</tr>
<tr>
<td>(R_{JC(top)}) Junction-to-case (top) thermal resistance</td>
<td>(R_{JC(top)}) Junction-to-case (top) thermal resistance</td>
<td>(R_{JC(top)}) Junction-to-case (top) thermal resistance</td>
<td>(R_{JC(top)}) Junction-to-case (top) thermal resistance</td>
</tr>
<tr>
<td>(275.5)</td>
<td>(228.4)</td>
<td>(188.6)</td>
<td>(°C/W)</td>
</tr>
<tr>
<td>(R_{JB}) Junction-to-board thermal resistance</td>
<td>(R_{JB}) Junction-to-board thermal resistance</td>
<td>(R_{JB}) Junction-to-board thermal resistance</td>
<td>(R_{JB}) Junction-to-board thermal resistance</td>
</tr>
<tr>
<td>(372.2)</td>
<td>(166.5)</td>
<td>(113.2)</td>
<td>(°C/W)</td>
</tr>
<tr>
<td>(Ψ_{JT}) Junction-to-top characterization parameter</td>
<td>(Ψ_{JT}) Junction-to-top characterization parameter</td>
<td>(Ψ_{JT}) Junction-to-top characterization parameter</td>
<td>(Ψ_{JT}) Junction-to-top characterization parameter</td>
</tr>
<tr>
<td>(55.5)</td>
<td>(138.5)</td>
<td>(82.3)</td>
<td>(°C/W)</td>
</tr>
<tr>
<td>(Ψ_{JB}) Junction-to-board characterization parameter</td>
<td>(Ψ_{JB}) Junction-to-board characterization parameter</td>
<td>(Ψ_{JB}) Junction-to-board characterization parameter</td>
<td>(Ψ_{JB}) Junction-to-board characterization parameter</td>
</tr>
<tr>
<td>(370.3)</td>
<td>(165.3)</td>
<td>(112.4)</td>
<td>(°C/W)</td>
</tr>
<tr>
<td>(R_{JC(bot)}) Junction-to-case (bottom) thermal resistance</td>
<td>(R_{JC(bot)}) Junction-to-case (bottom) thermal resistance</td>
<td>(R_{JC(bot)}) Junction-to-case (bottom) thermal resistance</td>
<td>(R_{JC(bot)}) Junction-to-case (bottom) thermal resistance</td>
</tr>
<tr>
<td>(165.1)</td>
<td>N/A</td>
<td>N/A</td>
<td>(°C/W)</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
6.5 Electrical Characteristics

$V_S = 1.8 \text{ V to } 5 \text{ V}, \quad V_{CM} = V_S / 2$; minimum and maximum values are at $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (unless otherwise noted). Typical values are at $T_A = 25^\circ\text{C}$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IO}$</td>
<td>Input offset voltage</td>
<td>$V_S = 1.8 \text{ V and } 5 \text{ V}, \quad V_{CM} = V_S / 2$</td>
<td>±0.5</td>
<td>±8</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{HYS}$</td>
<td>Hysteresis</td>
<td>$V_S = 1.8 \text{ V and } 5 \text{ V}, \quad V_{CM} = V_S / 2$</td>
<td>1.2</td>
<td>4.2</td>
<td>14</td>
</tr>
<tr>
<td>$V_{CM}$</td>
<td>Common-mode voltage range</td>
<td>$V_S = 2.5 \text{ V to } 5 \text{ V}$</td>
<td>$V_{EE}$</td>
<td>$V_{CC} + 0.1$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = 1.8 \text{ V to } 2.5 \text{ V}$</td>
<td>$V_{EE} + 0.1$</td>
<td>$V_{CC} + 0.1$</td>
<td></td>
</tr>
<tr>
<td>$I_G$</td>
<td>Input bias current</td>
<td></td>
<td>5</td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input offset current</td>
<td></td>
<td>1</td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output voltage high (for TLV7011 only)</td>
<td>$V_S = 5 \text{ V}, \quad I_O = 3 \text{ mA}$</td>
<td>4.7</td>
<td>4.8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output voltage low</td>
<td>$V_S = 5 \text{ V}, \quad I_O = 3 \text{ mA}$</td>
<td>120</td>
<td>220</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{KG}$</td>
<td>Open-drain output leakage current (TLV7021 only)</td>
<td>$V_{EE} &lt; V_{CM} &lt; V_{CC}, \quad V_S = 5 \text{ V}$</td>
<td>100</td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio</td>
<td>$V_S = 5 \text{ V}, \quad V_{OD} = +0.1 \text{ V (output high)}$, $V_{PULLUP} = V_{CC}$</td>
<td>78</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power supply rejection ratio</td>
<td>$V_S = 1.8 \text{ V to } 5 \text{ V}, \quad V_{CM} = V_S / 2$</td>
<td>78</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Short-circuit current</td>
<td>$V_S = 5 \text{ V, sourcing}$</td>
<td>65</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = 5 \text{ V, sinking}$</td>
<td>44</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply current</td>
<td>$V_S = 1.8 \text{ V, no load}$</td>
<td>$V_{ID} = -0.1 \text{ V (Output Low)}$</td>
<td>5</td>
<td>10</td>
</tr>
</tbody>
</table>

6.6 Switching Characteristics

Typical values are at $T_A = 25^\circ\text{C}$, $V_{CC} = 5 \text{ V}, \quad V_{CM} = 2.5 \text{ V}$; $C_L = 15 \text{ pF}$, input overdrive = 100 mV (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PHL}$</td>
<td>Propagation delay time, high-to-low</td>
<td>Midpoint of input to midpoint of output, $V_{OD} = 100 \text{ mV}$</td>
<td>260</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>Propagation delay time, low-to-high</td>
<td>Midpoint of input to midpoint of output, $V_{OD} = 100 \text{ mV}$</td>
<td>310</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_R$</td>
<td>Rise time (for TLV7011 only)</td>
<td>20% to 80%</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_F$</td>
<td>Fall time</td>
<td>80% to 20%</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{ON}$</td>
<td>Power-up time (1)</td>
<td></td>
<td>20</td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

(1) During power on, $V_S$ must exceed 1.6 V for $t_{ON}$ before the output tracks the input.

6.7 Timing Diagrams
Figure 2. Propagation Delay Timing Diagram
6.8 Typical Characteristics

\( T_A = 25^\circ\text{C}, \ V_{\text{CC}} = 5 \ \text{V}, \ V_{\text{EE}} = 0 \ \text{V}, \ V_{\text{CM}} = V_{\text{CC}}/2, \ C_L = 15 \ \text{pF} \)

---

**Figure 3. TLV7011 Propagation Delay (L-H) vs. Input Overdrive**

**Figure 4. Propagation Delay (H-L) vs. Input Overdrive**

**Figure 5. TLV7011 Propagation Delay (L-H) vs. Input Overdrive**

**Figure 6. Propagation Delay (H-L) vs. Input Overdrive**

**Figure 7. TLV7021 Propagation Delay (L-H) vs. Input Overdrive**

**Figure 8. Hysteresis vs. Temperature**
Typical Characteristics (continued)

$T_A = 25^\circ C, V_{CC} = 5 \text{ V}, V_{EE} = 0 \text{ V}, V_{CM} = V_{CC}/2, C_L = 15 \text{ pF}$

$V_{CC} = 3.3 \text{ V}$

$V_{CC} = 1.8 \text{ V}$

$V_{CC} = 5 \text{ V}$

Figure 9. Hysteresis vs. Temperature

Figure 10. Hysteresis vs. Temperature

Figure 11. Hysteresis vs. $V_{CM}$

Figure 12. Hysteresis vs. $V_{CM}$

Figure 13. Hysteresis vs. $V_{CM}$

Figure 14. Hysteresis Histogram

Distribution Taken From 10,777 Comparators
Typical Characteristics (continued)

\[ T_A = 25^\circ \text{C}, \ V_{CC} = 5 \text{ V}, \ V_{EE} = 0 \text{ V}, \ V_{CM} = V_{CC}/2, \ C_L = 15 \text{ pF} \]

\[ V_{CC} = 1.8 \text{ V} \]

\[ V_{CC} = 5 \text{ V} \]

\[ V_{CC} = 3.3 \text{ V} \]

\[ V_{CC} = 3.3 \text{ V}, \ 50 \text{ devices} \]

\[ V_{CC} = 5 \text{ V}, \ 50 \text{ devices} \]

\[ V_{CC} = 1.8 \text{ V}, \ 50 \text{ devices} \]
### Typical Characteristics (continued)

**T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF**

#### Figure 21. Input Offset Voltage Histogram

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Input Offset (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40</td>
<td>3</td>
</tr>
<tr>
<td>25</td>
<td>2</td>
</tr>
<tr>
<td>85</td>
<td>1</td>
</tr>
<tr>
<td>125</td>
<td>0</td>
</tr>
</tbody>
</table>

Distribution Taken From 10,777 Comparators

#### Figure 22. TLV7011 Output Voltage High vs. Output Source Current

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>V_{OH} (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40</td>
<td>1.8</td>
</tr>
<tr>
<td>25</td>
<td>1.78</td>
</tr>
<tr>
<td>85</td>
<td>1.795</td>
</tr>
<tr>
<td>125</td>
<td>1.81</td>
</tr>
</tbody>
</table>

#### Figure 23. TLV7011 Output Voltage High vs. Output Source Current

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>I_{OUT} (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40</td>
<td>0.1</td>
</tr>
<tr>
<td>25</td>
<td>0.2</td>
</tr>
<tr>
<td>85</td>
<td>0.3</td>
</tr>
<tr>
<td>125</td>
<td>0.4</td>
</tr>
</tbody>
</table>

#### Figure 24. Output Voltage Low vs. Output Sink Current

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>I_{OL} (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40</td>
<td>0</td>
</tr>
<tr>
<td>25</td>
<td>0.01</td>
</tr>
<tr>
<td>85</td>
<td>0.02</td>
</tr>
<tr>
<td>125</td>
<td>0.03</td>
</tr>
</tbody>
</table>

#### Figure 25. Output Voltage Low vs. Output Sink Current

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>V_{OL} (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40</td>
<td>0.05</td>
</tr>
<tr>
<td>25</td>
<td>0.03</td>
</tr>
<tr>
<td>85</td>
<td>0.015</td>
</tr>
<tr>
<td>125</td>
<td>0.01</td>
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</table>

#### Figure 26. Output Short-Circuit (Sink) Current vs. Temperature

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>I_{CM} (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40</td>
<td>60</td>
</tr>
<tr>
<td>25</td>
<td>50</td>
</tr>
<tr>
<td>85</td>
<td>40</td>
</tr>
<tr>
<td>125</td>
<td>30</td>
</tr>
</tbody>
</table>

**V_{CC} = 1.8 V**

**V_{CM} = V_{CC}/2**

---

[Figure 21. Input Offset Voltage Histogram](#)

[Figure 22. TLV7011 Output Voltage High vs. Output Source Current](#)

[Figure 23. TLV7011 Output Voltage High vs. Output Source Current](#)

[Figure 24. Output Voltage Low vs. Output Sink Current](#)

[Figure 25. Output Voltage Low vs. Output Sink Current](#)

[Figure 26. Output Short-Circuit (Sink) Current vs. Temperature](#)
Typical Characteristics (continued)

\[ T_A = 25^\circ C, \ V_{CC} = 5 \ V, \ V_{EE} = 0 \ V, \ V_{CM} = \frac{V_{CC}}{2}, \ C_L = 15 \ pF \]

\[ V_{CM} = \frac{V_{CC}}{2} \]

**Figure 27. TLV7011 Output Short-Circuit (Source) Current vs. Temperature**

**Figure 28. Output Short Circuit (Sink) vs. \( V_{CC} \)**

**Figure 29. TLV7011 Output Short Circuit (Source) vs. \( V_{CC} \)**

**Figure 30. \( I_{CC} \) vs. Temperature**

**Figure 31. \( I_{CC} \) vs. \( V_{CC} \)**

\[ V_{CM} = \frac{V_{CC}}{2} \]

**Figure 32. \( I_{CC} \) vs. \( V_{CM} \)**

\[ V_{CC} = 3.3 \ V \]

\[ V_{CC} = 3.5 \ V \]

\[ V_{CC} = 5.5 \ V \]
Typical Characteristics (continued)

\[ T_A = 25^\circ C, \quad V_{CC} = 5 \text{ V}, \quad V_{EE} = 0 \text{ V}, \quad V_{CM} = V_{CC}/2, \quad C_L = 15 \text{ pF} \]

![Graph showing I\(_{CC}\) vs. \(V_{CM}\)](image)

\[ V_{CC} = 5 \text{ V} \]

**Figure 33.** I\(_{CC}\) vs. \(V_{CM}\)

![Graph showing Input Bias Current vs. Temperature](image)

\[ V_{CC} = 3.3 \text{ V} \]

**Figure 34.** Input Bias Current vs. Temperature

![Graph showing Output Rise Time vs. Load Capacitance](image)

\[ V_{OD} = 100\text{mV} \]

**Figure 35.** TLV7011 Output Rise Time vs. Load Capacitance

![Graph showing Output Fall Time vs. Load Capacitance](image)

\[ V_{OD} = 100\text{mV} \]

**Figure 36.** Output Fall Time vs. Load Capacitance
7 Detailed Description

7.1 Overview
The TLV7011 and TLV7021 devices are single-channel, micro-power comparators with push-pull and open-drain outputs. Operating from 1.6 V to 5.5 V and consuming only 5 µA, the TLV7011 and TLV7021 are ideally suited for portable and industrial applications. The TLV7011 and TLV7021 are available in an ultra-small X2SON package (0.8 x 0.8 mm) to offer significant board space saving in space-challenged designs. Small 5-pin SC70 and SOT-23 packages are also available for these devices.

7.2 Functional Block Diagram

![Functional Block Diagram](image)

7.3 Feature Description
The TLV7011 (push-pull) and TLV7021 (open-drain) devices are micro-power comparators that are capable of operating at low voltages. The TLV7011 and TLV7021 feature a rail-to-rail input stage capable of operating up to 100 mV beyond the VCC power supply rail. The TLV7011 and TLV7021 also feature a push-pull and open-drain output stage with internal hysteresis.

7.4 Device Functional Modes
The TLV7011 and TLV7021 have a Power-on-Reset (POR) circuit. While the power supply (V_S) is ramping up or ramping down, the POR circuitry will be activated.

For the TLV7011, the POR circuit will hold the output low (at V_{EE}) while activated.

For the TLV7021, the POR circuit will keep the output high impedance (logical high) while activated.

When the supply voltage is greater than, or equal to, the minimum supply voltage, the comparator output reflects the state of the differential input (V_{ID}).

7.4.1 Inputs
The TLV7011 and TLV7021 input common-mode extends from V_{EE} to 100 mV above V_{CC}. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output will occur when the input pins exceed V_{CC} and V_{EE}.
Device Functional Modes (continued)

While TI recommends operating the TLV7011 and TLV7021 within the specified range of the \textit{Electrical Characteristics} table, the inputs are fault tolerant to voltages up to 5.5 V independent of the applied \(V_{CC}\) value. Fault tolerant is defined as maintaining the same high input impedance when \(V_{CC}\) is unpowered or within the recommended operating range. Because the inputs of the TLV7011 and TLV7021 are fault tolerant, the inputs to the comparator can be any value between 0 V and 5.5 V while \(V_{CC}\) is ramping up or staying at 0 V. This feature allows any supply and input driven sequence as long as the input value and supply are within the specified ranges. In this case, no current limiting resistor is required. This is possible since the \(V_{CC}\) is isolated from the inputs such that it maintains its value even when a higher voltage is applied to the input.

The input bias current is typically 1 pA for input voltages between \(V_{CC}\) and \(V_{EE}\). The comparator inputs are protected from undervoltage by internal diodes connected to \(V_{EE}\). As the input voltage goes under \(V_{EE}\), the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles every 10°C temperature increases.

7.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in Figure 37. This curve is a function of three components: \(V_{TH}\), \(V_{OS}\), and \(V_{HYST}\):

- \(V_{TH}\) is the actual set voltage or threshold trip voltage.
- \(V_{OS}\) is the internal offset voltage between \(V_{IN+}\) and \(V_{IN-}\). This voltage is added to \(V_{TH}\) to form the actual trip point at which the comparator must respond to change output states.
- \(V_{HYST}\) is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise (4.2 mV for the TLV7011).

![Figure 37. Hysteresis Transfer Curve](image)

7.4.3 Output

The TLV7011 features a push-pull output stage eliminating the need for an external pullup resistor. On the other hand, the TLV7021 features an open-drain output stage enabling the output logic levels to be pulled up to an external source up to 6 V independently of the supply voltage.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV7011 and TLV7021 are micro-power comparators with reasonable response time. The comparators have a rail-to-rail input stage that can monitor signals beyond the positive supply rail with integrated hysteresis. When higher levels of hysteresis are required, positive feedback can be externally added. The push-pull output stage of the TLV7011 is optimal for reduced power budget applications and features no shoot-through current. When level shifting or wire-ORing of the comparator outputs is needed, the TLV7021 with its open-drain output stage is well suited to meet the system needs. In either case, the wide operating voltage range, low quiescent current, and micro-package of the TLV7011 and TLV7021 make these comparators excellent candidates for battery-operated and portable, handheld designs.

8.1.1 Inverting Comparator With Hysteresis for TLV7011

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 38. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. Equation 1 defines the high-to-low trip voltage (V_{A1}).

\[ V_{A1} = V_{CC} \times \frac{R2}{(R1 || R3) + R2} \]

When V_{IN} is greater than V_A, the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. Use Equation 2 to define the low to high trip voltage (V_{A2}).

\[ V_{A2} = V_{CC} \times \frac{R2 || R3}{R1 + (R2 || R3)} \]

Equation 3 defines the total hysteresis provided by the network.

\[ \Delta V_A = V_{A1} - V_{A2} \]

Figure 38. TLV7011 in an Inverting Configuration With Hysteresis
Application Information (continued)

8.1.2 Noninverting Comparator With Hysteresis for TLV7011

A noninverting comparator with hysteresis requires a two-resistor network, as shown in Figure 39, and a voltage reference \((V_{\text{REF}})\) at the inverting input. When \(V_{\text{IN}}\) is low, the output is also low. For the output to switch from low to high, \(V_{\text{IN}}\) must rise to \(V_{\text{IN}1}\). Use Equation 4 to calculate \(V_{\text{IN}1}\).

\[
V_{\text{IN}1} = R_1 \times \frac{V_{\text{REF}}}{R_2} + V_{\text{REF}}
\]

When \(V_{\text{IN}}\) is high, the output is also high. For the comparator to switch back to a low state, \(V_{\text{IN}}\) must drop to \(V_{\text{IN}2}\) such that \(V_A\) is equal to \(V_{\text{REF}}\). Use Equation 5 to calculate \(V_{\text{IN}2}\).

\[
V_{\text{IN}2} = \frac{V_{\text{REF}} (R_1 + R_2) - V_{\text{CC}} \times R_1}{R_2}
\]

The hysteresis of this circuit is the difference between \(V_{\text{IN}1}\) and \(V_{\text{IN}2}\), as shown in Equation 6.

\[
\Delta V_{\text{IN}} = V_{\text{CC}} \times \frac{R_1}{R_2}
\]

Figure 39. TLV7011 in a Noninverting Configuration With Hysteresis
8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 40 shows a simple window comparator circuit.

![Diagram of Window Comparator](image)

**Figure 40. Window Comparator**

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 40. Connect V_{CC} to a 3.3-V power supply and V_{EE} to ground. Make R1, R2 and R3 each 10-MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and V_{TH-}). With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-} is 1.1 V. Large resistor values such as 10-MΩ are used to minimize power consumption. The sensor output voltage is applied to the inverting and noninverting inputs of the two TLV7021's. The TLV7021 is used for its open-drain output configuration. Using the TLV7021 allows the two comparator outputs to be Wire-Ored together. The respective comparator outputs will be low when the sensor is less than 1.1 V or greater than 2.2 V. V_{OUT} will be high when the sensor is in the range of 1.1 V to 2.2 V.
Typical Applications (continued)

8.2.1.3 Application Curve

![Application Curve Diagram](image)

Figure 41. Window Comparator Results

8.2.2 IR Receiver Analog Front End

A single TLV7011 device can be used to build a complete IR receiver analog front end (AFE). The nanoamp quiescent current and low input bias current make it possible to be powered with a coin cell battery, which could last for years.

![IR Receiver Analog Front End Diagram](image)

Figure 42. IR Receiver Analog Front End Using TLV7011

8.2.2.1 Design Requirements

For this design, follow these design requirements:

- Use a proper resistor (R₁) value to generate an adequate signal amplitude applied to the inverting input of the comparator.
- The low input bias current Iᵦ (2 pA typical) ensures that a greater value of R₁ to be used.
Typical Applications (continued)

- The RC constant value ($R_2$ and $C_1$) must support the targeted data rate (that is, 9,600 bauds) to maintain a valid tripping threshold.
- The hysteresis introduced with $R_3$ and $R_4$ helps to avoid spurious output toggles.

8.2.2.2 Detailed Design Procedure

The IR receiver AFE design is highly streamlined and optimized. $R_1$ converts the IR light energy induced current into voltage and applies to the inverting input of the comparator. Because a reverse biased IR LED is used as the IR receiver, a higher $I/V$ transimpedance gain is required to boost the amplitude of reduced current. A 10M resistor is used as $R_1$ to support a $1-V, 100-nA$ transimpedance gain. This is made possible with the picoamps Input bias current $I_B$ (5pA typical). The RC network of $R_2$ and $C_1$ establishes a reference voltage $V_{\text{ref}}$ which tracks the mean amplitude of the IR signal. The RC constant of $R_2$ and $C_1$ (about 4.7 ms) is chosen for $V_{\text{ref}}$ to track the received IR current fluctuation but not the actual data bit stream. The noninverting input is connected to $V_{\text{ref}}$ and the output over the $R_3$ and $R_4$ resistor network which provides additional hysteresis for improved guard against spurious toggles.

To reduce the current drain from the coin cell battery, data transmission must be short and infrequent.

8.2.2.3 Application Curve

![Figure 43. IR Receiver AFE Waveforms](image-url)
Typical Applications (continued)

8.2.3 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source.

![Square-Wave Oscillator Diagram]

Figure 44. Square-Wave Oscillator

8.2.3.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor and resistor. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help to reduce BOM cost and board space.

8.2.3.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

Figure 45. Square-Wave Oscillator Timing Thresholds

First consider the output of Figure Figure 44 is high which indicates the inverted input $V_C$ is lower than the noninverting input ($V_A$). This causes the $C_1$ to be charged through $R_4$, and the voltage $V_C$ increases until it is equal to the noninverting input. The value of $V_A$ at the point is calculated by Equation 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 R_3}$$

(7)

if $R_1 = R_2 = R_3$, then $V_{A1} = 2 V_{CC}/3$
Typical Applications (continued)

At this time the comparator output trips pulling down the output to the negative rail. The value of $V_A$ at this point is calculated by Equation 8.

$$V_{A2} = \frac{V_{CC}(R_2 IR_3)}{R_1 + R_2 IR_3}$$

(8)

if $R_1 = R_2 = R_3$, then $V_{A2} = \frac{V_{CC}}{3}$

The $C_1$ now discharges though the $R_4$, and the voltage $V_{CC}$ decreases until it reaches $V_{A2}$. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for $C_1$ from $2V_{CC}/3$ to $V_{CC}/3$ then back to $2V_{CC}/3$, which is given by $R_4 C_1 \times \ln 2$ for each trip. Therefore, the total time duration is calculated as $2 R_4 C_1 \times \ln 2$. The oscillation frequency can be obtained by Equation 9:

$$f = \frac{1}{(2 R_4 C_1 \times \ln 2)}$$

(9)

8.2.3.3 Application Curve

Figure 46 shows the simulated results of tan oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100 \, \text{k}\Omega$
- $C_1 = 100 \, \text{pF}, C_L = 20 \, \text{pF}$
- $V_+ = 5 \, \text{V}, V_- = \text{GND}$
- $C_{\text{stray}}$ (not shown) from $V_A$ TO GND = 10 pF

![Figure 46. Square-Wave Oscillator Output Waveform](image-url)
9 Power Supply Recommendations

The TLV7011 and TLV7021 have a recommended operating voltage range \( (V_S) \) of 1.6 V to 5.5 V. \( V_S \) is defined as \( V_{CC} - V_{EE} \). Therefore, the supply voltages used to create \( V_S \) can be single-ended or bipolar. For example, single-ended supply voltages of 5 V and 0 V and bipolar supply voltages of +2.5 V and –2.5 V create comparable operating voltages for \( V_S \). However, when bipolar supply voltages are used, it is important to realize that the logic low level of the comparator output is referenced to \( V_{EE} \).

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

10 Layout

10.1 Layout Guidelines

To reduce PCB fabrication cost and improve reliability, TI recommends using a 4-mil via at the center pad connected to the ground trace or plane on the bottom layer.

A power-supply bypass capacitor of 100 nF is recommended when supply output impedance is high, supply traces are long, or when excessive noise is expected on the supply lines. Bypass capacitors are also recommended when the comparator output drives a long trace or is required to drive a capacitive load. Due to the fast rising and falling edge rates and high-output sink and source capability of the TLV7011 and TLV7021 output stages, higher than normal quiescent current can be drawn from the power supply. Under this circumstance, the system would benefit from a bypass capacitor across the supply pins.

10.2 Layout Example

![Figure 47. Layout Example](image-url)
11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV70x1 device family. The TLV7011 Micro-Power Comparator Dip Adaptor Evaluation Module can be requested at the Texas Instruments website through the product folder or purchased directly from the TI eStore.

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

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<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
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</thead>
<tbody>
<tr>
<td>TLV7011</td>
<td>Click here</td>
<td>Click here</td>
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<tr>
<td>TLV7021</td>
<td>Click here</td>
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</tr>
</tbody>
</table>

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community  TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support  TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

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<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
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</tr>
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</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.**: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# TAPE AND REEL INFORMATION

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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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*All dimensions are nominal.*
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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<tr>
<th>Device</th>
<th>Package Type</th>
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<th>Pins</th>
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<th>Width (mm)</th>
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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.
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