LM98714 Three Channel, 16-Bit, 45 MSPS Analog Front End with LVDS/CMOS Output and Integrated CCD/CIS Sensor Timing Generator

Check for Samples: LM98714

FEATURES

- **LVDS/CMOS Outputs**
- **LVDS/CMOS Pixel Rate Input Clock or ADC Input Clock**
- **CDS or S/H Processing for CCD or CIS Sensors**
- **Independent Gain/Offset Correction for Each Channel**
- **Digital Black Level Correction Loop for Each Channel**
- **Programmable Input Clamp Voltage**
- **Flexible CCD/CIS Sensor Timing Generator**

APPLICATIONS

- **Multi-Function Peripherals**
- **Facsimile Equipment**
- **Flatbed or Handheld Color Scanners**
- **High-Speed Document Scanner**

KEY SPECIFICATIONS

- **Maximum Input Level: 1.2 or 2.4 Volt Modes**
  - **(Both with + or - Polarity Option)**
- **ADC Resolution: 16-Bit**
- **ADC Sampling Rate: 45 MSPS**
- **INL: ±23 LSB (Typ)**
- **Channel Sampling Rate: 15/22.5/30 MSPS**
- **PGA Gain Steps: 256 Steps**
- **PGA Gain Range: 0.7 to 7.84x**
- **Analog DAC Resolution: ±9 Bits**
- **Analog DAC Range: ±300mV or ±600mV**
- **Digital DAC Resolution: ±6 Bits**
- **Digital DAC Range: -1024 LSB to + 1008 LSB**
- **SNR: -74dB (@ 0 dB PGA Gain)**
- **Power Dissipation: 505 mW (LVDS) 610 mW (CMOS)**
- **Operating Temp: 0 to 70°C**
- **Supply Voltage: 3.3 V Nominal (3.0 V to 3.6 V Range)**

DESCRIPTION

The LM98714 is a fully integrated, high performance 16-Bit, 45 MSPS signal processing solution for digital color copiers, scanners, and other image processing applications. High-speed signal throughput is achieved with an innovative architecture utilizing Correlated Double Sampling (CDS), typically employed with CCD arrays, or Sample and Hold (S/H) inputs (for Contact Image Sensors and CMOS image sensors). The signal paths utilize 8 bit Programmable Gain Amplifiers (PGA), a ±9-Bit offset correction DAC and independently controlled Digital Black Level correction loops for each input. The PGA and offset DAC are programmed independently allowing unique values of gain and offset for each of the three inputs. The signals are then routed to a 45MHz high performance analog-to-digital converter (ADC). The fully differential processing channel shows exceptional noise immunity, having a very low noise floor of –74dB. The 16-bit ADC has excellent dynamic performance making the LM98714 transparent in the image reproduction chain.

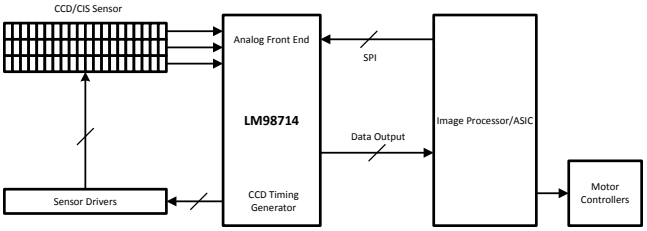

Figure 1. System Block Diagram

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LM98714 Overall Chip Block Diagram

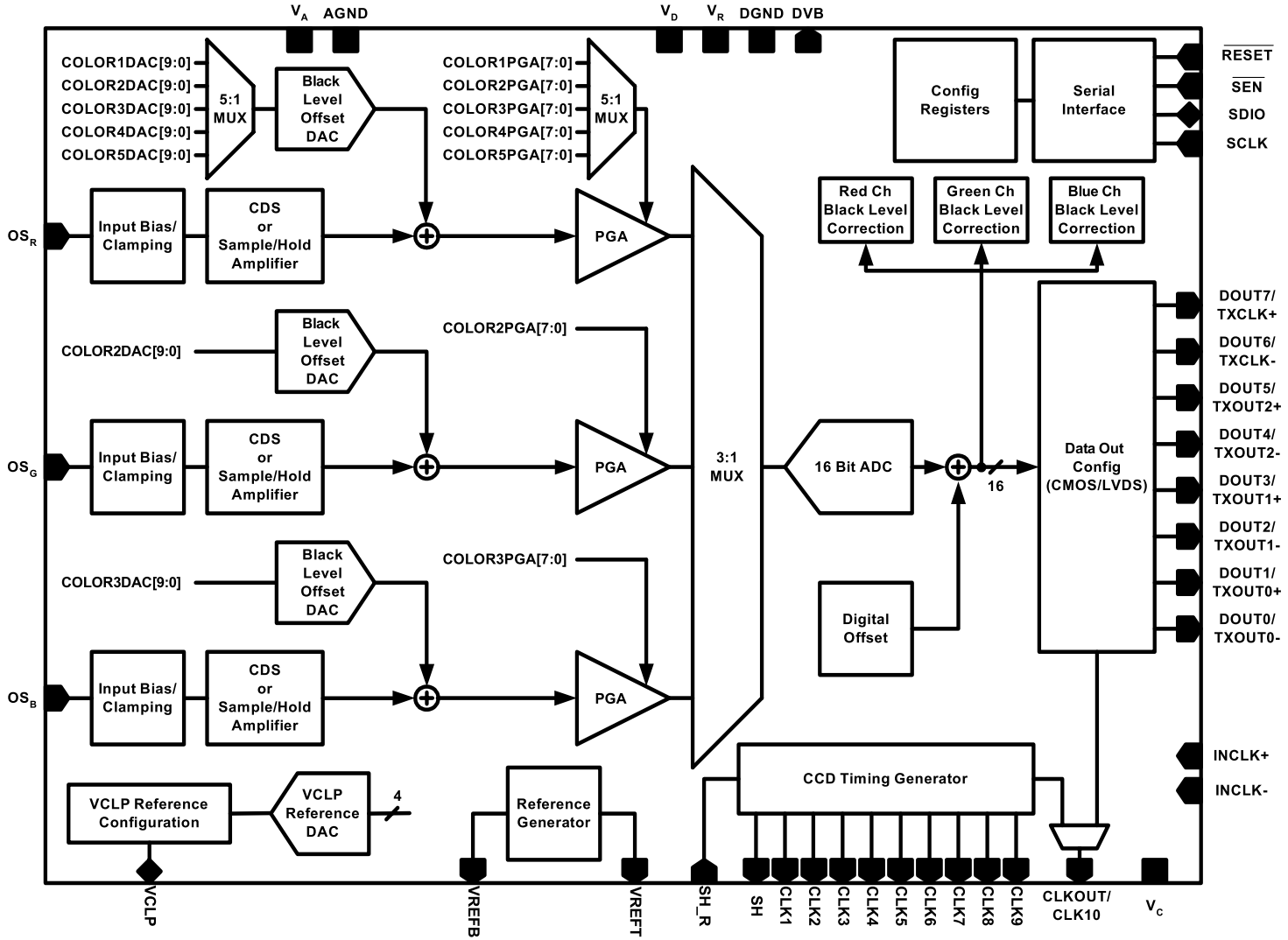

Figure 2. Chip Block Diagram

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LM98714 Pin Out Diagram

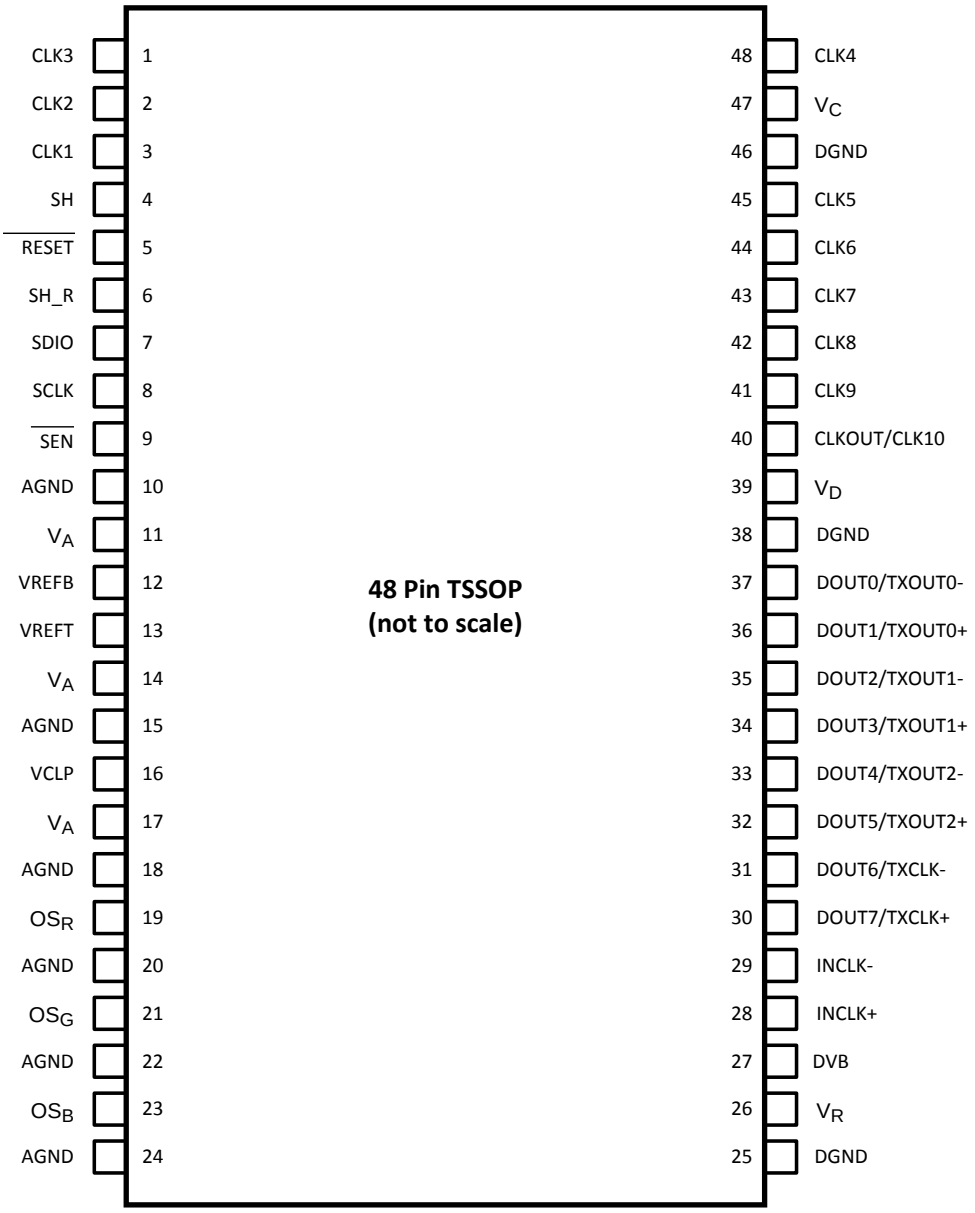

Figure 3. LM98714 Pin Out Diagram

Typical Application Diagram

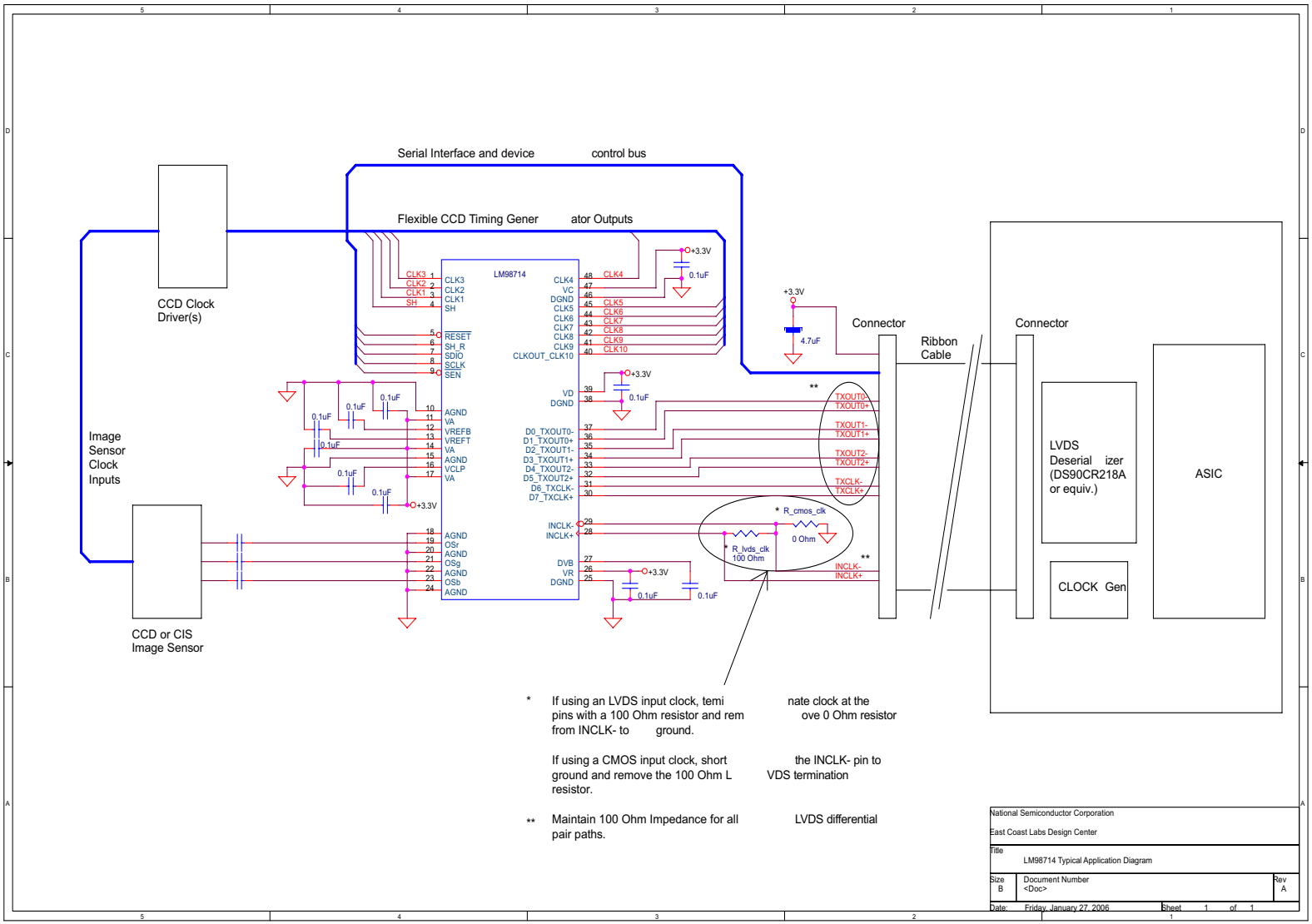

Figure 4. Typical Application Diagram

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PIN DESCRIPTIONS(1)

Pin	Name	I/O	Typ	Res	Description
1	CLK3	O	D	PU	Configurable sensor control output.
2	CLK2	O	D	PD	Configurable sensor control output.
3	CLK1	O	D	PU	Configurable sensor control output.
4	SH	O	D	PD	Sensor - Shift or transfer control signal for CCD and CIS sensors.
5	$\overline{\text{RESET}}$	I	D	PU	Active-low master reset. NC when function not being used.
6	SH_R	I	D	PD	External request for an SH pulse.
7	SDIO	I/O	D		Serial Interface Data Input
8	SCLK	I	D	PD	Serial Interface shift register clock.
9	$\overline{\text{SEN}}$	I	D	PU	Active-low chip enable for the Serial Interface.
10	AGND		P		Analog ground return.
11	V_A		P		Analog power supply. Bypass voltage source with 4.7µF and pin with 0.1µF to AGND.
12	VREFB	O	A		Bottom of ADC reference. Bypass with a 0.1µF capacitor to ground.
13	VREFT	O	A		Top of ADC reference. Bypass with a 0.1µF capacitor to ground.
14	V_A		P		Analog power supply. Bypass voltage source with 4.7µF and pin with 0.1µF to AGND.
15	AGND		P		Analog ground return.
16	VCLP	IO	A		Input Clamp Voltage. Normally bypassed with a 0.1µF, and a 4.7µF capacitor to AGND. An external reference voltage may be applied to this pin.
16	VCLP	IO	A		Input Clamp Voltage. Normally bypassed with a 0.1µF , and a 10µF capacitor to AGND. An external reference voltage may be applied to this pin.
17	V_A		P		Analog power supply. Bypass voltage source with 4.7µF and pin with 0.1µF to AGND.
18	AGND		P		Analog ground return.
19	OS_R	I	A		Analog input signal. Typically sensor Red output AC-coupled thru a capacitor.
20	AGND		P		Analog ground return.
21	OS_G	I	A		Analog input signal. Typically sensor Green output AC-coupled thru a capacitor.
22	AGND		P		Analog ground return.
23	OS_B	I	A		Analog input signal. Typically sensor Blue output AC-coupled thru a capacitor.
24	AGND		P		Analog ground return.
25	DGND		P		Digital ground return.
26	V_R		P		Power supply input for internal voltage reference generator. Bypass this supply pin with a 0.1µF capacitor.
27	DVB	O	D		Digital Core Voltage bypass. Not an input. Bypass with 0.1µF capacitor to DGND.
28	INCLK+	I	D		Clock Input. Non-Inverting input for LVDS clocks or CMOS clock input. CMOS clock is selected when pin 29 is held at DGND, otherwise clock is configured for LVDS operation.
29	INCLK-	I	D		Clock Input. Inverting input for LVDS clocks, connect to DGND for CMOS clock.
30	DOUT7/	O	D		Bit 7 of the digital video output bus in CMOS Mode, LVDS Frame Clock+ in LVDS Mode.
	TXCLK+				
31	DOUT6/	O	D		Bit 6 of the digital video output bus in CMOS Mode, LVDS Frame Clock- in LVDS Mode.
	TXCLK-				
32	DOUT5/	O	D		Bit 5 of the digital video output bus in CMOS Mode, LVDS Data Out2+ in LVDS Mode.
	TXOUT2+				
33	DOUT4/	O	D		Bit 4 of the digital video output bus in CMOS Mode, LVDS Data Out2- in LVDS Mode.
	TXOUT2-				
34	DOUT3/	O	D		Bit 3 of the digital video output bus in CMOS Mode, LVDS Data Out1+ in LVDS Mode.
	TXOUT1+				
35	DOUT2/	O	D		Bit 2 of the digital video output bus in CMOS Mode, LVDS Data Out1- in LVDS Mode.
	TXOUT1-				

(1) (I=Input), (O=Output), (IO=Bi-directional), (P=Power), (D=Digital), (A=Analog), (PU=Pull Up with an internal resistor), (PD=Pull Down with an internal resistor.).

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PIN DESCRIPTIONS[1] (continued)

Pin	Name	I/O	Typ	Res	Description
36	DOUT1/ TXOUT0+	O	D		Bit 1 of the digital video output bus in CMOS Mode, LVDS Data Out0+ in LVDS Mode.
37	DOUT0/ TXOUT0-	O	D		Bit 0 of the digital video output bus in CMOS Mode, LVDS Data Out0- in LVDS Mode.
38	DGND		P		Digital ground return.
39	V_D		P		Power supply for the digital circuits. Bypass this supply pin with 0.1µF capacitor. A single 4.7µF capacitor should be used between the supply and the VD, VR and VC pins.
40	CLKOUT/ CLK10	O	D	PD	Output clock for registering output data when using CMOS outputs, or configurable sensor control output.
41	CLK9	O	D	PD	Configurable sensor control output.
42	CLK8	O	D	PD	Configurable sensor control output.
43	CLK7	O	D	PD	Configurable sensor control output.
44	CLK6	O	D	PU	Configurable sensor control output.
45	CLK5	O	D	PD	Configurable sensor control output.
46	DGND		P		Digital ground return.
47	V_C		P		Power supply for the sensor control outputs. Bypass this supply pin with 0.1µF capacitor.
48	CLK4	O	D	PD	Configurable sensor control output.

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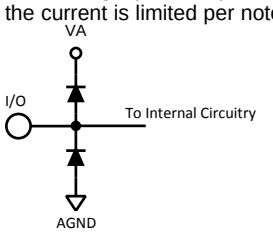
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage (VA,VR,VD,VC)		4.2 V
Voltage on Any Input Pin (Not to exceed 4.2 V)(3)		−0.3 V to (VA + 0.3 V)
Voltage on Any Output Pin (execpt DVB and not to exceed 4.2 V)		−0.3 V to (VA + 0.3 V)
DVB Output Pin Voltage		2.0V
Input Current at any pin other than Supply Pins(4)		±25 mA
Package Input Current (except Supply Pins)(4)		±50 mA
Maximum Junction Temperature (T_A)		150°C
Thermal Resistance (θ_{JA})		66°C/W
Package Dissipation at T_A = 25°C(5)		1.89 W
ESD Rating(6)	Human Body Model	2500 V
	Machine Model	250 V
Storage Temperature		−65°C to +150°C
Soldering process must comply with Texas Instruments' Reflow Temperature Profile specifications. Refer to www.ti.com/packaging(7)		

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the Operating Ratings is not recommended.
(2) All voltages are measured with respect to AGND = DGND = 0V, unless otherwise specified.
(3) The analog inputs are protected as shown below. Input voltage magnitudes beyond the supply rails will not damage the device, provided the current is limited per note 3. However, input errors will be generated If the input goes above VA and below AGND.



(4) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V_A or V_D), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.
(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (for example, when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0 Ω.
(7) Reflow temperature profiles are different for lead-free and non-lead-free packages.

Operating Ratings(1)(2)

Operating Temperature Range	0°C ≤ T_A ≤ +70°C
All Supply Voltage	+3.0 V to +3.6 V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the Operating Ratings is not recommended.
(2) All voltages are measured with respect to AGND = DGND = 0V, unless otherwise specified.

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Electrical Characteristics

The following specifications apply for VA = VD = VR = VC = 3.3V, C_L = 10pF, and f_{INCLK} = 15MHz unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
CMOS Digital Input DC Specifications (RESETb, SH_R, SCLK, SENb)						
V_{IH}	Logical “1” Input Voltage		2.0			V
V_{IL}	Logical “0” Input Voltage				0.8	V
I_{IH}	Logical “1” Input Current	V_{IH} = VD $\overline{RESET}$ SH_R, SCLK $\overline{SEN}$		 235 70 130		 nA µA nA
I_{IL}	Logical “0” Input Current	VIL = DGND $\overline{RESET}$ SH_R, SCLK $\overline{SEN}$		 70 235 70		 µA nA µA
CMOS Digital Output DC Specifications (SH, CLK1 to CLK10, CMOS Data Outputs)						
V_{OH}	Logical “1” Output Voltage	I_{OUT} = -0.5mA	2.95			V
V_{OL}	Logical “0” Output Voltage	I_{OUT} = 1.6mA			0.25	V
I_{OS}	Output Short Circuit Current	V_{OUT} = DGND V_{OUT}= VD		16 -20		mA
I_{OZ}	CMOS Output TRI-STATE Current	V_{OUT} = DGND V_{OUT} = VD		20 -25		nA
CMOS Digital Input/Output DC Specifications (SDIO)						
I_{IH}	Logical “1” Input Current	V_{IH} = VD		90		nA
I_{IL}	Logical “0” Input Current	V_{IL} = DGND		90		nA
LVDS/CMOS Clock Receiver DC Specifications (INCLK+ and INCLK- Pins)						
V_{IHL}	Differential LVDS Clock High Threshold Voltage	R_L = 100W, V_{CM} (LVDS Input Common Mode Voltage)= 1.25V			100	mV
V_{ILL}	Differential LVDS Clock Low Threshold Voltage		-100			mV
V_{IHC}	CMOS Clock High Threshold Voltage	INCLK- = DGND	2.0			V
V_{ILC}	CMOS Clock Low Threshold Voltage				0.8	V
I_{IHL}	CMOS Clock Input High Current				280	µA
I_{ILC}	CMOS Clock Input Low Current				-150	µA
LVDS Output DC Specifications						
V_{OD}	Differential Output Voltage	R_L = 100Ω	180	328	450	mV
V_{OS}	LVDS Output Offset Voltage		1.17	1.23	1.3	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω		7.9		mA

(1) Typical figures are at T_A = 25°C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

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Electrical Characteristics (continued)

The following specifications apply for VA = VD = VR = VC = 3.3V, C_L = 10pF, and f_{INCLK} = 15MHz unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
Power Supply Specifications						
IA	VA Analog Supply Current	VA Normal State	60	97	125	mA
		VA Low Power State (Powerdown)	12	23	32	
IR	VR Digital Supply Current	VR Normal State (LVDS Outputs)	30	64	75	mA
		CMOS Output Data Format	15	47	55	mA
		LVDS Output Data Format with Data Outputs Disabled		47		mA
ID	VD Digital Output Driver Supply Current	LVDS Output Data Format		0.05		mA
		CMOS Output Data Format (ATE Loading of CMOS Outputs > 50pF)	12		40	mA
IC	VC CCD Timing Generator Output Driver Supply Current	Typical sensor outputs: SH, CLK1=Φ1A, CLK2=Φ2A, CLK3=ΦB, CLK4=ΦC, CLK5=RS, CLK6=CP (ATE Loading of CMOS Outputs > 50pF)	0.5		12	mA
PWR	Average Power Dissipation	LVDS Output Data Format	350	505	650	mW
		CMOS Output Data Format (ATE Loading of CMOS Outputs > 50pF)	380	610	700	mW
Input Sampling Circuit Specifications						
V_{IN}	Input Voltage Level	CDS Gain=1x, PGA Gain=1x		2.3		Vp-p
		CDS Gain=2x, PGA Gain= 1x		1.22		
I_{IN_SH}	Sample and Hold Mode Input Leakage Current	Source Followers Off CDS Gain = 1x OS_X = VA (OS_X = AGND)	50 (-70)		70 (-40)	µA
		Source Followers Off CDS Gain = 2x OS_X = VA (OS_X = AGND)	75 (-105)		105 (-75)	µA
		Source Followers On CDS Gain = 2x OS_X = VA (OS_X = AGND)	-200	-10 -16	200	nA
C_{SH}	Sample/Hold Mode Equivalent Input Capacitance (see Figure 12)	CDS Gain = 1x		2.5		pF
		CDS Gain = 2x		4		
I_{IN_CDS}	CDS Mode Input Leakage Current	Source Followers Off OS_X = VA (OS_X = AGND)	-300	7 (-25)	300	nA
R_{CLPIN}	CLPIN Switch Resistance (OS_X to VCLP Node in Figure 9)			16	50	Ω
VCLP Reference Circuit Specifications						
	VCLP DAC Resolution			4		Bits
	VCLP DAC Step Size			0.16		V
V_{VCLP}	VCLP DAC Voltage Min Output	VCLP Config. Register = 0001 0000b	0.14	0.26	0.43	V
	VCLP DAC Voltage Max Output	VCLP Config. Register = 0001 1111b	2.38	2.68	2.93	V
	Resistor Ladder Enabled	VCLP Config. Register = 0010 xxxxb	1.54	V_A / 2	1.73	V
I_{SC}	VCLP DAC Short Circuit Output Current	VCLP Config. Register = 0001 xxxxb		30		mA

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Electrical Characteristics (continued)

The following specifications apply for VA = VD = VR = VC = 3.3V, C_L = 10pF, and f_{INCLK} = 15MHz unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
Black Level Offset DAC Specifications						
	Resolution			10		Bits
	Monotonicity			Ensured by characterization		
	Offset Adjustment Range Referred to AFE Input	CDS Gain = 1x Minimum DAC Code = 0x000 Maximum DAC Code = 0x3FF		-614 614		mV
		CDS Gain = 2x Minimum DAC Code = 0x000 Maximum DAC Code = 0x3FF		-307 307		mV
	Offset Adjustment Range Referred to AFE Output	Minimum DAC Code = 0x000 Maximum DAC Code = 0x3FF	-16000 16000		-18200 18200	LSB
	DAC LSB Step Size	CDS Gain = 1x Referred to AFE Output		1.2 (32)		mV (LSB)
DNL	Differential Non-Linearity		-0.95		3.25	LSB
INL	Integral Non-Linearity		-3.1		2.65	LSB
PGA Specifications						
	Gain Resolution			8		Bits
	Monotonicity			Ensured by characterization		
	Maximum Gain	CDS Gain = 1x	7.18	7.9	8.77	V/V
		CDS Gain = 1x	17.1	17.9	18.9	dB
	Minimum Gain	CDS Gain = 1x	0.56	0.7	0.82	V/V
		CDS Gain = 1x	-5	-3	-1.72	dB
	PGA Function	Gain (V/V) = (196/(280-PGA Code)) Gain (dB) = 20LOG10(196/(280-PGA Code))				
	Channel Matching	Minimum PGA Gain Maximum PGA Gain		3 12.7		%
ADC Specifications						
V_{REFT}	Top of Reference			2.07		V
V_{REFB}	Bottom of Reference			0.89		V
V_{REFT} - V_{REFB}	Differential Reference Voltage		1.07	1.18	1.29	V
	Overrange Output Code			65535		
	Underrange Output Code			0		
Digital Offset "DAC" Specifications						
	Resolution			7		Bits
	Digital Offset DAC LSB Step Size	Referred to AFE Output		16		LSB
	Offset Adjustment Range Referred to AFE Output	Min DAC Code =7b0000000		-1024		LSB
		Mid DAC Code =7b1000000		0		
		Max DAC Code = 7b1111111		1008		

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Electrical Characteristics (continued)

The following specifications apply for VA = VD = VR = VC = 3.3V, C_L = 10pF, and f_{INCLK} = 15MHz unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Units
Full Channel Performance Specifications						
DNL	Differential Non-Linearity		-0.99	0.8/-0.6	2.55	LSB
INL	Integral Non-Linearity		-73	+/-23	78	LSB
Noise Floor		Minimum PGA Gain		-79		dB
				7.2		LSB RMS
		PGA Gain = 1x		-74		dB
				13	30	LSB RMS
		Maximum PGA Gain		-56		dB
				104		LSB RMS
	Channel to Channel Crosstalk	Mode 3		47		LSB
		Mode 2		16		

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AC Timing Specifications

The following specifications apply for VA = VD = VR = VC = 3.3V, C_L = 10pF, and f_{INCLK} = 15MHz unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Units
Input Clock Timing Specifications						
f_{INCLK}	Input Clock Frequency	INCLK = PIXCLK (Pixel Rate Clock)			15 (Mode 3) 22.5 (Mode 2) 30 (Mode 1)	MHz
		INCLK = ADCCLK (ADC Rate Clock)	5		45 (Mode 3) 45 (Mode 2) 30 (Mode 1)	MHz
T_{dc}	Input Clock Duty Cycle		40/60	50/50	60/40	%
Full Channel Latency Specifications						
t_{SHFP}	SH out to First Sampled Pixel Figure 19 (Mode 3) Figure 20 (Mode 2) Figure 21 (Mode 1)	PIXPHASE0		3		T_{ADC}
		PIXPHASE1		3 3/7		
		PIXPHASE2		4		
		PIXPHASE3		4 3/7		
t_{LAT3}	3 Channel Mode Pipeline Delay Figure 53 (LVDS) Figure 58 (CMOS)	PIXPHASE0		19		T_{ADC}
		PIXPHASE1		18 4/7		
		PIXPHASE2		18		
		PIXPHASE3		17 4/7		
t_{LAT2}	2 Channel Mode Pipeline Delay Figure 54 (LVDS) Figure 59(CMOS)	PIXPHASE0		18		T_{ADC}
		PIXPHASE1		17 4/7		
		PIXPHASE2		17		
		PIXPHASE3		16 4/7		
t_{LAT1}	1 Channel Mode Pipeline Delay Figure 55 (LVDS) Figure 60(CMOS)	PIXPHASE0		16		T_{ADC}
		PIXPHASE1		15 4/7		
		PIXPHASE2		15		
		PIXPHASE3		14 4/7		
t_{SHFD}	SH out to First Valid Data (t_{SHFP} + t_{LATx})	Mode 3		22		T_{ADC}
		Mode 2		21		
		Mode 1		19		
SH_R Timing Specifications (Figure 49)						
t_{SHR_S}	SH_R Setup Time		1.28			ns
t_{SHR_H}	SH_R Hold Time		2.25			ns
LVDS Output Timing Specifications (Figure 52)						
TX_{valid}	TX Output Data Valid window	f_{INCLK} = 45MHz INCLK = ADCCLK (ADC Rate Clock)	2			ns
TX_{pp0}	TXCLK to Pulse Position 0	LVDS Output Specifications not tested in production. Min/Max ensured by design, characterization and statistical analysis.		0.013		ns
TX_{pp1}	TXCLK to Pulse Position 1			3.093		ns
TX_{pp2}	TXCLK to Pulse Position 2			6.238		ns
TX_{pp3}	TXCLK to Pulse Position 3			9.613		ns
TX_{pp4}	TXCLK to Pulse Position 4			12.663		ns
TX_{pp5}	TXCLK to Pulse Position 5			15.762		ns
TX_{pp6}	TXCLK to Pulse Position 6			18.982		ns

(1) Typical figures are at T_A = 25°C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

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AC Timing Specifications (continued)

The following specifications apply for VA = VD = VR = VC = 3.3V, C_L = 10pF, and f_{INCLK} = 15MHz unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Units
CMOS Output Timing Specifications						
t_{CRDO}	CLKOUT Rising Edge to CMOS Output Data	f_{INCLK} = 45MHz INCLK = ADCCLK (ADC Rate Clock)	-2.83		2.7	ns
t_{CFDO}	CLKOUT Falling Edge to CMOS Output Data	f_{INCLK} = 45MHz INCLK = ADCCLK (ADC Rate Clock)	-2.83		2.7	ns
Serial Interface Timing Specifications						
f_{SCLK}	Input Clock Frequency	f_{SCLK} <= f_{INCLK} INCLK = PIXCLK (Pixel Rate Clock) Mode 3/2/1			15/22.5/30	MHz
		f_{SCLK} <= f_{INCLK} INCLK = ADCCLK (ADC Rate Clock) Mode 3/2/1			45/45/30	MHz
	SCLK Duty Cycle			50/50		ns
t_{IH}	Input Hold Time		1			ns
t_{IS}	Input Setup Time		4			ns
t_{SENSC}	SCLK Start Time After $\overline{SEN}$ Low		1.25			ns
t_{SCSEN}	$\overline{SEN}$ High after last SCLK Rising Edge		2.82			ns
t_{SENW}	$\overline{SEN}$ Pulse Width	INCLK must be active during serial interface commands.	4			T_{INCLK}
t_{OD}	Output Delay Time			11	14.6	ns
t_{HZ}	Data Output to High Z				0.5	T_{SCLK}

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System Overview

INTRODUCTION

The LM98714 is a 16-bit, three-input, complete Analog Front End (AFE) for digital color copier and Multi-Function Peripheral (MFP) applications. The system block diagram of the LM98714, shown in Figure 2 highlights the main features of the device. Each input has its own Input Bias and Clamping Network which are routed through a selectable Sample/Hold (S/H) or Correlated Double Sampler (CDS) amplifier. A +/-9-Bit Offset DAC applies independent offset correction for each channel. A -3 to 17.9dB Programmable Gain Amplifier (PGA) applies independent gain correction for each channel. The LM98714 also provides independent Digital Black Level Correction Feedback Loops for each channel. The Black Level Correction Loop can be configured to run in Manual Mode (where the user inputs their own values of DAC offset) or in Automatic Mode where the LM98714 calculates each channel's Offset DAC value during optical black pixels and then adjusts the Offset register accordingly. The signals are routed to a single high performance 16-bit, 45MHz analog-to-digital converter.

MODES OF OPERATION INTRODUCTION

The LM98714 can be configured to operate in several different operating modes. The following sections are a brief introduction to these modes of operation. A more rigorous explanation of the operating modes is contained in the Modes of Operation section. including input sampling diagrams for each mode as well as a description of the operating conditions.

Mode 3 - Three Channel Input/Synchronous Pixel Sampling

OS_B, OS_G, and OS_R inputs are sampled synchronously at a pixel rate. The sampled signals are processed with each channel's offset and gain adjusted independently via the control registers. The order in which pixels are processed from the input to the ADC is fully programmable and is synchronized by the SH pulse. In this mode, the maximum channel speed is 15MSPS per channel with the ADC running at 45MSPS yielding a three color throughput of 45MSPS.

Mode 2 - Two Channel Input/Synchronous Pixel Sampling

Mode 2 is useful for CCD sensors with a Black and White mode with Even and Odd outputs. In its default configuration, Mode 2 samples the Even output via the OS_B channel input, and the Odd output via the OS_G channel input. Sampling of the Even and Odd pixels is performed synchronously at a maximum sample rate of 22.5MSPS per input with the ADC running at 45MSPS.

Mode 1a - One Channel Input/One, Two, Three, Four, or Five Color Sequential Line Sampling

In Mode 1a, all pixels are processed through a single input (OS_R, OS_G, or OS_B) chosen through the control register setup. This mode is useful in applications where only one input channel is used. The selected input is programmable through the control register. If more than one color is being sent to the input, the user can configure the OS_R channel to utilize up to five offset and gain coefficients for up to five different lines of color pixels. The SH pulse at the beginning of each line sequences the DAC and PGA coefficients as configured in the control registers. In this mode, the maximum channel speed is 30MSPS per channel with the ADC running at 30MSPS.

Mode 1b - One Channel Input Per Line/Sequential Line (Input) Sampling/Three Channel Processing

In Mode 1b the OS_R, OS_G, and OS_B inputs are sampled one input per line with the input selection being sequenced to the next color by an SH pulse. This mode is useful with sensors that output whole lines of pixels of a single color. The order in which the inputs are sampled is fully programmable. Sequencing from one channel to the next is triggered by the SH pulse. The first SH pulse after this mode is set (or reset) sets up the first programmed input for gain and offset and initiates sampling through that input alone. The next SH pulse switches the active input to the second channel indicated by the configuration registers. This sequencing with SH pulses continues to the third input and then continuously loops through the inputs. In this mode, the maximum channel speed is 30MSPS per channel with the ADC running at 30MSPS.

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INPUT CLOCK INTRODUCTION

The clock input to the LM98714 can be a differential LVDS clock on the INCLK+ and INCLK- pins or a CMOS level clock applied to the INCLK+ pin with the INCLK- pin connected to DGND. The external clock signal format is auto sensed internally. In addition to the two available level formats, the input clock can be applied at the Pixel frequency (PIXCLK) or at the ADC frequency (ADCCLK). The LM98714 can perform internal clock multiplication when a Pixel frequency clock is applied, or no multiplication when an ADC frequency clock is applied. The internal configuration registers need to be written to perform the proper setup of the input clock. The available input clock configurations for each operating mode is outlined in the following table.

AFE Mode	Input Clock Type	Internal Multiplier	INCLK Max Freq.	Configuration Register Settings
Mode 3	INCLK = Pixel Freq. (PIXCLK)	3x	15MHz	PIXCLK Configuration: Main Config Reg 1, Bit[2] = 1'b1
	INCLK = ADC Freq. (ADCCLK)	1x	45MHz	ADCCLK Configuration: Main Config Reg 1, Bit[2] = 1'b0
Mode 2	INCLK = Pixel Freq. (PIXCLK)	2x	22.5MHz	PIXCLK Configuration: Main Config Reg 1, Bit[2] = 1'b1
	INCLK = ADC Freq. (ADCCLK)	1x	45MHz	ADCCLK Configuration: Main Config Reg 1, Bit[2] = 1'b0
Mode 1	INCLK = Pixel Freq. = ADC Freq (ADCCLK = PIXCLK in Mode 1)	1x	30MHz	Main Config Reg 1, Bit[2] = 1'bx

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Modes of Operation

MODE 3 - THREE CHANNEL INPUT/SYNCHRONOUS PIXEL SAMPLING

In Mode 3, the OS_R, OS_G, and OS_B input channels are sampled synchronously. The sampled input signals are then processed in parallel through their respective channels with each channel offset and gain adjusted by their respective control registers. The signals are then routed through a 3-1 MUX to the ADC. The order in which pixels are processed through the MUX to the ADC is programmable (OS_R-OS_G-OS_B, or OS_B-OS_G-OS_R) and is synchronized by the SH pulse.

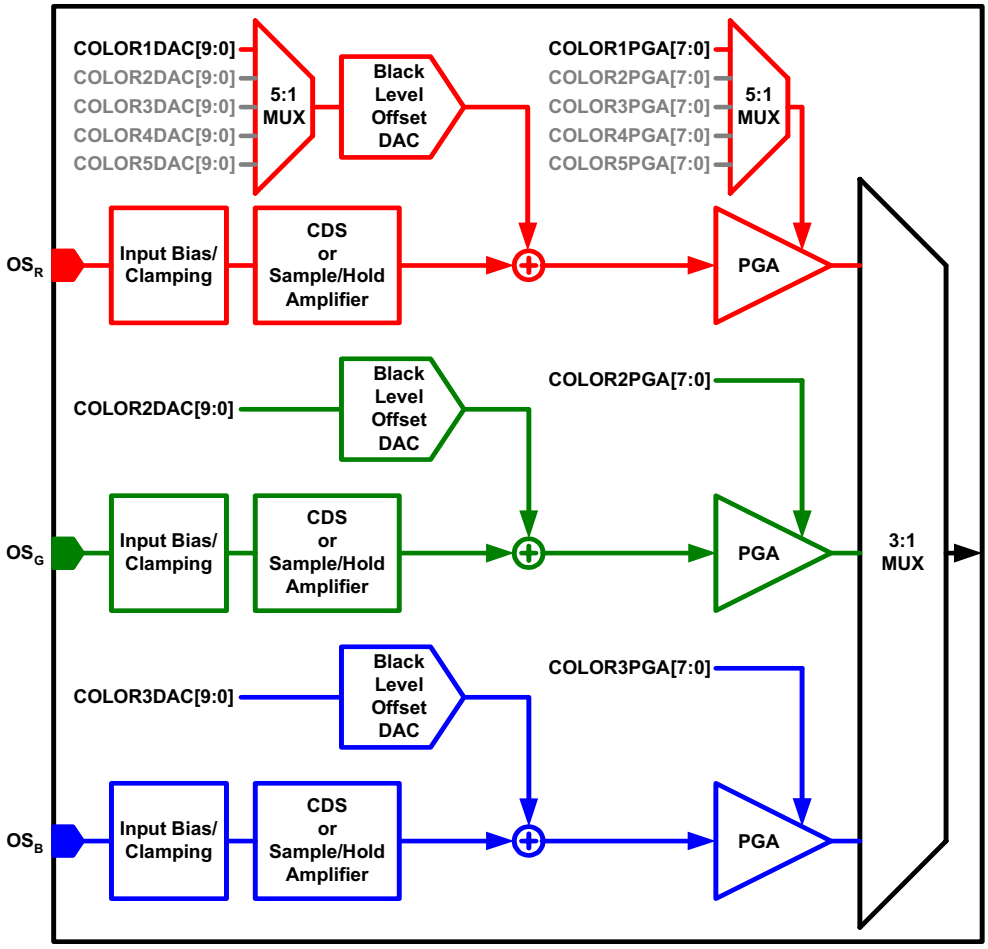

Figure 5. Synchronous Three Channel Pixel Mode Signal Routing

Table 1. Mode 3 Operating Details

			Detail
Channels Active	OS_B & OS_G & OS_R		3 channel synchronous pixel sampling.
Channel Sample Rate	15		MSPS per Channel (max)
ADC Sample Rate		45	MSPS (max)
f_{ADC}: f_{INCLK}	Internal 3x Clock Selected	3:01	f_{INCLK} = 15MHz (max)
	Internal 1x Clock Selected	1:01	f_{INCLK} = 45MHz (max)
Output Sequencing	SH Signal --> R-G-B-R-G-B-R-G-B→ or SH Signal --> B-G-R-B-G-R-B-G-R→		

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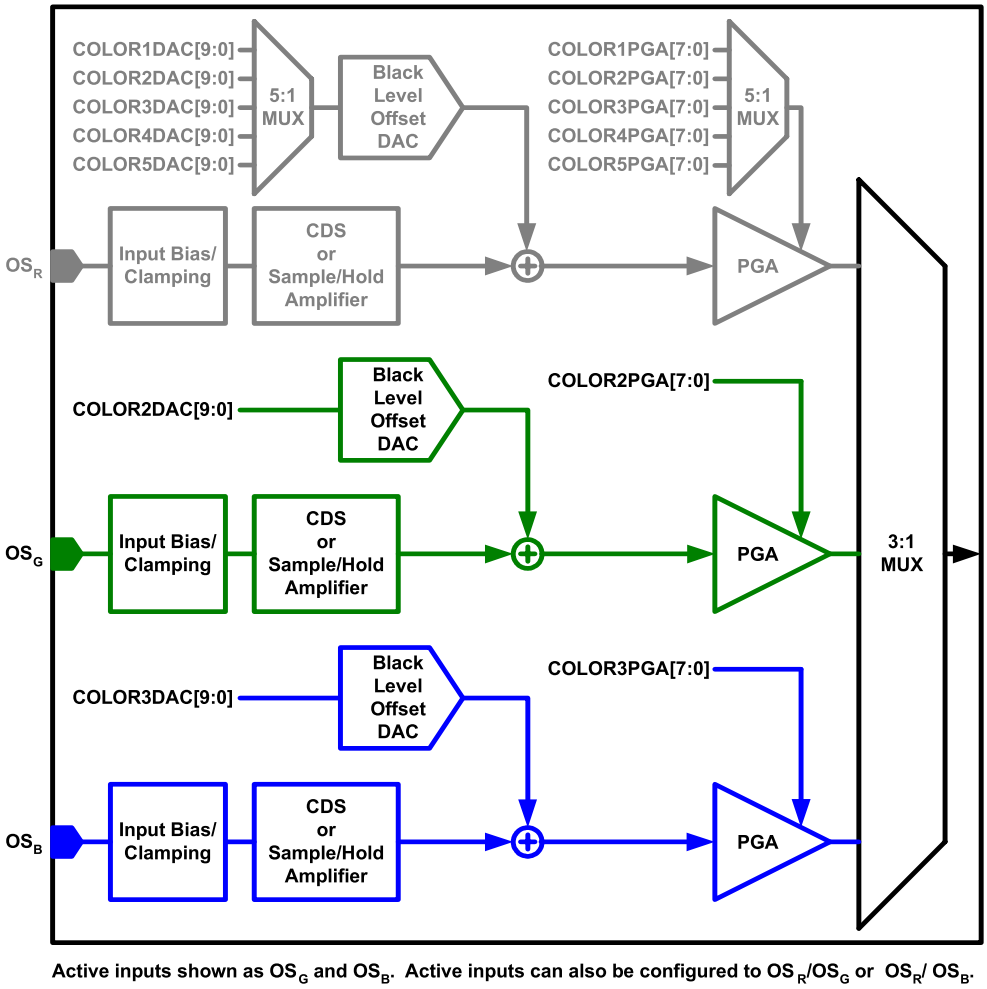
MODE 2 - TWO CHANNEL INPUT/SYNCHRONOUS PIXEL SAMPLING

Mode 2 is useful for CCD sensors with a Black and White line with Even and Odd pixels. In its default configuration, Mode 2 samples Even sensor pixels via the Blue Channel Input, and Odd sensor pixels via the Green Channel Input. The selection of Even/Odd inputs can be changed through the serial interface registers. Sampling of the Even and Odd inputs is performed synchronously.



Active inputs shown as OS_G and OS_B. Active inputs can also be configured to OS_R/OS_G or OS_R/ OS_B.

Figure 6. Mode 2 Signal Routing

Table 2. Mode 2 Operating Details

			Detail
Channels Active	OS_G and OS_B (Default) or OS_R and OS_G or OS_B and OS_R		Two inputs synchronously processed as Even and Odd Pixels. Channel inputs are configurable.
Channel Sample Rate	22.5		MSPS per Channel (max)
ADC Sample Rate		45	MSPS (max)
f_{ADC}: f_{INCLK}	Internal 2x Clock Selected	2:01	f_{INCLK} = 22.5MHz (max)
	Internal 1x Clock Selected	1:01	f_{INCLK} = 45MHz (max)
Output Sequencing	SH Signal --> Even-Odd-Even-Odd-Even-Odd-Even→ or SH Signal --> Odd-Even-Odd-Even-Odd-Even-Odd→		

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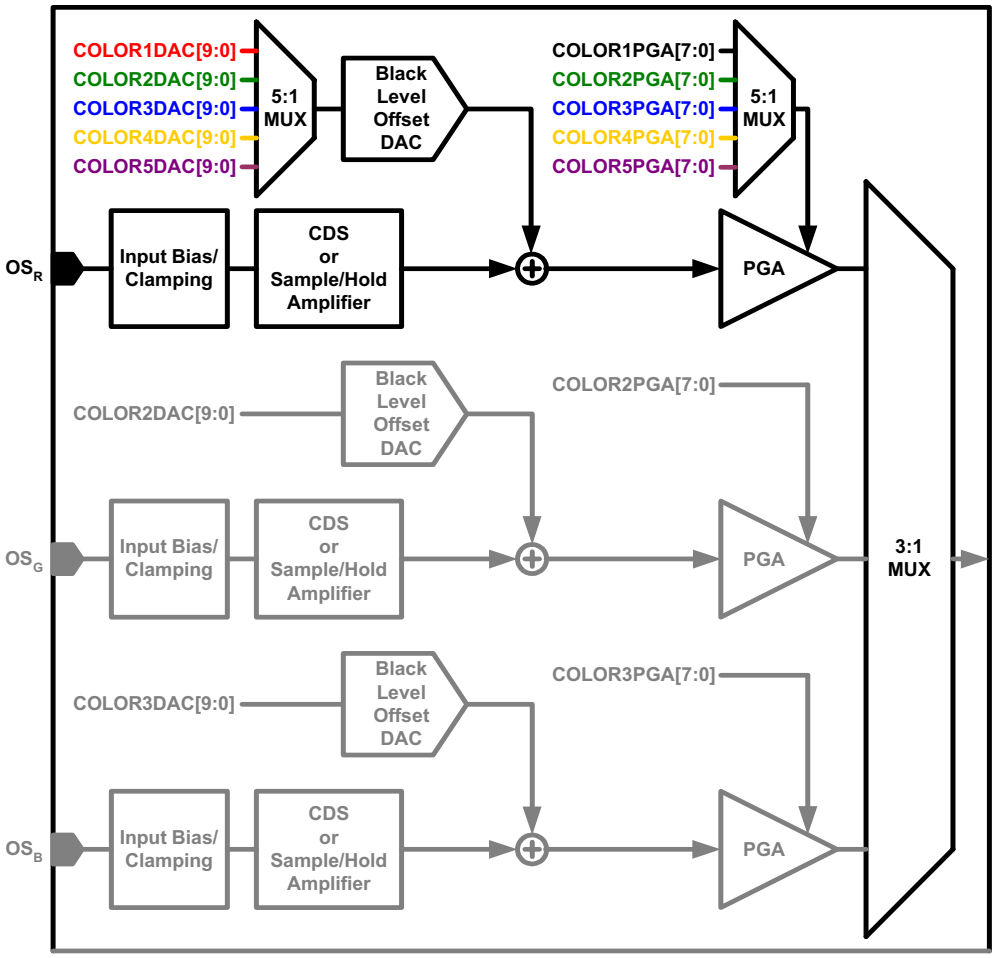
MODE 1A - ONE CHANNEL INPUT/ONE, TWO, THREE, FOUR, OR FIVE COLOR SEQUENTIAL LINE SAMPLING

In Mode 1a, all pixels are processed through a single input (OS_R, OS_G, or OS_B) chosen through the control register setup. This mode is useful in applications where only one input channel is used. The selected input is programmable through the control register. If more than one color is being sent to the input, the user can configure the OS_R channel to utilize up to five offset and gain coefficients for up to five different lines of color pixels. The SH pulse at the beginning of each line sequences the DAC and PGA coefficients as configured in the control registers. In this mode, the maximum channel speed is 30MSPS per channel with the ADC running at 30MSPS.



Up to "Five Color" line sequences shown thru OS_R input. "Single Color" sequences also selectable thru the OS_G and OS_B inputs.

Figure 7. Mode 1a Signal Routing

Table 3. Mode 1a Operating Details

			Detail
Channels Active	OS_R		One color active per line.
Channel Sample Rate	30		MSPS per Channel (max)
ADC Sample Rate		30	MSPS (max)
f_{ADC}: f_{INCLK}	Internal 1x Clock Selected	1:01	f_{INCLK} = 30MHz (max)

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Table 3. Mode 1a Operating Details (continued)

	Detail
Output Sequencing	SH Signal → Color 1→Color 1→Color 1→Color 1→Color 1→ →SH Signal → Color 2→Color 2→Color 2→Color 2→Color 2→ →SH Signal → Color 3→Color 3→Color 3→Color 3→Color 3→ →SH Signal → Color 4→Color 4→Color 4→Color 4→Color 4→ →SH Signal → Color 5→Color 5→Color 5→Color 5→Color 5→ or SH Signal → Color 5→Color 5→Color 5→Color 5→Color 5→ →SH Signal → Color 4→Color 4→Color 4→Color 4→Color 4→ →SH Signal → Color 3→Color 3→Color 3→Color 3→Color 3→ →SH Signal → Color 2→Color 2→Color 2→Color 2→Color 2→ →SH Signal → Color 1→Color 1→Color 1→Color 1→Color 1→

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MODE 1B - ONE CHANNEL COLOR INPUT PER LINE/SEQUENTIAL LINE (INPUT) SAMPLING/THREE CHANNEL PROCESSING

In Mode 1b, the OS_R, OS_G, and OS_B inputs are sampled sequentially and processed through their respective channels. This mode allows an entire line of Red, Green, or Blue Pixels to be sampled before sequencing to the next input. This mode is useful with sensors that output whole lines of pixels of a single color. The order in which the channels are sampled is fully programmable. Actual switching from channel to channel is triggered by an SH pulse. The first SH pulse after this mode is set (or reset) sets up the first programmed channel for gain and offset and initiates sampling through that channel alone. The next SH pulse switches the active channel to the second channel indicated by the configuration registers. This sequencing with SH pulses continues to the third channel and then continuously loops through the channels.

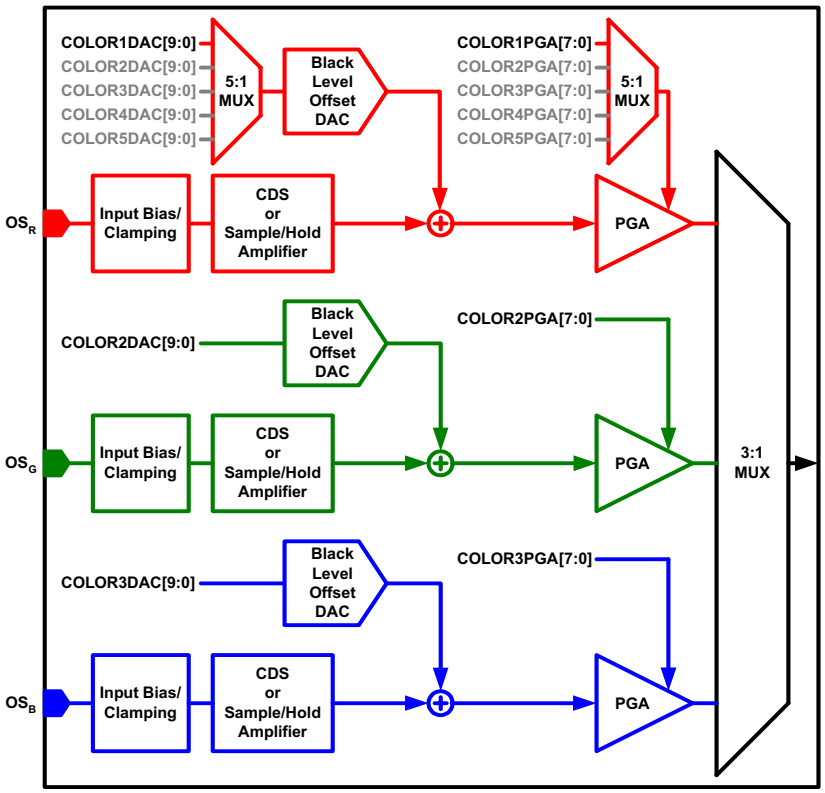

Figure 8. Mode 1b Signal Routing

Table 4. Mode 1b Operating Details

			Detail
Channels Active	OS_B or OS_G or OS_R		One channel active per line. Active channel is sequenced by SH pulse at start of new line.
Channel Sample Rate	30		MSPS per Channel (max)
ADC Sample Rate		30	MSPS (max)
f_{ADC}: f_{INCLK}	Internal 1x Clock Selected	1:01	f_{INCLK} = 30MHz (max)
Output Sequencing	SH Signal → R-R-R-R-R-R-R-R-R-R-R-R-R→ →SH Signal → G-G-G-G-G-G-G-G-G-G-G-G-G→ →SH Signal → B-B-B-B-B-B-B-B-B-B-B-B-B→ or SH Signal → B-B-B-B-B-B-B-B-B-B-B-B-B→ →SH Signal → G-G-G-G-G-G-G-G-G-G-G-G-G→ →SH Signal → R-R-R-R-R-R-R-R-R-R-R-R-R→		

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MODES OF OPERATION REGISTER SETTINGS TABLE

Table 5.

Operating Mode	Sampling Input(s)	Signal Path(s)	Output Sequencing Mode 3 and 2 = Pixel Seq Mode 1 = Color Line Seq	Main Config.	Main Config. Register 0							
				Reg. 3	Mode		Color		Order	Color Seq. Length		
				Bit [3]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Mode3-RGB Forward	OS_R||OS_G||OS_B	RGB	$Pixel_R$→$Pixel_G$→$Pixel_B$→	x	1	1	1	1	0	0	0	1
Mode3-RGB Reverse	OS_R||OS_G||OS_B	RGB	$Pixel_B$→$Pixel_G$→$Pixel_R$→	x	1	1	1	1	1	0	0	1
Mode2-RG Forw.	OS_R||OS_G	RG	$Pixel_R$→$Pixel_G$→	x	1	0	0	0	0	0	0	1
Mode2-RG Rev.	OS_R||OS_G	RG	$Pixel_G$→$Pixel_R$→	x	1	0	0	0	1	0	0	1
Mode2-GB Forw.	OS_G||OS_B	GB	$Pixel_G$→$Pixel_B$→	x	1	0	0	1	0	0	0	1
Mode2-GB Rev.	OS_G||OS_B	GB	$Pixel_B$→$Pixel_G$→	x	1	0	0	1	1	0	0	1
Mode2-RB Forw.	OS_R||OS_B	RB	$Pixel_R$→$Pixel_B$→	x	1	0	1	0	0	0	0	1
Mode2-RB Rev.	OS_R||OS_B	RB	$Pixel_B$→$Pixel_R$→	x	1	0	1	0	1	0	0	1
Mode1-R Mono	OS_R	R	Color Line Seq: 1→1→1→1→1→	x	0	1	0	0	0	0	0	1
Mode1a-R 2 Color For.	OS_R	R	Color Line Seq: 1→2→1→2→1→	0	0	1	0	0	0	0	1	0
Mode1a-R 2 Color Rev	OS_R	R	Color Line Seq: 2→1→2→1→2→	0	0	1	0	0	1	0	1	0
Mode1a-R 3 Color For.	OS_R	R	Color Line Seq: 1→2→3→1→2→	0	0	1	0	0	0	0	1	1
Mode1a-R 3 Color Rev	OS_R	R	Color Line Seq: 3→2→1→3→2→	0	0	1	0	0	1	0	1	1
Mode1a-R 4 Color For.	OS_R	R	Color Line Seq: 1→2→3→4→1→	0	0	1	0	0	0	1	0	0
Mode1a-R 4 Color Rev	OS_R	R	Color Line Seq: 4→3→2→1→4→	0	0	1	0	0	1	1	0	0
Mode1a-R 5 Color For.	OS_R	R	Color Line Seq: 1→2→3→4→5→	0	0	1	0	0	0	1	0	1
Mode1a-R 5 Color Rev	OS_R	R	Color Line Seq: 5→4→3→2→1→	0	0	1	0	0	1	1	0	1
Mode1a-G Mono	OS_G	G	Color Line Seq: 1→1→1→1→1→	1	0	1	0	1	0	0	0	1
Mode1a-B Mono	OS_B	B	Color Line Seq: 1→1→1→1→1→	1	0	1	1	0	0	0	0	1
Mode1b-RGB Forward	OS_R→OS_G→OS_B	RGB	$Line_R$→$Line_G$→$Line_B$→	1	0	0	1	1	0	x	x	x
Mode1b-RGB Reverse	OS_B→OS_G→OS_R	RGB	$Line_R$→$Line_G$→$Line_B$→	1	0	0	1	1	1	x	x	x

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Input Bias and Clamping

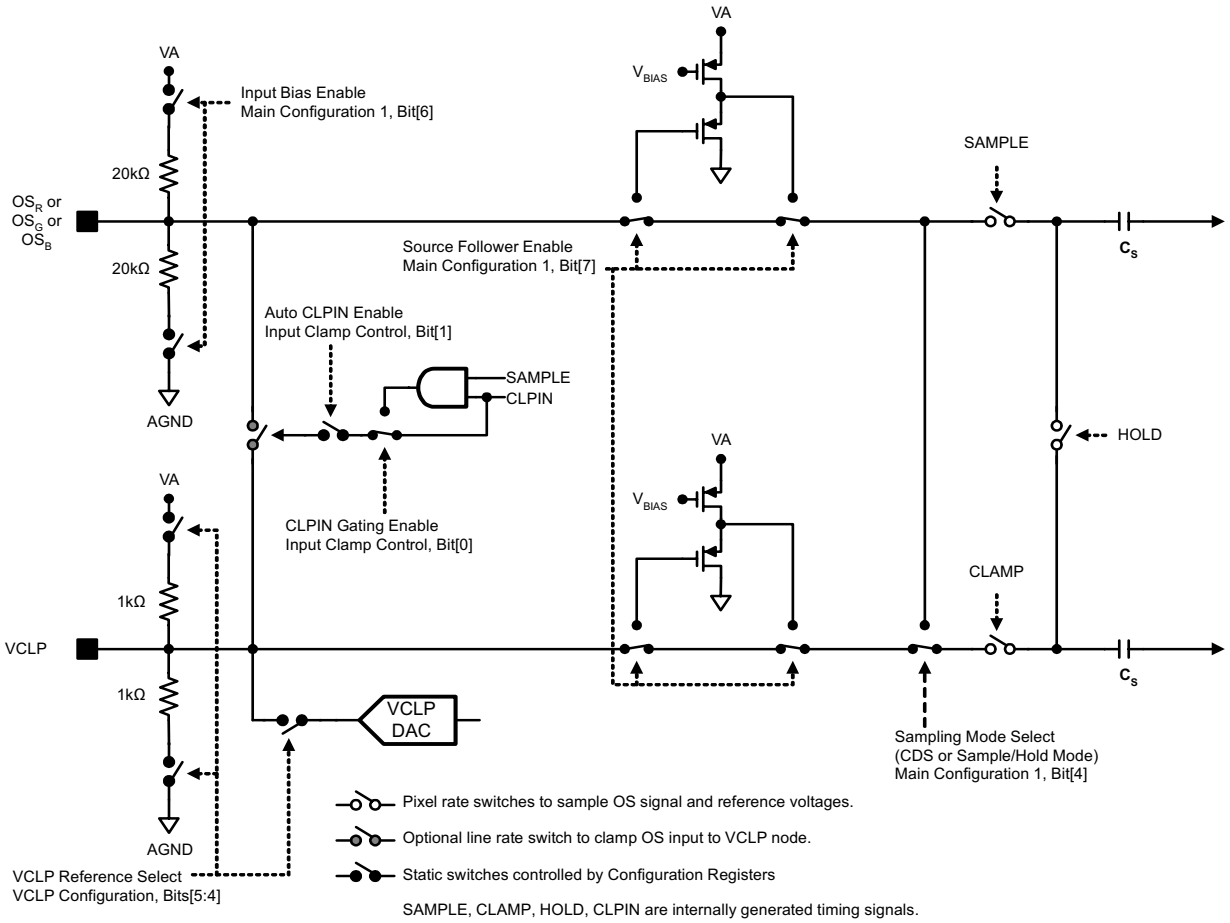

Figure 9. Input Bias and Clamping Diagram

The inputs to the LM98714 are typically AC coupled through a film capacitor and can be sampled in either Sample and Hold Mode (S/H Mode) or Correlated Double Sampling Mode (CDS Mode). In either mode, the DC bias point for the LM98714 side of the AC coupling capacitor is set using the circuit of Figure 9 which can be configured to operate in a variety of different modes.

A typical CCD waveform is shown in Figure 10. Also shown in Figure 10 is an internal signal “SAMPLE” which can be used to “gate” the CLPIN signal so that it only occurs during the “signal” portion of the CCD pixel waveform.

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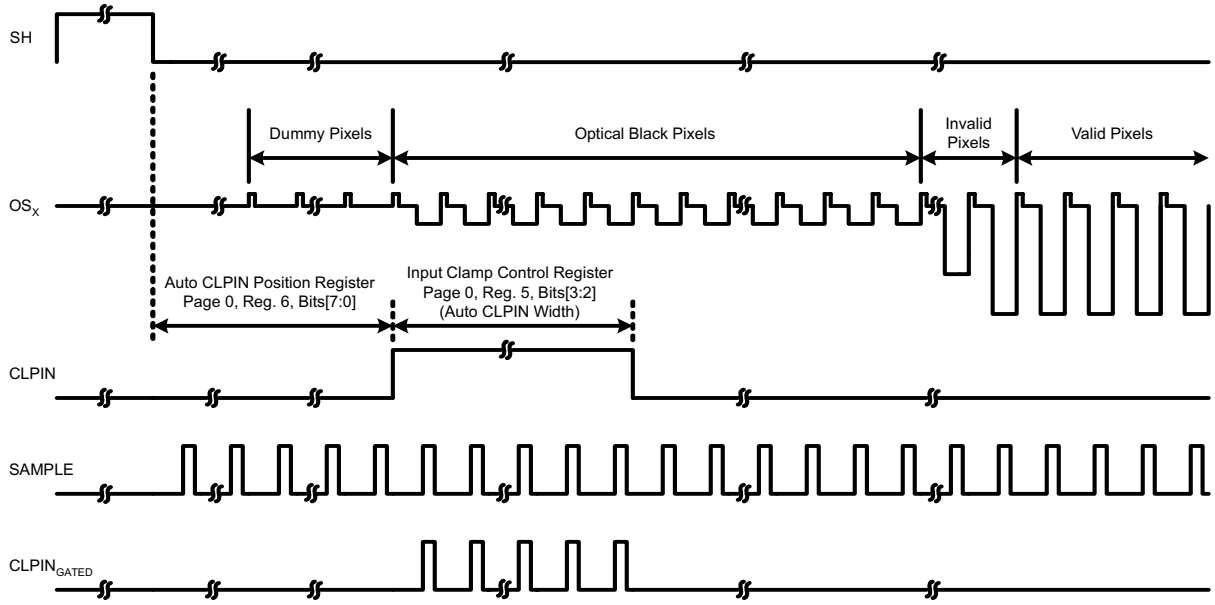

Figure 10. Typical CCD Waveform and LM98714 Input Clamp Signal (CLPIN)

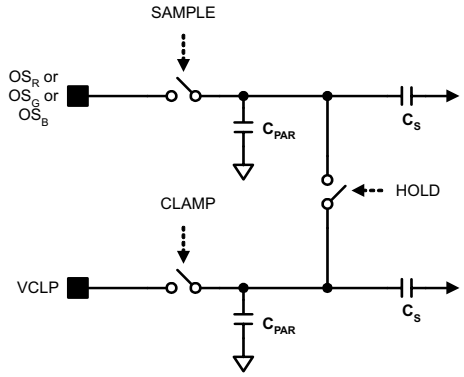

Figure 11. Sample and Hold Mode Simplified Input Diagram

Proper DC biasing of the CCD waveform in Sample and Hold mode is critical for realizing optimal operating conditions. In Sample/Hold mode, the Signal Level of the CCD waveform is compared to the DC voltage on the VCLP pin. In order to fully utilize the range of the input circuitry, it is desirable to cause the Black Level signal voltage to be as close to the VCLP voltage as possible, resulting in a near zero scale output for Black Level pixels.

In Sample/Hold Mode, the DC bias point of the input pin is typically set by actuating the input clamp switch (see Figure 9) during optical black pixels which connects the input pins to the VCLP pin DC voltage. The signal controlling this switch is an auto-generated pulse, CLPIN. CLPIN is generated with a programmable pixel delay with respect to SH and a programmable pixel width. These parameters are available through the serial interface control registers.

Actuating the input clamp will force the average value of the CCD waveform to be centered around the VCLP DC voltage. During Optical Black Pixels, the CCD output has roughly three components. The first component of the pixel is a “Reset Noise” peak followed by the Reset (or Pedestal) Level voltage, then finally the Black Level voltage signal. Taking the average of these signal components will result in a final “clamped” DC bias point that is close to the Black Level signal voltage.

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To provide a more precise DC bias point (i.e. a voltage closer to the Black Level voltage), the CLPIN pulse can be "gated" by the internally generated SAMPLE clock. This resulting $CLPIN_{GATED}$ signal is the logical "AND" of the SAMPLE and CLPIN signals as shown in Figure 10. By using the $CLPIN_{GATED}$ signal, the higher Reset Noise peak will not be included in the clamping period and only the average of the Reset Level and Black Level components of the CCD waveform will be centered around VCLP.

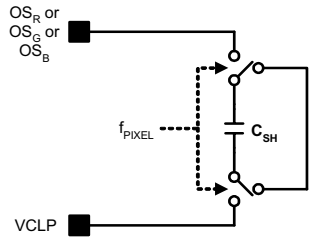

Figure 12. Equivalent Input Switched Capacitance S/H Mode

In Sample and Hold Mode, the impedance of the analog input pins is dominated by the switched capacitance of the CDS/Sample and Hold amplifier. The amplifier switched capacitance, shown as C_S in Figure 11, and internal parasitic capacitances can be estimated by a single capacitor switched between the analog input and the VCLP reference pin for Sample and Hold mode. During each pixel cycle, the modeled capacitor, C_{SH}, is charged to the OS_X-VCLP voltage then discharged. The average input current at the OS_X pin can be calculated knowing the input signal amplitude and the frequency of the pixel. If the application requires AC coupling of the CCD output to the LM98714 analog inputs, the Sample and Hold Mode input bias current may degrade the DC bias point of the coupling capacitor. To overcome this, Input Source Follower Buffers are available to isolate the larger Sample and Hold Mode input bias currents from the analog input pin (as discussed in the following section). As shown in CDS MODE, the input bias current is much lower for CDS mode, eliminating the need for the source follower buffers.

CDS MODE

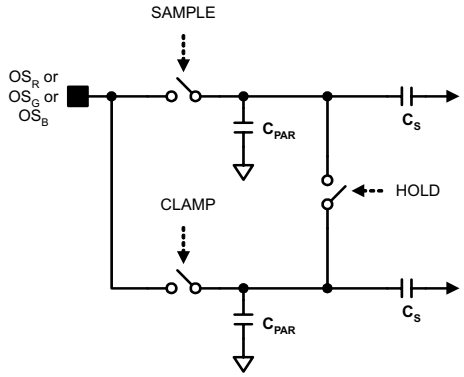

Figure 13. CDS Mode Simplified Input Diagram

Correlated Double Sampling mode does not require as precise a DC bias point as does Sample and Hold mode. This is due mainly to the nature of CDS itself, that is, the Video Signal voltage is referenced to the Reset Level voltage instead of the static DC VCLP voltage. The common mode voltage of these two points on the CCD waveform have little bearing on the resulting differential result. However, the DC bias point does need to be established to ensure the CCD waveform's common mode voltage is within rated operating ranges.

The CDS mode biasing can be performed in the same way as described in the Sample/Hold Mode Biasing section, or, an alternative method is available which precludes the need for a CLPIN pulse. Internal resistor dividers can be switched in across the OS_R, OS_G, and/or OS_B inputs to provide the DC bias voltage.

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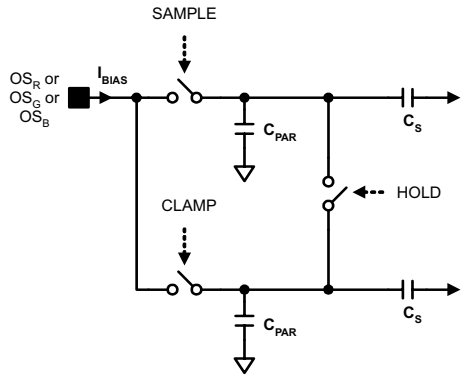

Figure 14. CDS Mode Input Bias Current

Unlike in Sample and Hold Mode, the input bias current in CDS Mode is relatively small. Due to the architecture of CDS switching, the average charge loss or gain on the input node is ideally zero over the duration of a pixel. This results in a much lower input bias current, whose main source is parasitic impedances and leakage currents. As a result of the lower input bias current in CDS Mode, maintaining the DC Bias point the input node over the length of a line will require a much smaller AC input coupling capacitor.

INPUT SOURCE FOLLOWER BUFFERS

The OS_R, OS_G, OS_B inputs each have an optional Source Follower Buffer which can be selected with Main Configuration Register 1, Bit[7]. These source followers provide a much higher impedance seen at the inputs. In some configurations, such as Sample and Hold Mode with AC coupled inputs, the DC bias point of the input nodes must remain as constant as possible over the entire length of the line to ensure a uniform comparison to reference level (VCLP in this case). The Source Followers effectively isolate the AC input coupling capacitor from the switched capacitor network internal to the LM98714's Sample and Hold/CDS Amplifier. This results in a greatly reduced charge loss or gain on the AC Input coupling capacitor over the length of a line, thereby preserving its DC bias point.

The Source Followers should only be used in the 1.2V input range (i.e. Main Configuration Register 2, Bit[4] = 1, CDS Gain = 2x). Using the Source Followers in the 2.4V (i.e. Main Configuration Register 2, Bit[4] = 0, CDS Gain = 1x). input range will result in a loss of performance (mainly linearity performance at the high and low ends of the input range).

VCLP DAC

The VCLP pin provides the reference level for incoming signals in Sample and Hold Mode. The pin's voltage can be set by one of three sources by writing to the VCLP Configuration Register on register page 0. By default, the VCLP pin voltage is established by an internal resistor divider which sets the voltage to VA/2. The resistor ladder can be disconnected and the pin driven externally by the application.

The most flexible method of setting the VCLP voltage is using the internal VCLP DAC buffer. The DAC is connected by setting the VCLP Configuration register Bit[5:4] to 2b'01. The DAC has a four bit "offset binary" format which is summarized in Table 6. The DAC output has an approximate swing of +/-1.2V.

Table 6. VCLP DAC Format

VCLP Configuration [3:0]	Typical VCLP Output
0	-Full Scale
0111	Mid Scale - LSB
1000	Mid Scale
1001	Mid Scale + 1 LSB
1111	+Full Scale

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PGA Gain Plots

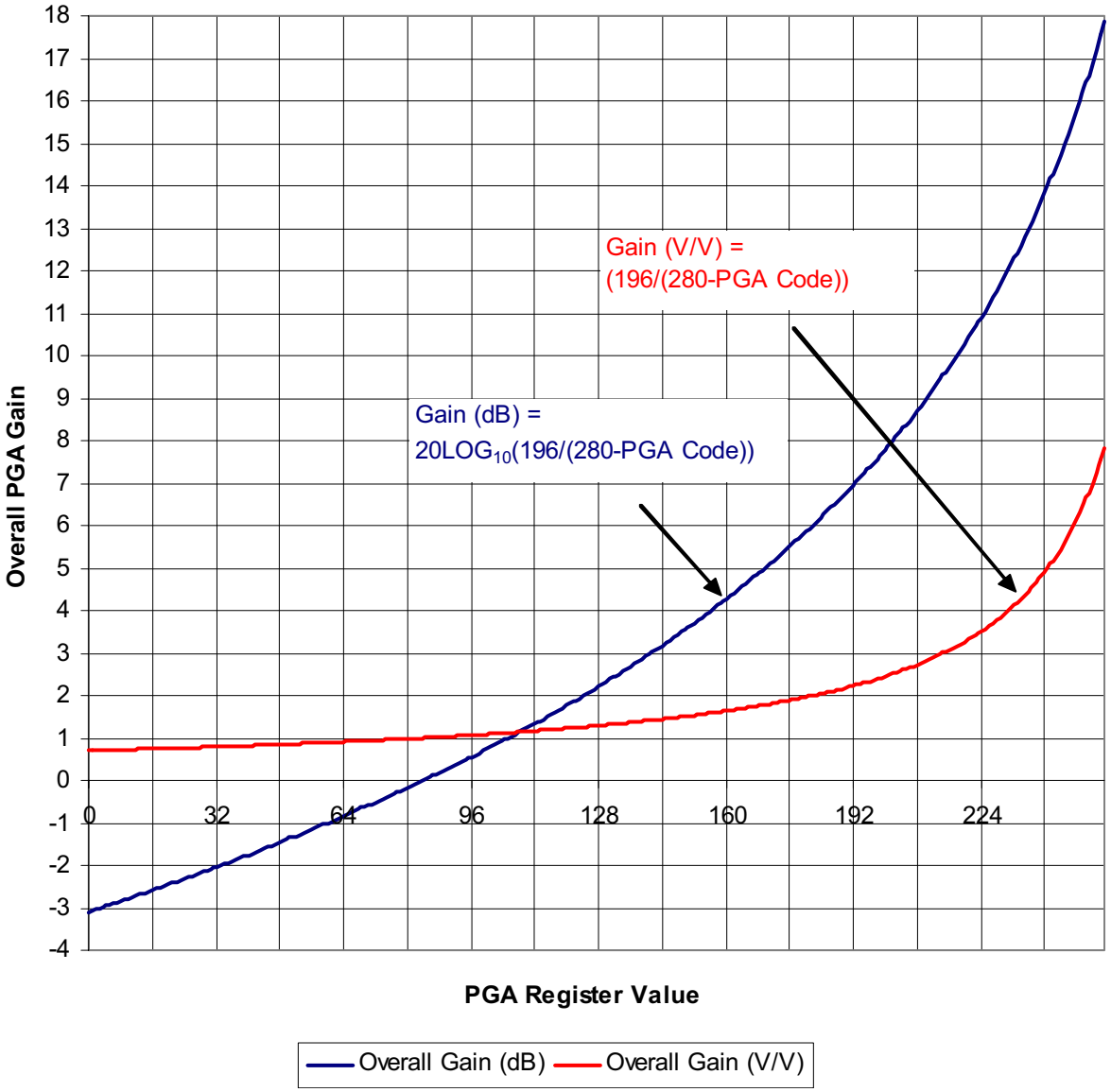

Figure 15. PGA Gain vs. PGA Gain Code

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Coarse Pixel Phase Alignment

Precise placement of the CCD video signal sampling point is a critical aspect in any typical imaging application. Many factors such as logic gate propagation delays and signal skew increase the difficulty in properly aligning the CCD pixel output signals with the AFE input sampling points. The LM98714 provides two powerful features to aid the system level designer in properly sampling the CCD video signal under a large range of conditions. The first feature, discussed in this section, is the Coarse Pixel Phase Alignment block. As the name implies, this block provides a very coarse range of timing adjustment to align the phase of the CCD Pixel output with the phase of the LM98714 sample circuit. The second feature, discussed on the Internal Sample Timing, is the block which is designed for fine tuning of the sampling points within the selected Coarse Pixel Alignment Phase. A small portion of a typical imaging application is shown in Figure 16.

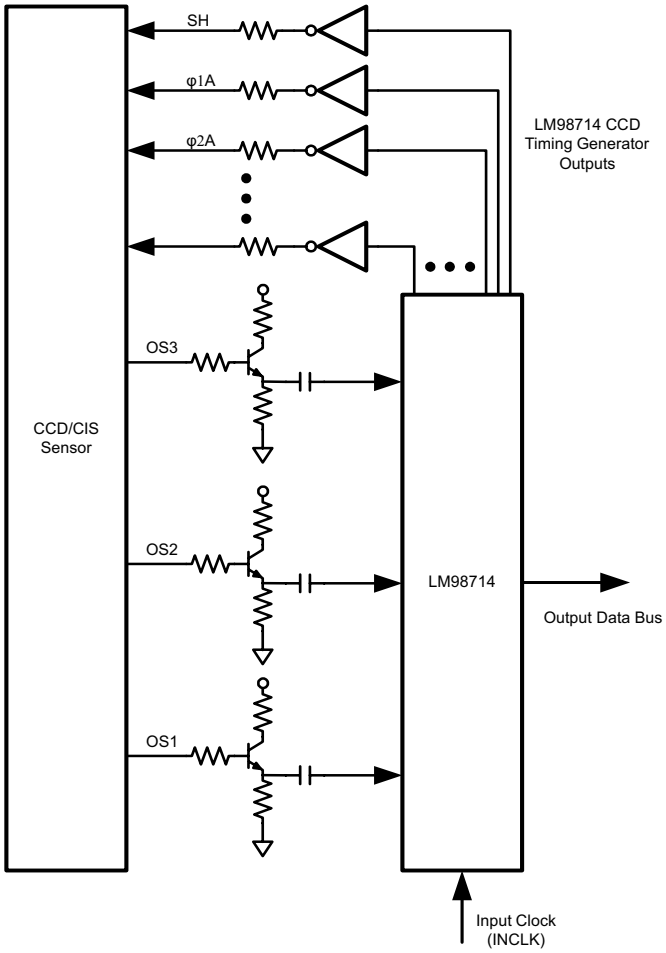

Figure 16. Typical AFE/CCD Interface

As shown in the diagram, the LM98714 provides the timing signals to drive the CCD using external logic gates to drive the high capacitance CCD clock pins. The pixels are shifted out of the CCD, thru the emitter follower buffers and received by the LM98714 inputs for processing.

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In an ideal application, depicted in Figure 17, the Pixel output signal would be in phase with the timing signals that drove the CCD. The LM98714 input sampling clocks (CLAMP and SAMPLE) are adjustable within a pixel period. By default, the pixel period (or pixel "phase") is defined to be in line with the input clock. As shown in the ideal case in Figure 17, CLAMP and SAMPLE can be properly adjusted to their ideal positions within the pixel phase, shown below at the stable region near the end of the pedestal and data phases.

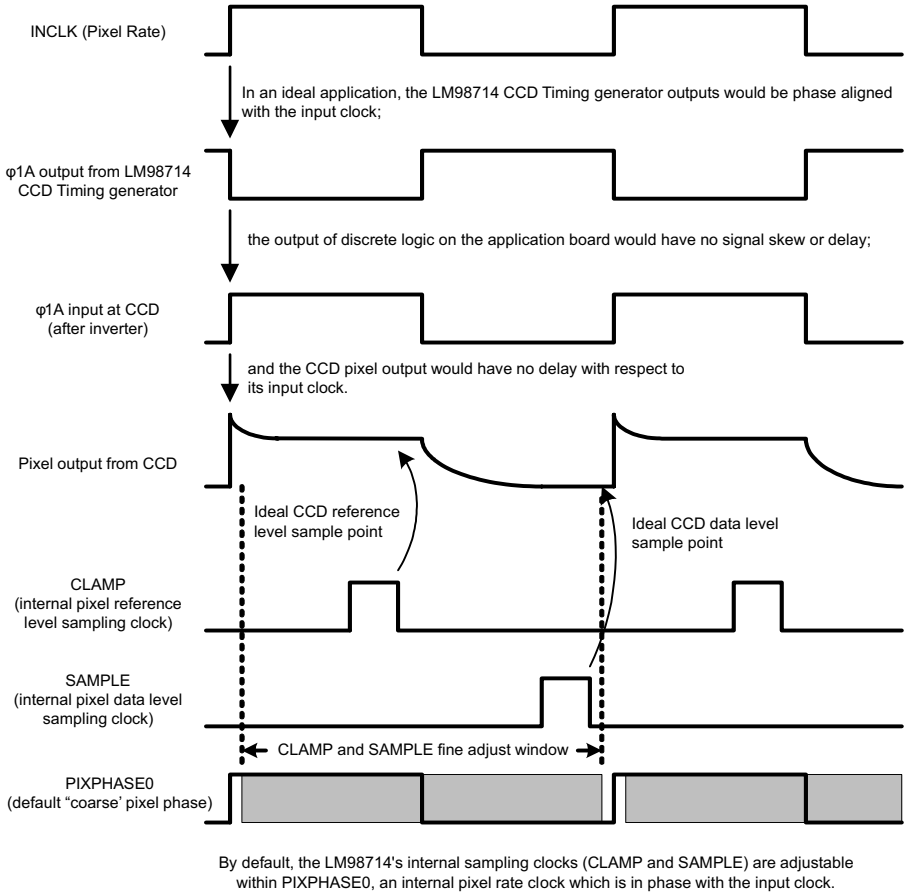

Figure 17. Clock Alignment in an Ideal Application

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In a real system however, propagation delays exist in all stages of the signal chain. These propagation delays will lead to a shift in the CCD Pixel outputs with respect to the LM98714 input clock. The phase shift of the CCD Pixel output, demonstrated in Figure 18, can lead to significant sample timing issues if not properly corrected.

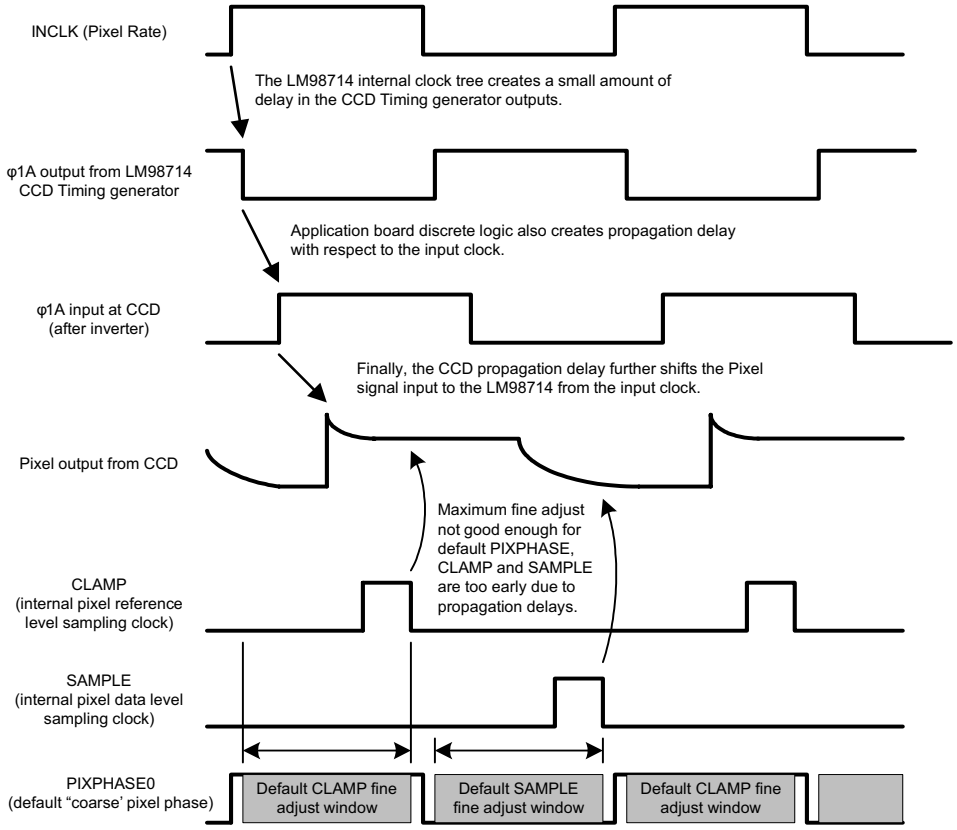

Figure 18. CCD Output Phase Shift in a Real Application

In the default mode, the LM98714 sampling is performed during a clock period whose phase is aligned with the input clock (ignoring any clock tree skew for the moment). The actual sampling clocks are adjustable within the clock period, as shown in Figure 18 (shown for CDS mode in the diagram) and further described in the Internal Sample Timing section. As shown in the diagram, the delay of the CCD Pixel output is shifted far enough that the fine CLAMP and SAMPLE clocks cannot be placed in a stable portion of the waveform. To remedy this situation, the LM98714's Coarse Pixel Phase Alignment feature allows the designer to shift the entire phase of the analog front end with respect to the input clock. This allows the designer to choose one of four sampling phases which best matches the delay in the external circuitry. Once the "Coarse Pixel Phase" has been chosen, the designer can then fine tune the sampling clocks using the fine adjustment (see Internal Sample Timing)

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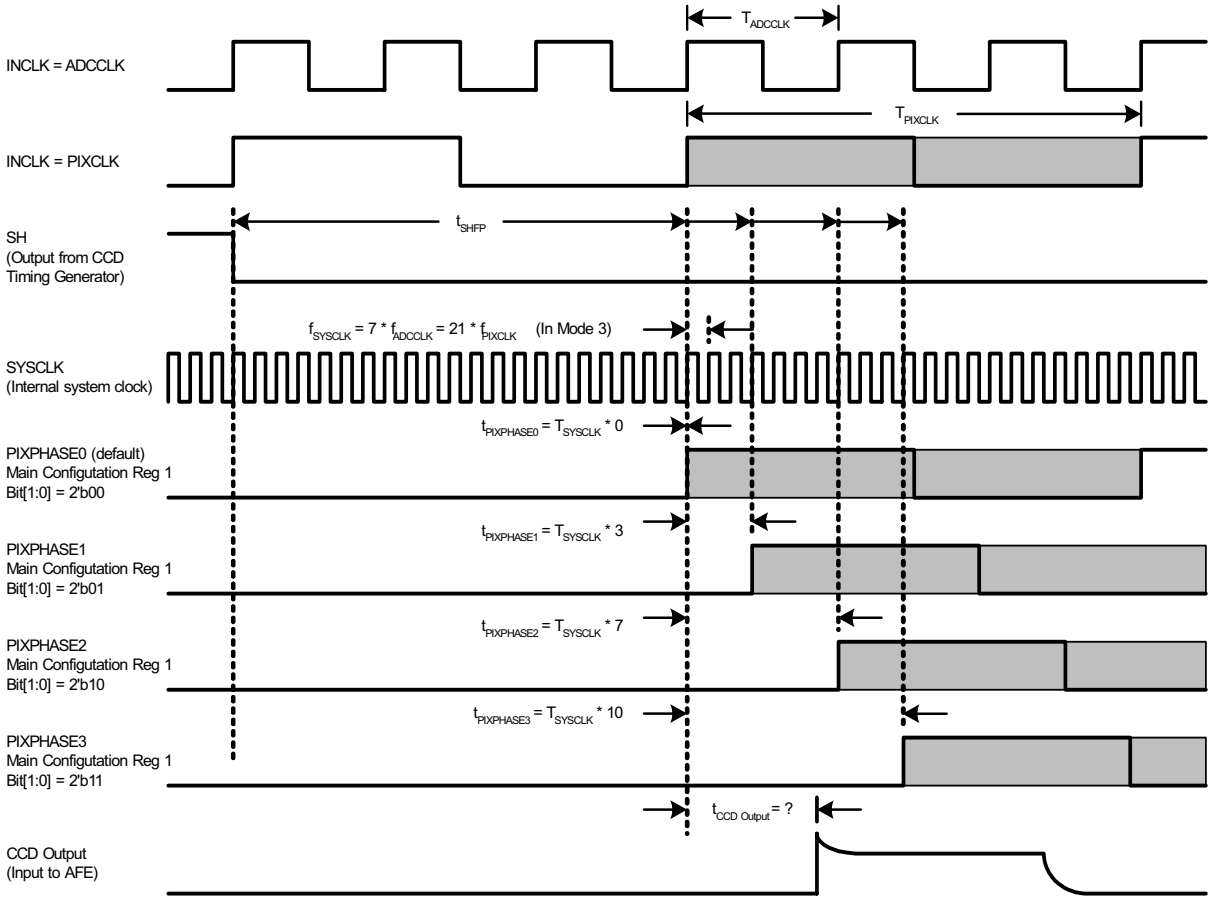
The four available Coarse Pixel Phases (PIXPHASE0 - PIXPHASE3) are depicted in Figure 19 (Mode 3), Figure 20 (Mode 2) and Figure 21 (Mode 1). Also shown in the diagrams are the external input clock (INCLK) and a typical CCD output delayed from the input clock.



The CCD output will usually have a measurable delay with respect to the input clock to the AFE. The AFE's internal sampling clocks are based on one of four PIXPHASE clocks. These PIXPHASE settings provide coarse adjustment of the internal AFE clock domain to best match the phase of the incoming CCD signal. Fine adjustment of the sampling clocks is discussed in another section. In this example above, PIXPHASE2 appears to provide the closest match for the incoming CCD signal.

Figure 19. Mode 3 Coarse Pixel Adjustment

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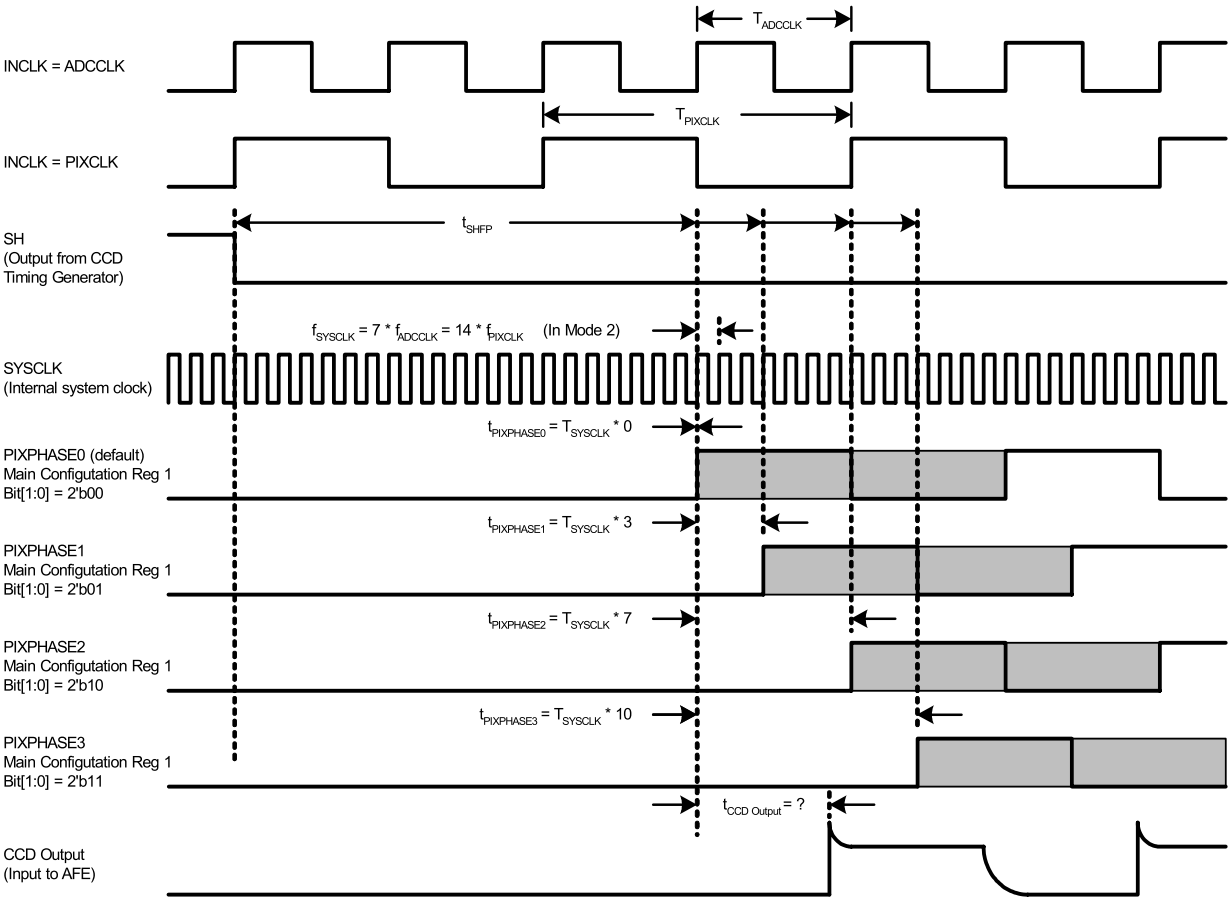
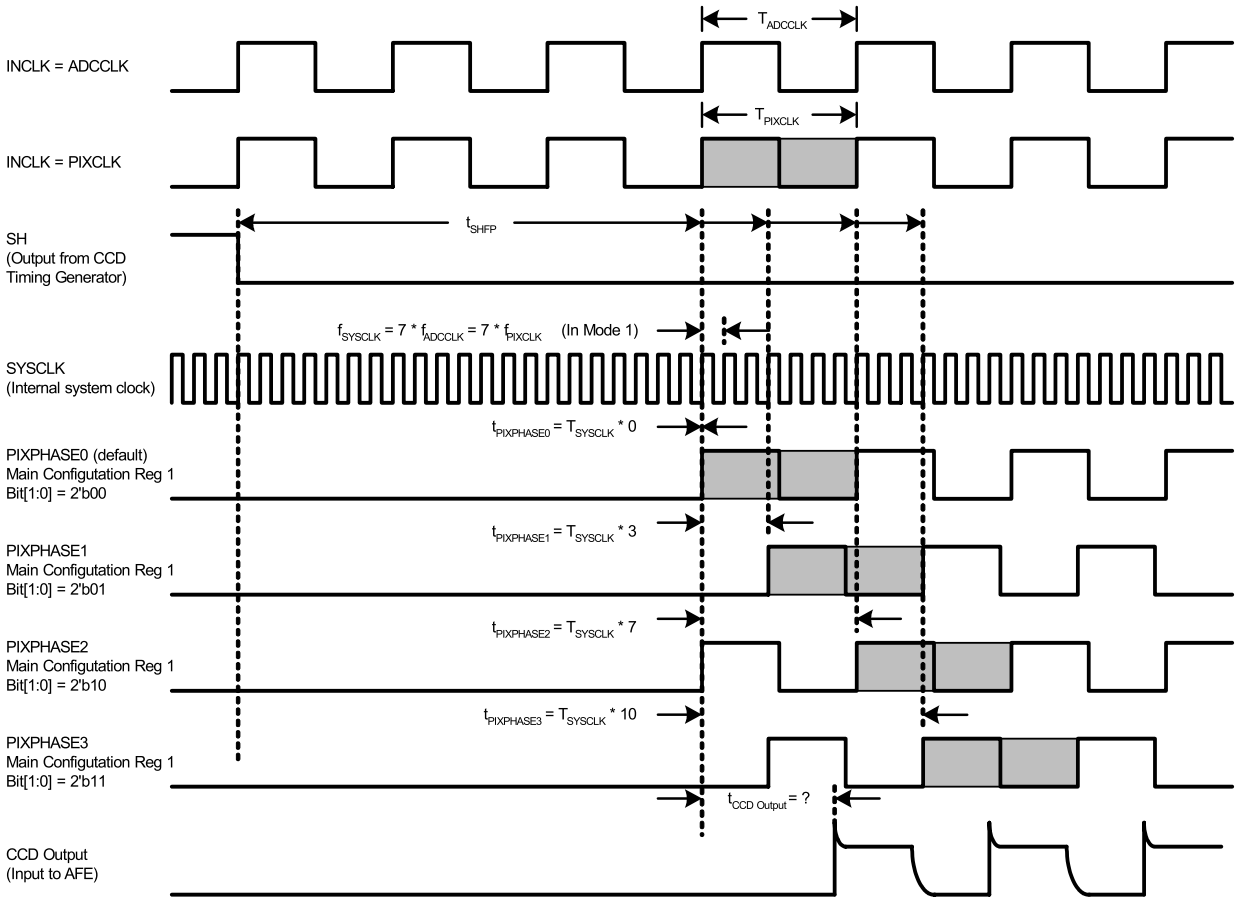


The CCD output will usually have a measurable delay with respect to the input clock to the AFE. The AFE's internal sampling clocks are based on one of four PIXPHASE clocks. These PIXPHASE settings provide coarse adjustment of the internal AFE clock domain to best match the phase of the incoming CCD signal. Fine adjustment of the sampling clocks is discussed in another section. In this example above, PIXPHASE2 appears to provide the closest match for the incoming CCD signal.

Figure 20. Mode 2 Coarse Pixel Phase Adjustment



The CCD output will usually have a measurable delay with respect to the input clock to the AFE. The AFE's internal sampling clocks are based on one of four PIXPHASE clocks. These PIXPHASE settings provide coarse adjustment of the internal AFE clock domain to best match the phase of the incoming CCD signal Fine adjustment of the sampling clocks is discussed in another section. In this example above, PIXPHASE2 appears to provide the closest match for the incoming CCD signal.

Figure 21. Mode 1 Coarse Pixel Phase Adjustment

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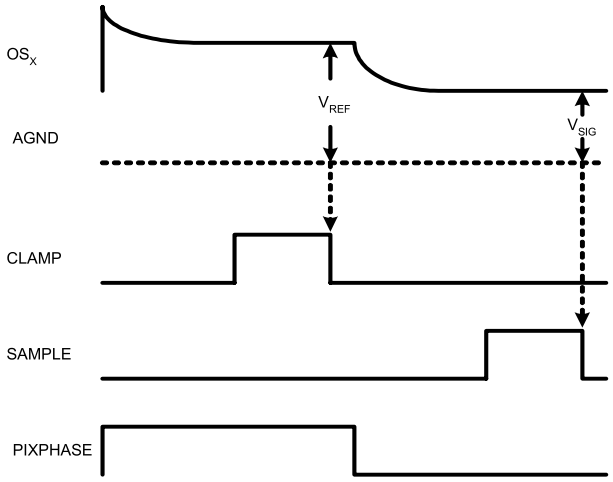
Internal Sample Timing

A typical CCD input signal is depicted in Figure 22 and Figure 23. Also shown are the internally generated SAMPLE and CLAMP pulses. These signals provide the sampling points of the input signal (OS_X). The timing of SAMPLE and CLAMP is derived from an internal system clock (SYSCLK).

The pixel's reference level input (depicted as V_{REF}) is captured by the falling edge of the CLAMP pulse. In Sample/Hold Mode the V_{REF} input is a sample of the VCLP DC voltage. In CDS Mode the CLAMP pulse samples the pedestal Level of the CCD output waveform.

The pixel's signal level input (depicted as V_{SIG}) is captured by the SAMPLE pulse. In either Sample/Hold or CDS Mode, the V_{SIG} input is the signal level of the CCD output waveform.

The LM98714 provides fine adjustment of the CLAMP and SAMPLE pulse placement within the pixel period. This allows the user to program the optimum location of the CLAMP and SAMPLE falling edges. In CDS mode, both CLAMP and SAMPLE are independently adjustable for each channel in use. In Sample/Hold mode, CLAMP is coincident with SAMPLE by default, but is also independently adjustable. The available fine tuning locations for CLAMP and SAMPLE are shown in Figure 24 through Figure 29 for each sampling mode (CDS or S/H) and channel mode (3, 2, or 1 Channel).

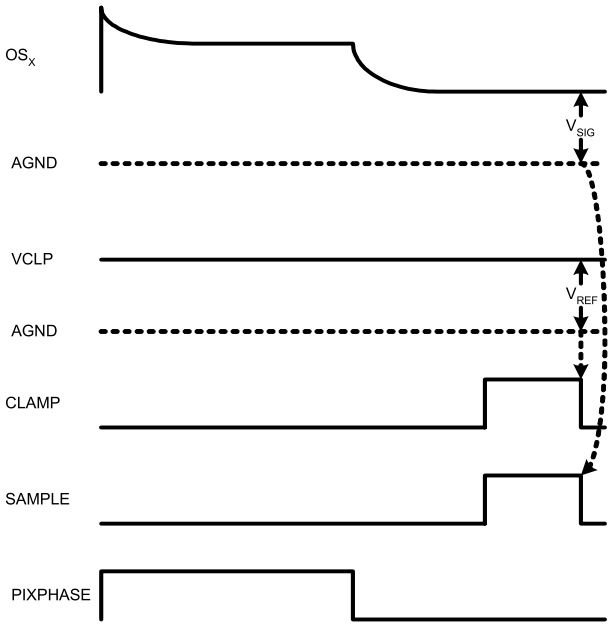


CLAMP and SAMPLE are the internal sampling clocks for the input CDS amplifier. CLAMP and SAMPLE are adjustable within the selected PIXPHASE setting.

In CDS mode, CLAMP falling edge captures the pixel reference level (V_{REF}).
In CDS mode, SAMPLE falling edge captures the pixel signal level (V_{SIG}).

PIXPHASE is 1 of 4 internal reference clocks used to estimate the phase of the incoming pixel. Once the coarse estimation of the pixel location is chosen via PIXPHASE, the CLAMP and SAMPLE clocks can be fine tuned within PIXPHASE to their optimum location.

Figure 22. Pixel Sampling in CDS Mode



CLAMP and SAMPLE are the internal sampling clocks for the input CDS amplifier. CLAMP and SAMPLE are adjustable within the selected PIXPHASE setting.

In S/H mode, CLAMP falling edge captures the VCLP pin voltage as the pixel reference voltage (V_{REF}).
In S/H mode, SAMPLE falling edge captures the pixel signal level (V_{SIG}).

PIXPHASE is 1 of 4 internal reference clocks used to estimate the phase of the incoming pixel. Once the coarse estimation of the pixel location is chosen via PIXPHASE, the CLAMP and SAMPLE clocks can be fine tuned within PIXPHASE to their optimum location.

Figure 23. Pixel Sampling in S/H Mode

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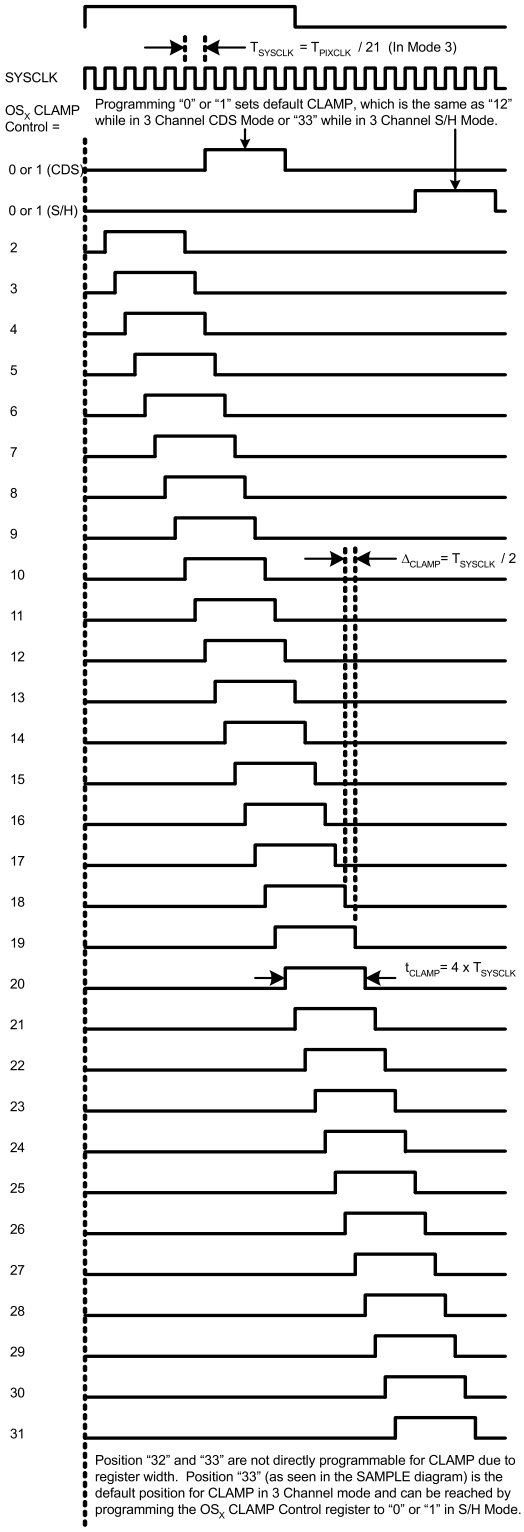

Figure 24. 3 Channel (Mode 3) CLAMP Timing

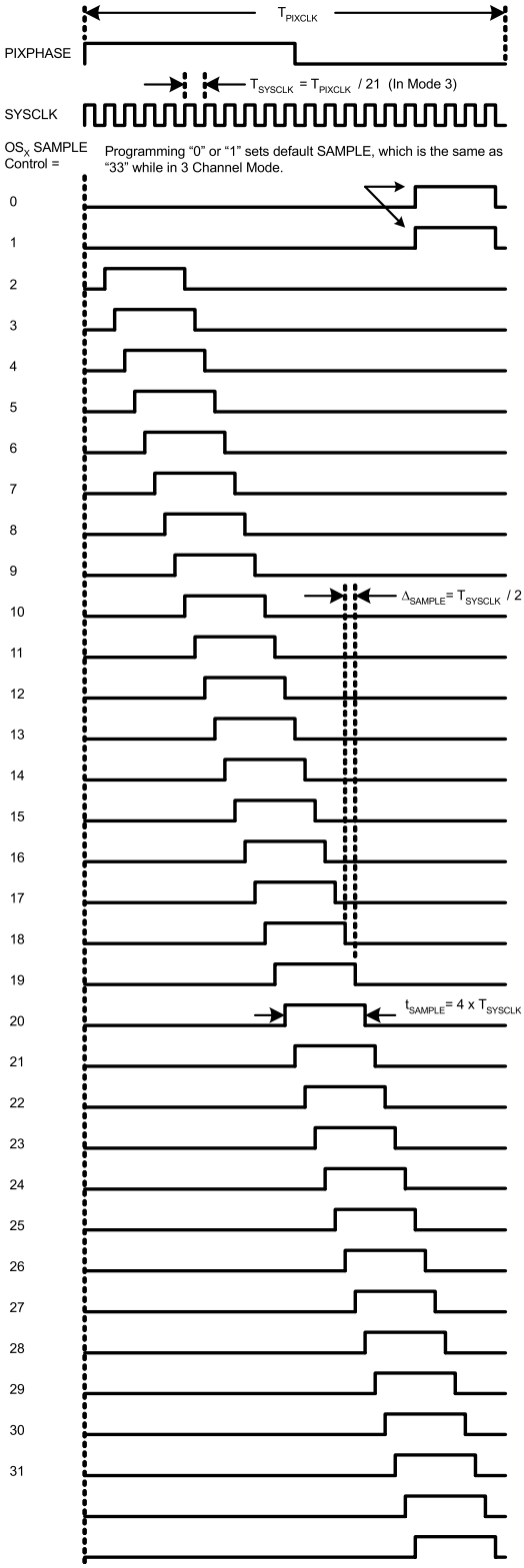

Figure 25. 3 Channel (Mode 3) SAMPLE Timing

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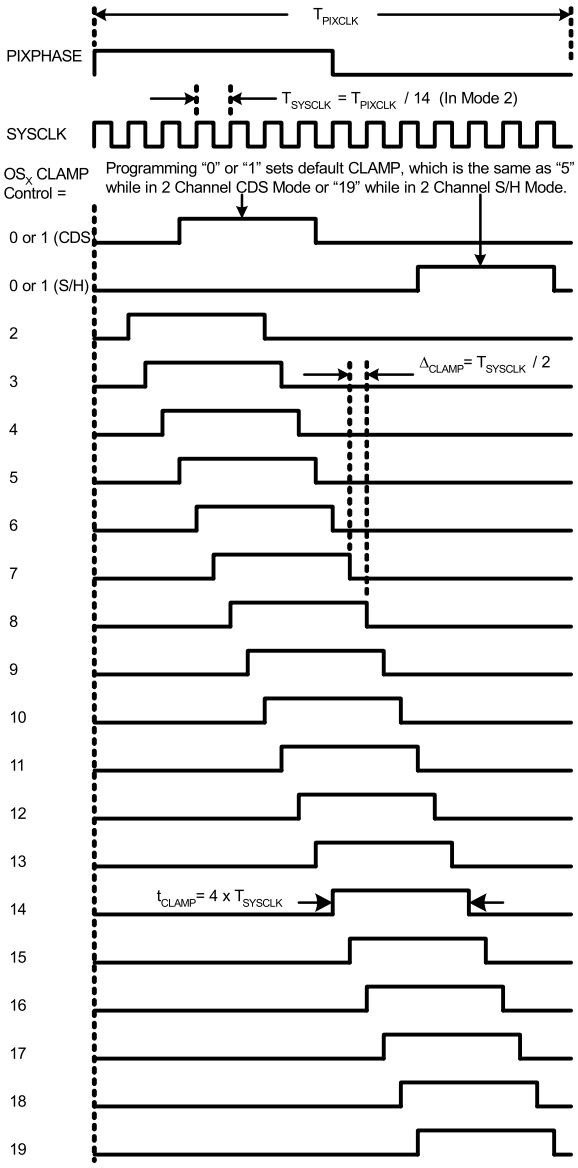

Figure 26. 2 Channel (Mode 2) CLAMP Timing

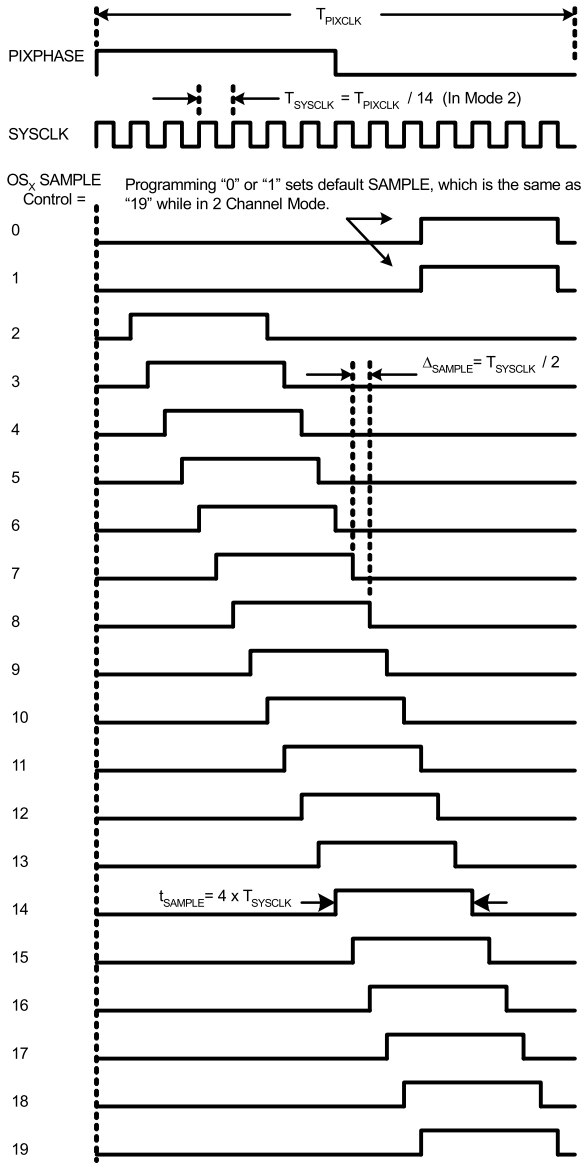

Figure 27. 2 Channel (Mode 2) SAMPLE Timing

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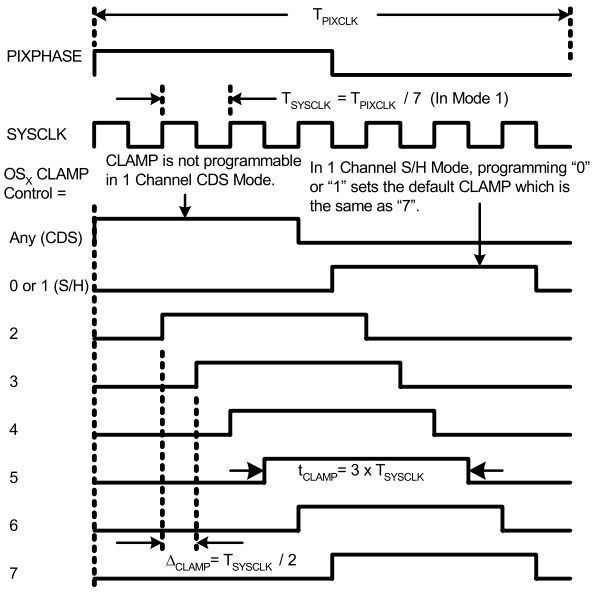

Figure 28. 1 Channel (Mode 1) CLAMP Timing

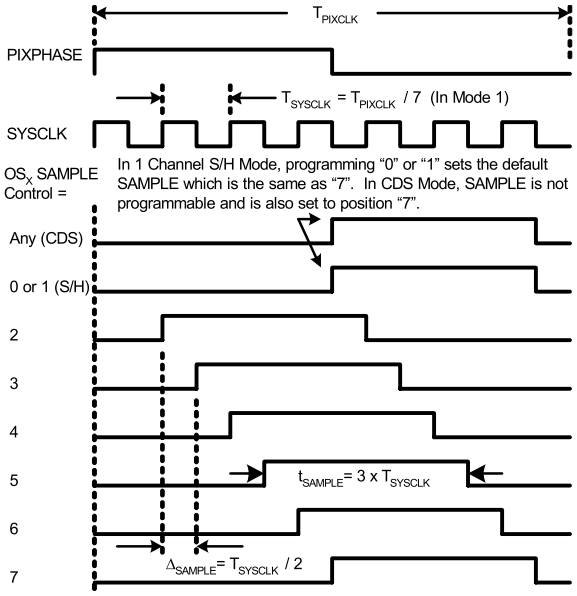

Figure 29. 1 Channel (Mode 1) SAMPLE Timing

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Automatic Black Level Correction Loop

CCD signal processors require a reference level for the proper handling of input signals; this reference level is commonly referred to as the black level. The LM98714 provides an Automatic Black Level Correction Loop as shown in Figure 30. The timing for this function is shown in Figure 31. The loop can be disabled and the Black Level Offset DAC registers programmed manually if desired.

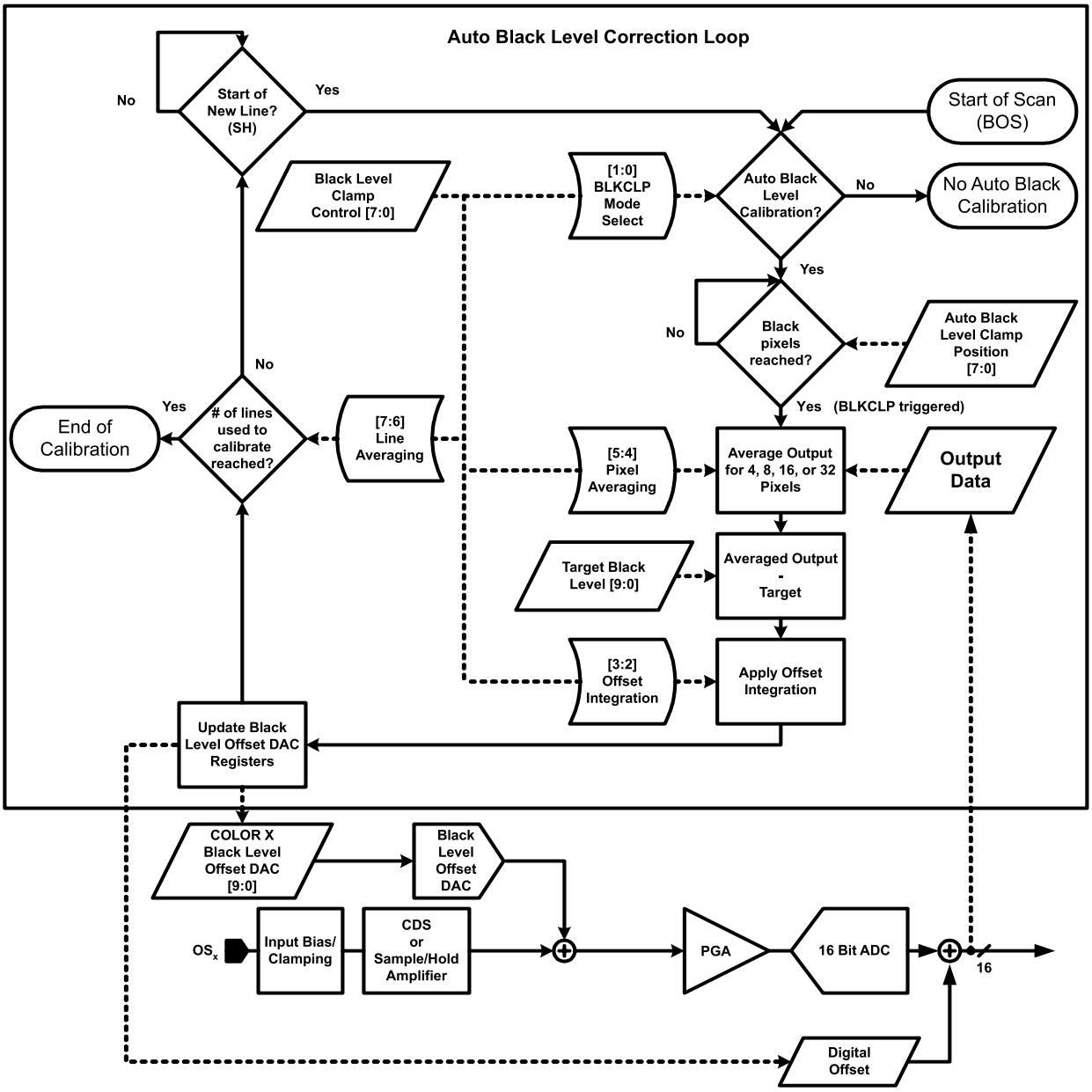


Figure 30. Black Level Correction Loop

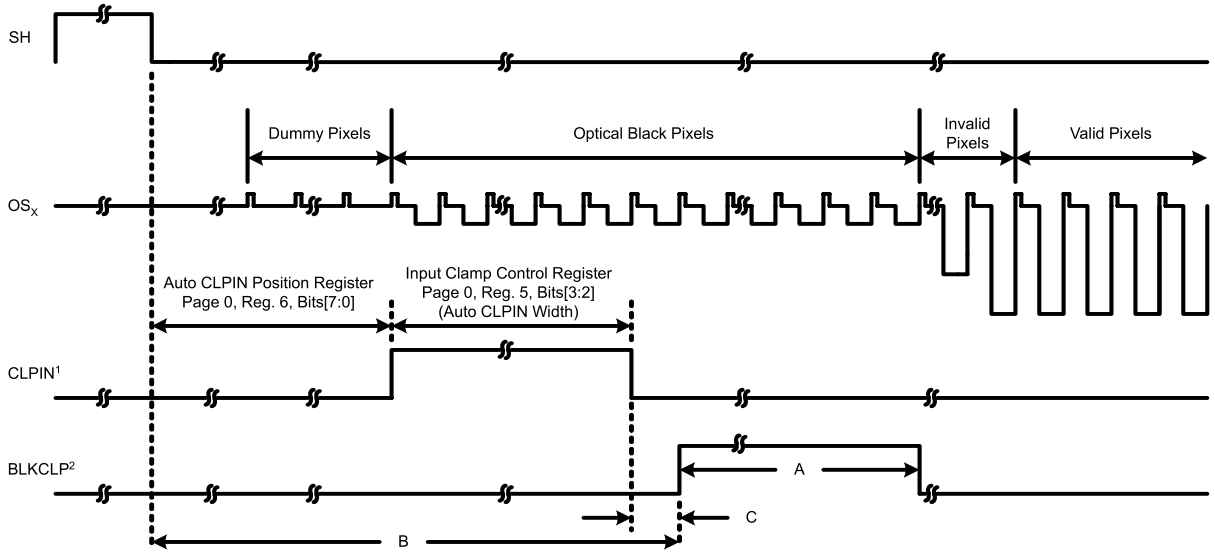
The loop is intended to be used prior to scanning the page or during the first several lines at the beginning of a scan. The loop calibrates the channel offset such that the ADC outputs the desired code for Optical Black Pixels. In automatic mode, the pixels used to calibrate the offset should be Optical Black pixels represented by the internal “BLKCLP” pulse in Figure 31.

BLACK LEVEL OFFSET DAC

The offset level registers store the DAC value required to meet the respective channel’s black level output. While using the Auto Black Level Correction Loop, the DAC registers are re-written as required every line the loop is enabled.

BLACK LEVEL CLAMP (BLKCLP)

The BLKCLP pulse can be synchronized by either the falling edge of the SH pulse or the CLPIN pulse (both shown in Figure 31). The automatic BLKCLP pulse will begin “n” number of pixel periods after the falling edge of the reference pulse where “n” is the Auto Black Level Clamp Position register. The reference point is programmed by the BLKCLP Mode Select Bits[1:0] within the Black Level Clamp Control register. The BLKCLP pulse should not be programmed coincident to the CLPIN pulse (if the CLPIN pulse is being used).



1. CLPIN is an optional input clamping signal. If CLPIN is used, the Black level Calibration Loop should be triggered after CLPIN returns low during Optical Black Pixels.
2. BLKCLP represents the time during a line where the Black level Calibration Loop is active. BLKCLP can be programmed to begin relative to the falling edge of SH or the falling edge of CLPIN (if CLPIN is being used).

A = Number of Optical Black Pixels the Black Level Calibration Loop averages per line. It is configured by the Black Level Clamp Control Register (Page 0, Reg. 8, Bits[5:4]).

B = Black Level Clamp Position with delay from SH. Auto Black Level Clamp Position (Page 0, Reg. 9) and BLKCLP Mode Select (Page 0, Reg. 8, Bits[1:0]) = 01b

C = Black Level Clamp Position with delay from CLPIN. Auto Black Level Clamp Position (Page 0, Reg. 9) and BLKCLP Mode Select (Page 0, Reg. 8, Bits[1:0]) = 10b

Figure 31. Black Level Correction Timing

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PIXEL AVERAGING

In order to obtain a snapshot of the current value for black (for comparison with the desired level of black) the ADC output is sampled upon activation of BLKCLP. Since a single optical black pixel is unlikely to be an accurate representation of the black level, a number of adjacent pixels are averaged. The number of pixels sampled is programmable by the Pixel Averaging Bit[5:4] within the Black Level Clamp Control register. The ability to select the number of pixels to be averaged (4, 8, 16, or 32 per line) provides greater flexibility allowing the LM98714 to be used with different CCDs having differing number of black pixels.

TARGET BLACK LEVEL

The Target Black Level registers define a 10-bit word that specifies an ADC output (on the 12 bit level) corresponding to the desired optical black output code (ignoring the four LSBs of the 16 Bit ADC output). In other words, one Target Black Level LSB corresponds to sixteen ADC LSBs. Assertion of the BLKCLP signal activates the digital black clamp loop and the black level is steered toward the value stored in the output black level register. The digital black clamp loop is only limited in it's range by the offset DAC's range.

Once the correct number of pixels have been averaged, the value is subtracted from the Target Black Level and an error value is produced.

OFFSET INTEGRATION

Each time the BLKCLP signal is activated, the average ADC output of several black pixels is compared to the Target Black Level producing an error value. This error value is not directly added (or subtracted) to the Black Level Offset register, rather, the value applied is a programmable fraction of this error. This has the effect of slowing down the offset convergence resulting in a calculation for offset that is less susceptible to noise. The scaling factor is stored in the Offset integration Bits[3:2] of the Black Level Clamp Control register. The scaling values are divided-by-8, 16, 32, or 64. Divide-by-8 provides the quickest convergence of the loop (for use when the number of lines available for calibration is limited) and Divide-by-64 the longest (for use when using an large number of lines to converge).

LINE AVERAGING

The Auto Black level Correction Loop can be run for 15 lines, 31 lines, 63 lines, or infinite (every line). The Line Averaging Bits[7:6] found in the lack Level Clamp Control register set the number of lines that the loop will run after the Start of Scan. The recommended use of the Auto Black Level Correction Loop is in a calibration period prior to moving the sensor down the page or during the first several lines of the page. By experimenting with the Line Averaging and Offset Integration bits with no sensor illumination (black pixels), the proper settings for the Auto Black Level Correction Loop are determined when the ADC output converges to the Target Black Level value. If the loop converges with the 15, 31, or 63 line setting, the loop can remain enabled. The loop does not update the Black Level Offset DAC once the number of lines since "Start of Scan" has passed. If the loop requires more than 63 lines to converge (i.e. requires Line Averaging = infinite), it is recommended to disable the loop after convergence has been reached. In the "infinite" setting, the loop will continuously update the Black Level Offset registers as long as the loop is enabled throughout the entire scan.

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Internal Timing Generation

A flexible internal timing generator is included to provide clocking signals to CCD and CIS sensors. A block diagram of the CCD Timing Generator is shown in Figure 32.

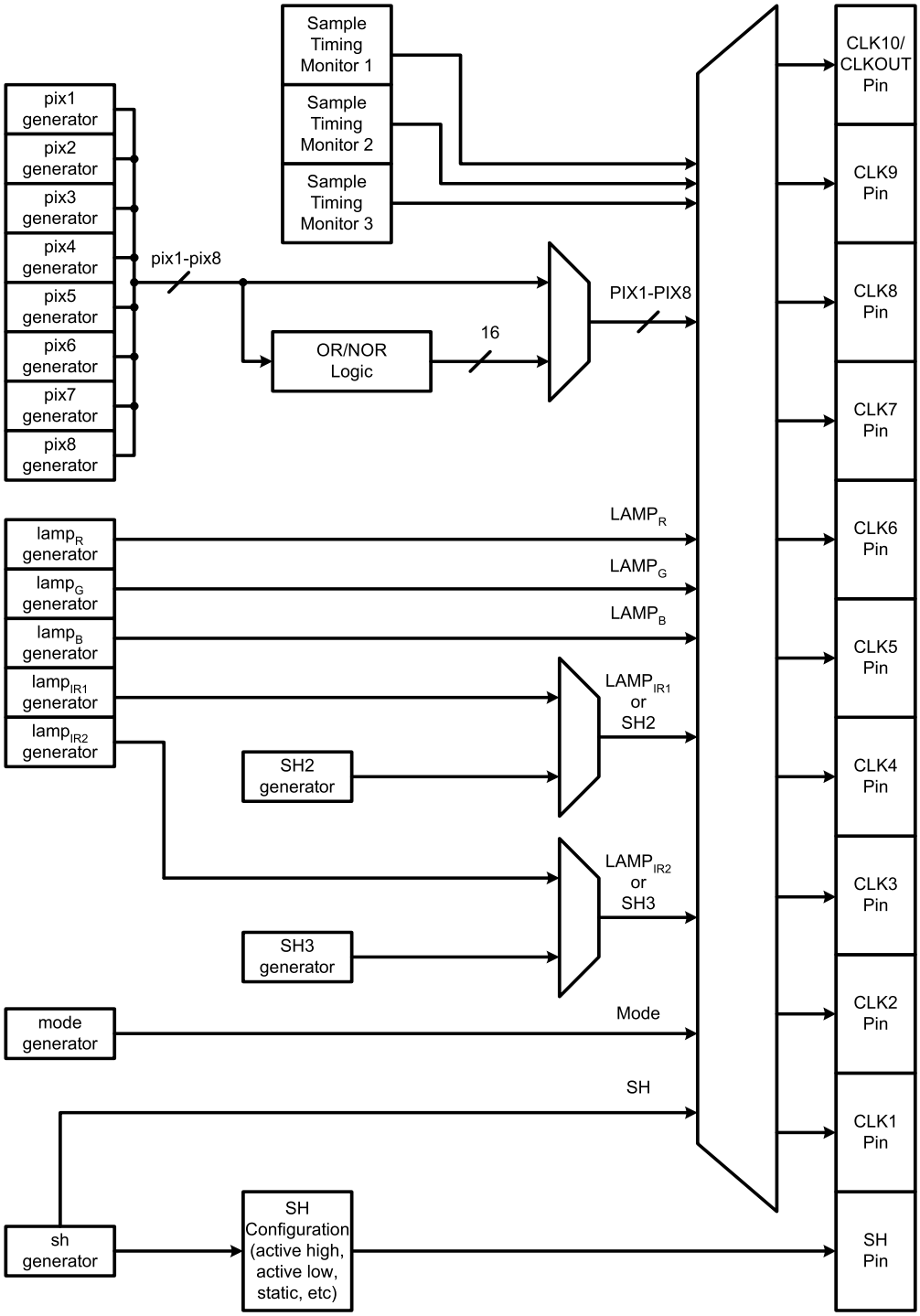

Figure 32. CCD Timing Generator Block Diagram

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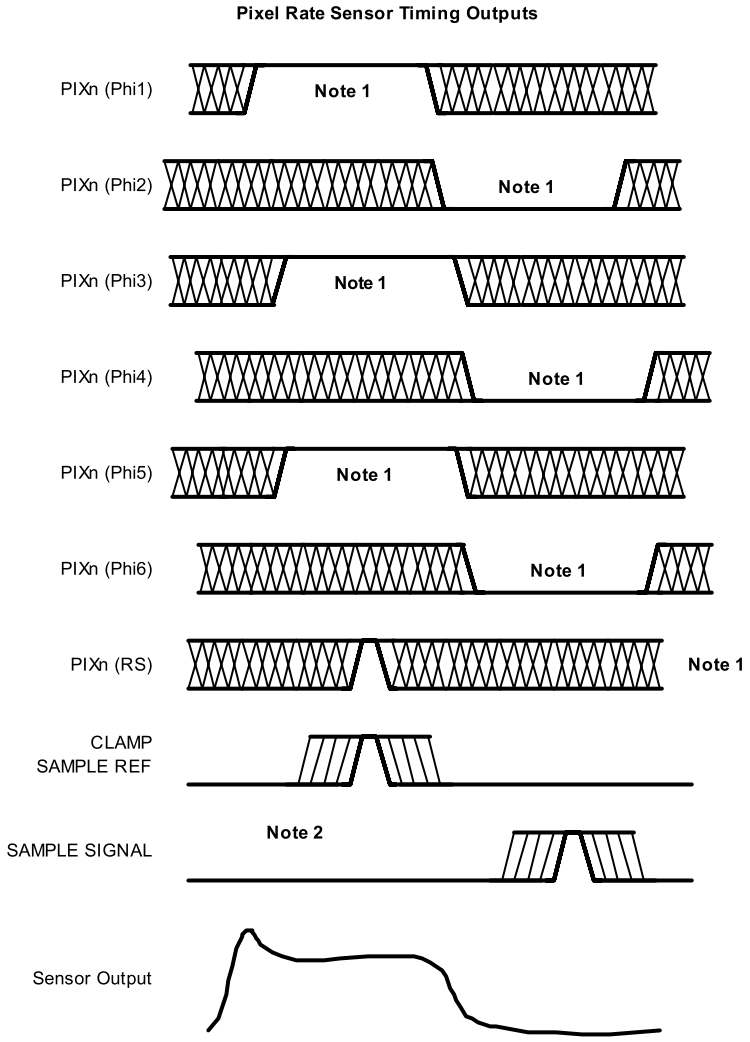
Examples of the various operating modes and settings are shown following. The detailed pixel timing is somewhat dependent on the operating modes of the AFE circuitry regarding the number of adjustment points for the on and off points of the different timing outputs.

NOTE

In addition to the timing adjustments shown, the polarity of all sensor clock signals can be adjusted by register control.



Note 1: PIXn rising and falling edges can be independently adjusted to any available point within the pixel period. Duration, duty cycle and position can all be adjusted as required. To ensure 50% duty cycle is possible, the internal clock system provides an even number of edges in all modes.
Note 2: CLAMP and SAMPLE signals have several available positions (see detailed AFE timing mode diagrams), but duration is fixed by design.
Note 3: The number of available edges for timing adjustments is dependent on the AFE operating mode.

Figure 33. Sensor Timing Control - Pixel Details - 1 Pixel per Phi

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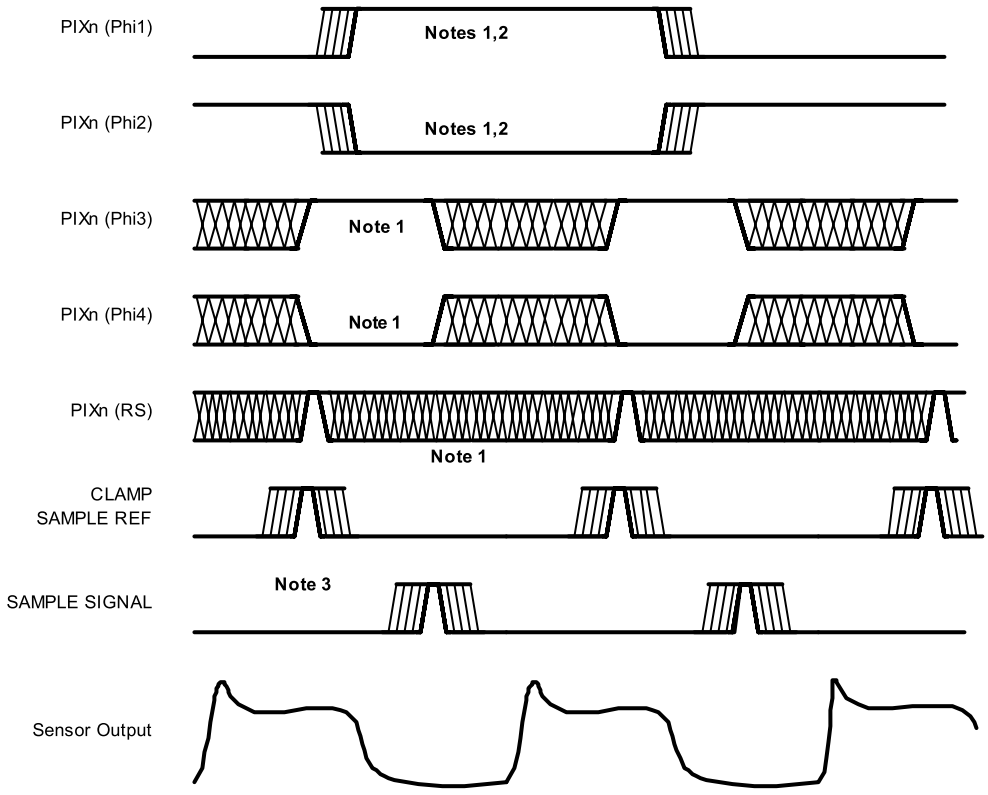

Note 1: PIXn rising and falling edges can be independently adjusted to any available point within the 2 pixel period. Duration, duty cycle and position can all be adjusted as required. To ensure 50% duty cycle is possible, the internal clock system provides an even number of edges in all modes.
Note 2: Each PIXn can be adjusted to have a frequency equal to or 1/2 that of the pixel frequency. In that case, rising and falling edges can be adjusted to any available edge within the 2 pixel interval.
Note 3: CLAMP and SAMPLE signals have several available positions (see detailed AFE timing mode diagrams), but duration is fixed by design.
Note 4: The number of available edges for timing adjustments is dependent on the AFE operating mode.

Figure 34. Sensor Timing Control - Pixel Details - 2 Pixels per Phi

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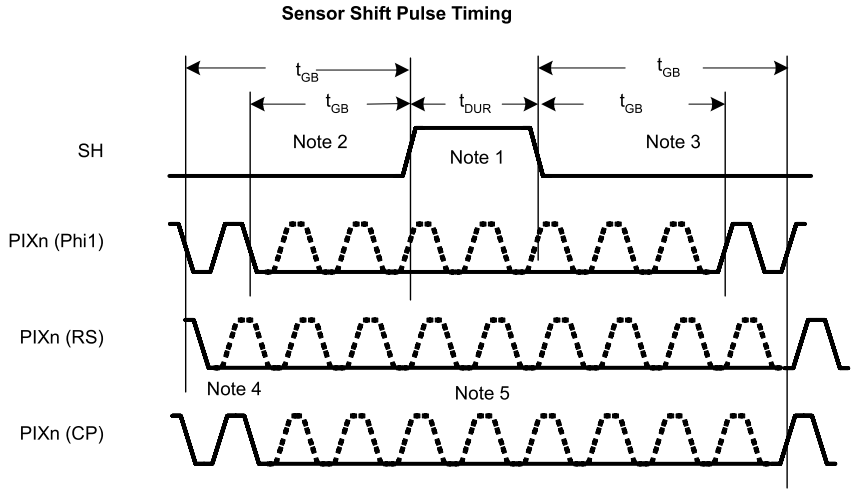
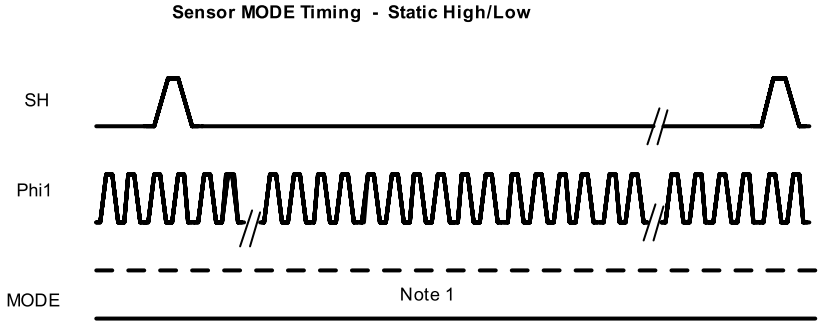


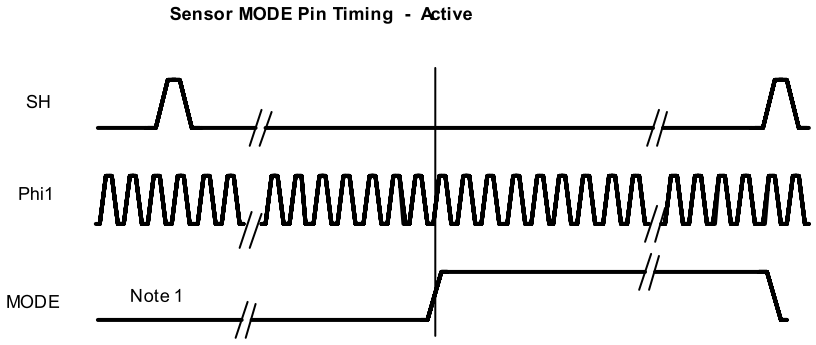
Note 1: SH duration can be adjusted.
Note 2: Guardband from end of PIX timing signal to start of SH can be selected individually for each PIX timing signal. Range of adjustment is 0 to 255 pixel periods.
Note 3: Guardband from end of SH to start of PIX timing signal can be selected individually for each PIX signal. Range of adjustment is 0 to 255 pixel periods.
Note 4: The detailed timing of each PIX signal is adjustable to any available PLL clock edge within the pixel period. Refer to PIX timing details.
Note 5: Each PIX signal can be selected as Inactive or Active during the SH pulse interval.
*RS and CP must be inactive during SH when using Toshiba CCD sensors.

Figure 35. Sensor Timing SH Pulse Details



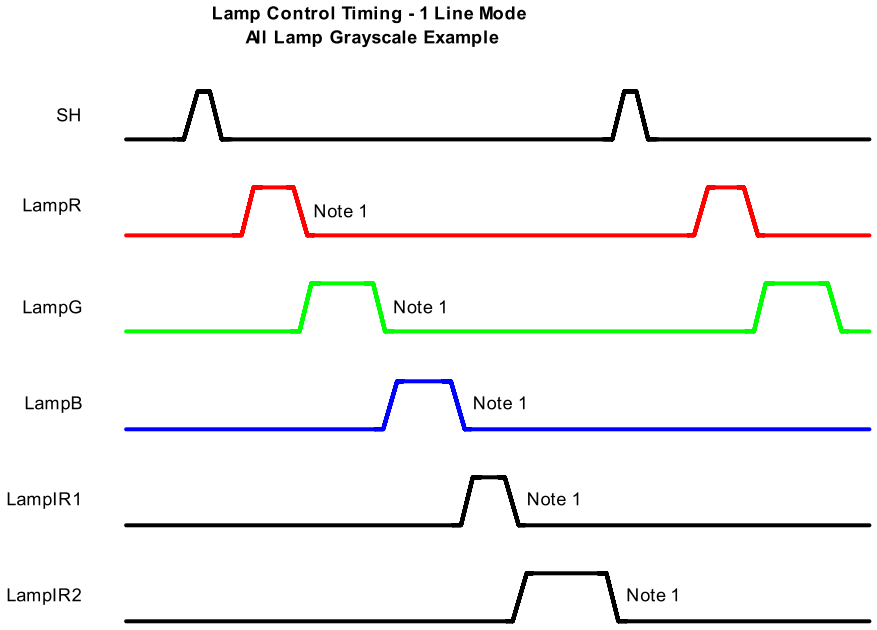
Note 1: MODE can be programmed to be static high or low.

Figure 36. Sensor Timing Mode Pin Output Details - Static High/Low



Note 1: MODE can be programmed to transition after a certain number of pixels have been clocked. This can be configured by register setting anywhere from pixel 1 to line end pixels. Polarity can be configured for initially low or initially high.

Figure 37. Sensor Timing Mode Pin Output Details - Active Programmed Transition



Note 1: LampR, LampG, LampB, LampIR1 and LampIR2 each turn on and off every line. The On and Off points are individually programmed for each Lamp output. *Lamps can be on simultaneously if desired and permitted by the CIS and system design.

Figure 38. Lamp Control Timing - 1 Line Mode (Monochrome)

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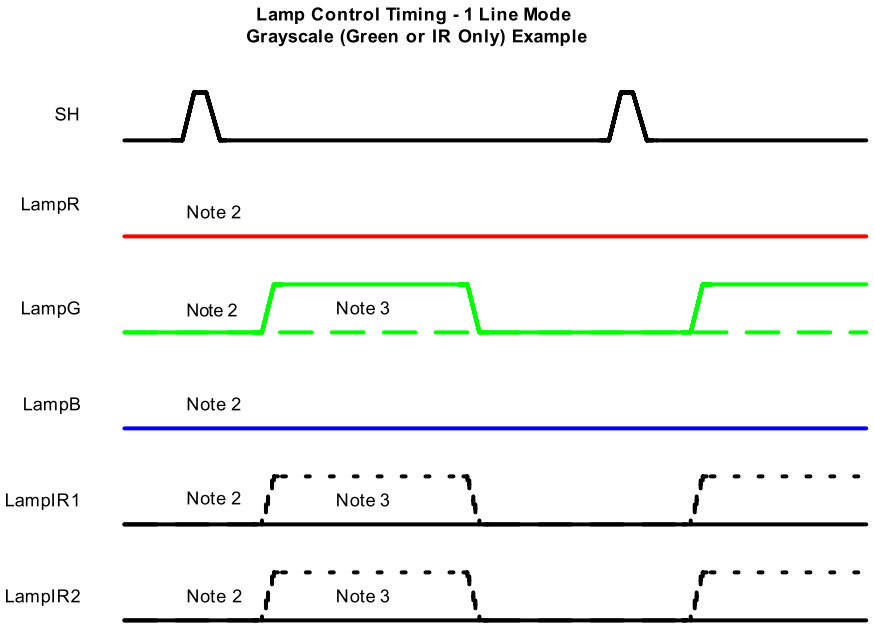
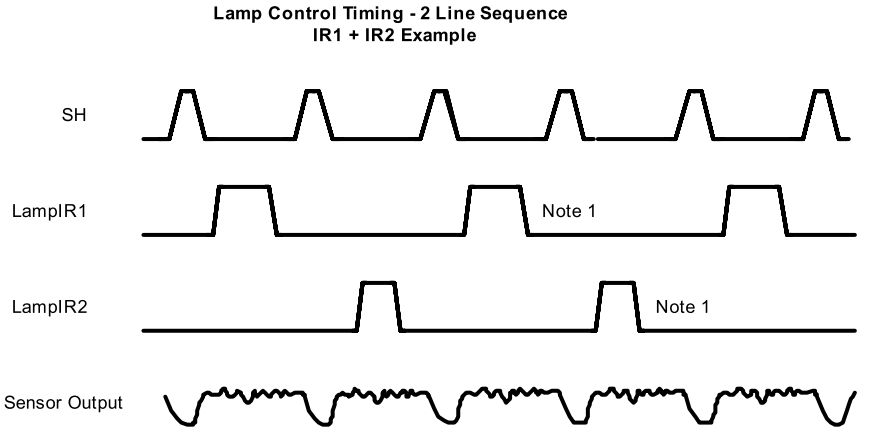


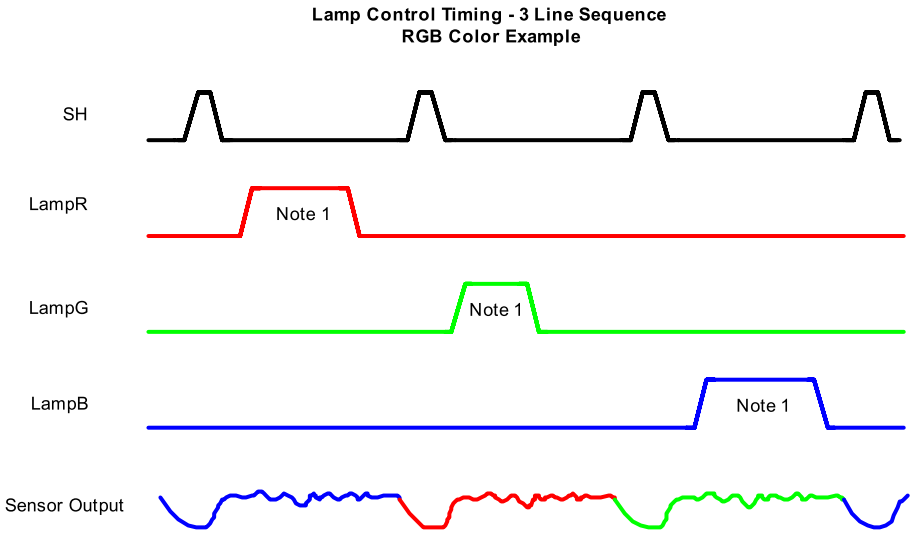
Note 1: LampR, LampG and LampB, LampIR1, and LampIR2 each turn on and off every line. The On and Off points are individually programmed for each Lamp output. *Lamps can be on simultaneously if desired and permitted by the CIS and system design.
Note 2: For Green only lamp mode, the settings for LampR, LampB, LampIR1 and LampIR2 can be set so that those lamps are always off.
Note 3: For IR scanning modes, the settings for LampR, LampG and LampB can be set so that those lamps are always off.

Figure 39. Lamp Control Timing - 1 Line Mode



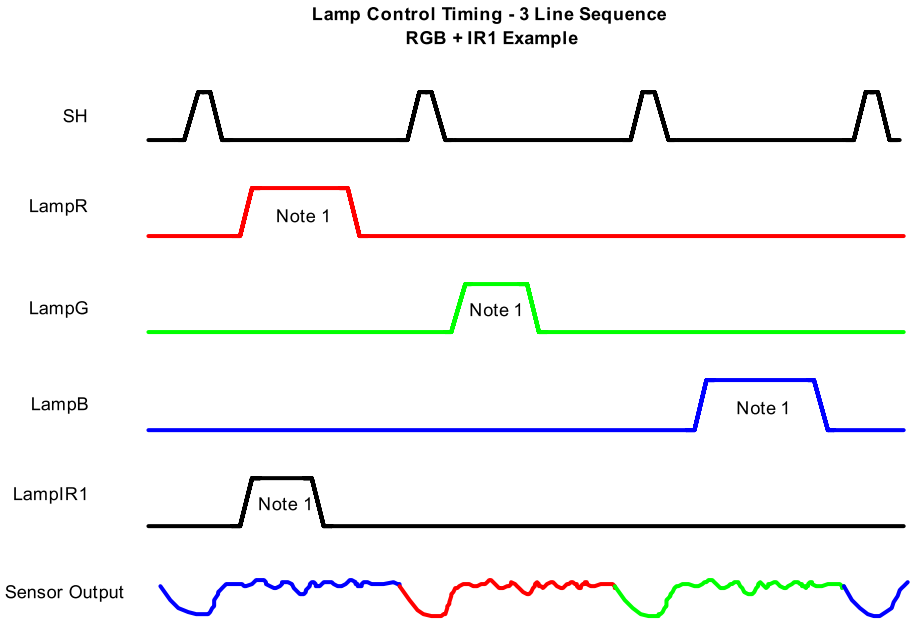
Note 1: In 2 line sequence mode, the Lamp outputs turn on sequentially, with the selected outputs on each line. Lamp On and Off points can be set individually via register control. Polarity is also selectable by register control.

Figure 40. Lamp Control Timing - 2 Line Sequence



Note 1: In the three line color sequence, the Lamp outputs turn on sequentially, with selected colors output on each line. Each of the three lines in the sequence can have the Lamps individually selected. Lamp On and Off points can be set individually via register control. Polarity is also selectable by register control.

Figure 41. Lamp Control Timing - 3 Line Sequence



Note 1: In the three line color sequence, the Lamp outputs turn on sequentially, with selected colors output on each line. Each of the three lines in the sequence can have the Lamps individually selected, included multiple lamps on in the same line as shown. Lamp On and Off points can be set individually via register control. Polarity is also selectable by register control.

Figure 42. Lamp Control Timing - 3 Line Sequence - IR Enhancement Example

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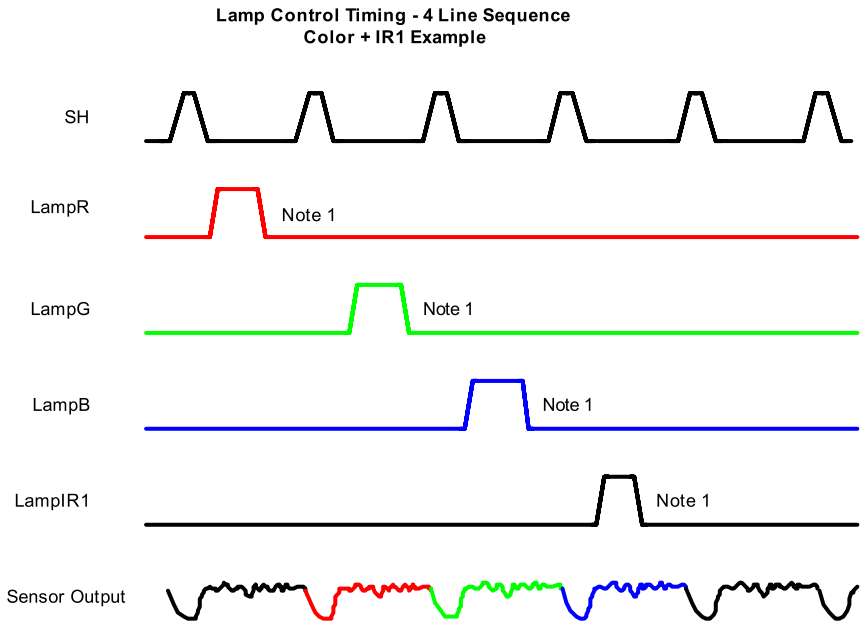
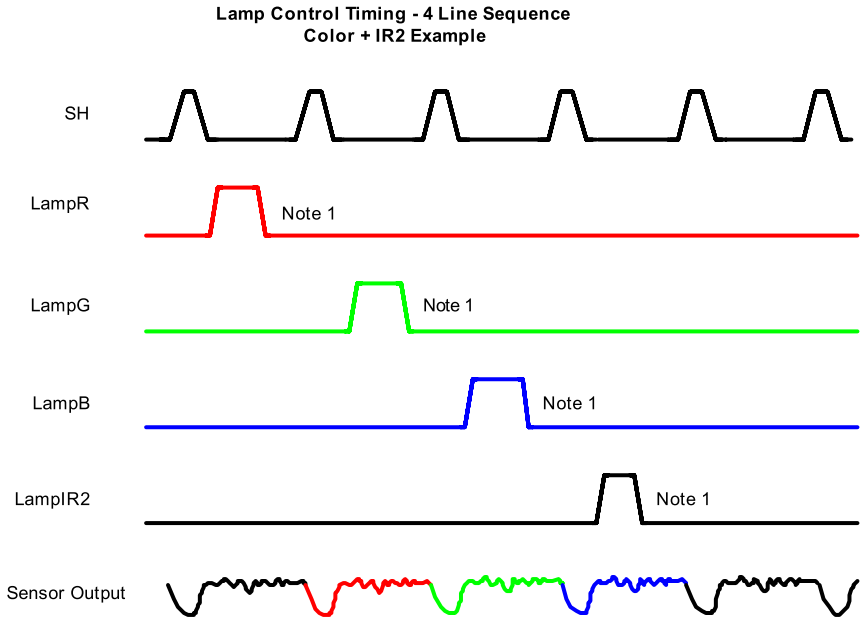


Note 1: In 4 line mode, the Lamp outputs turn on sequentially, with the selected outputs on each line. Lamp On and Off points can be set individually via register control. Polarity is also selectable by register control.

Figure 43. Lamp Control Timing - 4 Line Sequence Color + IR1 Example



Note 1: In 4 line mode, the Lamp outputs turn on sequentially, with the selected outputs on each line. Lamp On and Off points can be set individually via register control. Polarity is also selectable by register control.

Figure 44. Lamp Control Timing - 4 Line Sequence Color + IR2 Example

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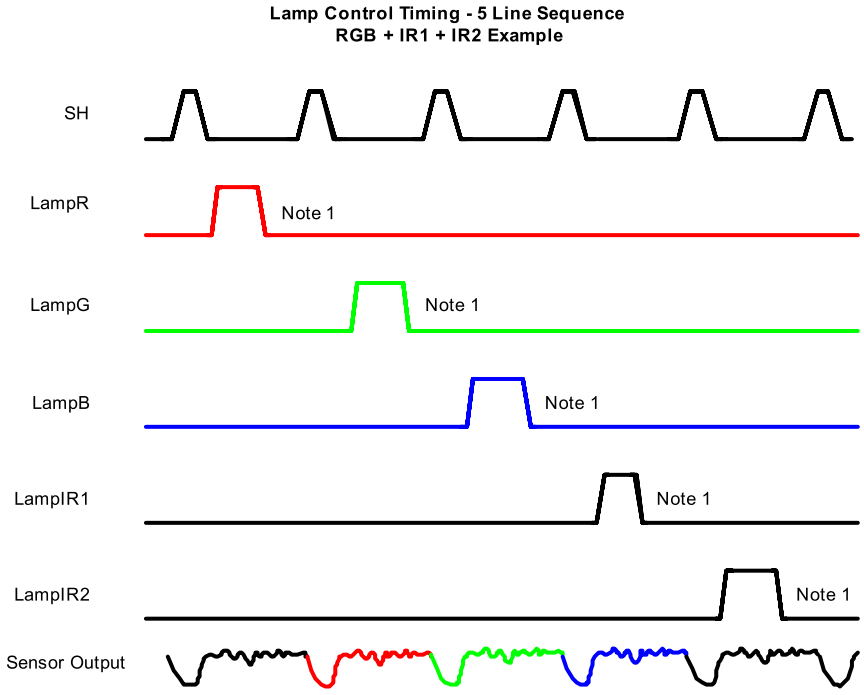

Note 1: In 5 line lamp mode, the Lamp outputs turn on sequentially, with the selected Lamps on each line. Lamp On and Off points can be set individually via register control. Polarity is also selectable by register control.

Figure 45. Lamp Control Timing - 5 Line Sequence

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PIX SIGNAL GENERATOR OR/NOR MODES

As shown in Figure 32, the PIX signal generators outputs can be used in their normal form and sent to the LM98714 output pins, or, they can be sent through an additional layer of OR and NOR logic to provide a number of clocking variations. The OR and NOR combinations of multiple PIX signals can be useful for such modes as pixel lumping, or other modes where more complicated phi clocks are required.

The OR and NOR functions are chosen through the PIX OR/NOR Control 1 and PIX OR/NOR Control 2 registers on Page 4 of the serial interface register map. When all of the OR/NOR control bits are 0 (default) the PIX signals are sent directly from the pix signal generators to the output pins configured by the Output Mapping Control registers (register Page 3). When an OR/NOR control bit is set to 1, the OR or NOR product of multiple pix signal generators is routed to the output pin described in the register details.

SH2 AND SH3 GENERATION

In some sensors, there is a requirement for up to three “SH” type signals. The LM98714 CCD Timing Generator can be configured to produce optional SH signals as shown in Figure 46, these SH signals (SH2 and SH3) toggle every other line and are coincident with the original SH pulse.

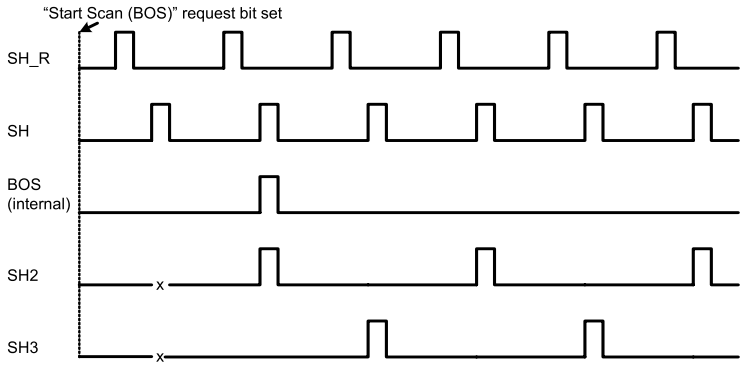

Figure 46. SH2 and SH3 Generation

The “Start Scan (BOS)” request bit is used to begin the proper sequence of CCD Timing outputs at the beginning of a scan. The first line of pixels are being processed by the CCD during the first integration period (after the first SH). The BOS signal (internal to the LM98714) occurs at the second SH to signal when the first line of pixels are actually shifting out of the CCD and in to the AFE. The SH2 pulse is synchronized with the BOS signal and continues to toggle on an every other line basis. The SH3 signal occurs on opposite lines from SH2.

The SH2 and SH3 signals are available in place of the Lamp IR1 and Lamp IR2 outputs respectively. The routing of SH2 and SH3 is depicted in Figure 32. The use of SH2 and SH3 is selected by the SH2/SH3 Control register (0x0F) on Page 4 of the register map.

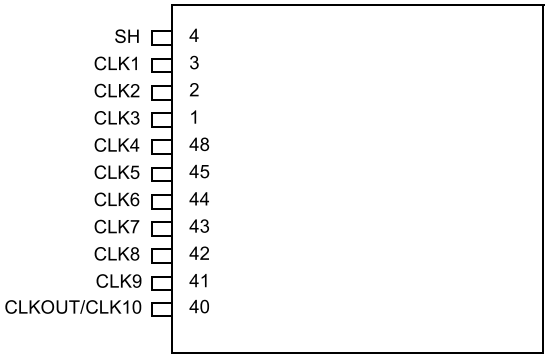

Figure 47. Sensor Control Outputs

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Table 7 shows a number of example mappings of the sensor timing signals to the sensor control CLKn outputs. Several typical timings are shown here, but any timing generator signal can be mapped to any of the CLKn outputs, providing maximum flexibility.

Table 7. Sensor Timing Mappings Examples

Sensor Control Output	Example A	Example B	Example C	Example D	Example E	Example F
SH	SH	SH	SH	SH	SH	SH
CLK1	PIX1(PHI1)	PIX1(PHI1)	PIX1(PHI1)	PIX1(PHI1)	PIX1(PHI1)	PIX1(PHI1)
CLK2	PIX2(PHI2)	PIX2(PHI2)	PIX2(PHI2)	PIX2(PHI2)	PIX2(PHI2)	PIX2(PHI2)
CLK3	PIX3(RS)	PIX3(RS)	PIX3(RS)	PIX3(RS)	PIX3(PHI3)	PIX3(RS)
CLK4	PIX4(CP)	PIX4(CP)	$LAMP_R$	PIX4(CP)	PIX4(PHI4)	PIX4(CP)
CLK5	$LAMP_R$	$LAMP_R$	$LAMP_G$	$LAMP_R$	PIX5(PHI5)	CB[0]
CLK6	$LAMP_G$	$LAMP_G$	$LAMP_B$	$LAMP_G$	PIX6(PHI6)	CB[1]
CLK7	$LAMP_B$	$LAMP_B$	LAMPIR1	$LAMP_B$	PIX7(RS)	CB[2]
CLK8	MODE	LAMPIR1	LAMPIR2	LAMPIR1	PIX8(CP)	CB[3]
CLK9	PIX5(PHI3)	LAMPIR2	MODE	LAMPIR2	MODE	CB[4]
CLKOUT/CLK10		(MODE)		PIX5(PHI3)		CLKOUT

These examples can be used for any customer need, but typical applications would be as follows:

In Examples A, B and C, only 10 sensor control outputs are used. This is to allow the CLKOUT/CLK10 pin to be used as a timing reference for the image output data when the outputs are in CMOS mode.

Example A: Used with most CCD or CIS sensors, including new sensors with 3 PHI clock inputs. Will support up to 3 color LED lamps. Supports CCD sensors with switchable resolution through the MODE control output.

Example B: Used in applications where up to 2 additional IR lamps are used in addition to the R, G, B lamps. No resolution MODE output is available.

Example C: Used where no CP pulse is needed, but 5 lamp outputs are needed as well as a MODE sensor resolution control pin.

In Examples D and E, the CLK10 output is also used. These modes are not available when the image data outputs are operating in CMOS mode.

Example D: Provides both PHI3 output and 5 LED lamp outputs. Does not provide MODE output for resolution control.

Example E: Provides 5 LED lamp outputs, and the MODE output for sensor resolution control.

CCD Timing Generator Master/Slave Modes

The internal CCD Timing generator is capable of operating in Master Mode or in Slave Mode. The Master/Slave operation is configured with the SH Mode Register (Register 0x00 on Page 2). In either Master or Slave Mode, control bit data can be sent to the output of the LM98714 to indicate when each new scan is starting as well as pixel information such as color, type (active, black, dummy, etc.), and the beginning of each line.

MASTER TIMING GENERATOR MODE

In Master Timing Mode, the LM98714 controls the entire CCD Timing Generator based on a Start Scan Bit (Main Configuration Register 2, Bit[0] is the “Start Scan” or “BOS/Beginning of Scan” bit). The Start Scan bit is set by the user to request a new scan. This bit is a self clearing register bit written to the serial interface. When received, the LM98714 controls where and when each new line of the scan begins and ends based on the CCD Timing Generator register settings. The scan is enabled as long as the $\overline{\text{Active/Standby}}$ bit is low. The period of the line (integration time) is controlled by the SH Width setting (SH Pulse Width Register) and the Line End setting (Line End MSB and Line End LSB registers).

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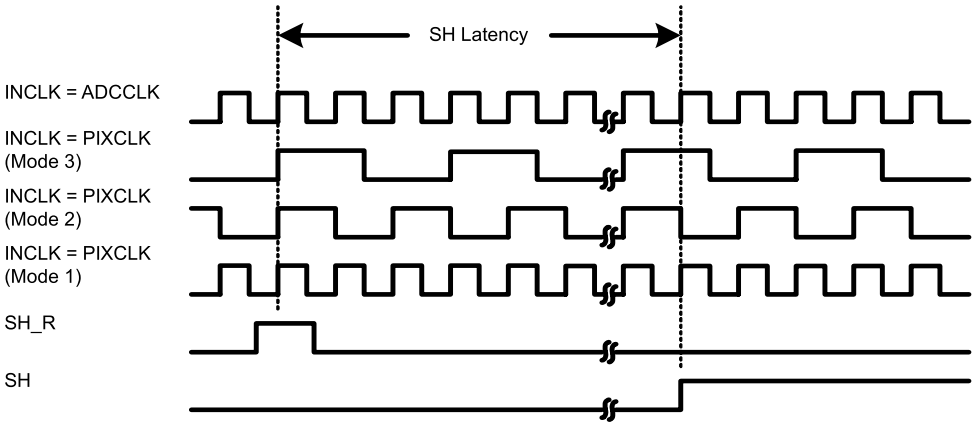
SLAVE TIMING GENERATOR MODE

In Slave Timing Mode, the LM98714 CCD Timing Generator is controlled by the external SH_R pin. Each new line of a scan is initiated by an SH_R pulse. The period of the line (integration time) is mainly controlled by the period of the incoming SH_R signal.



	If PIX Off Guardband > 1	If PIX Off Guardband <= 1
Mode 3 SH Latency	4 ADCCLK + 3*PIX Off Guardband	7 ADCCLK
Mode 2 SH Latency	4 ADCCLK + 2*PIX Off Guardband	6 ADCCLK
Mode 1 SH Latency	4 ADCCLK + PIX Off Guardband	5 ADCCLK

Note*: Latency is calculated with the largest programmed PIX Off Guardband value.

Figure 48. SH_R Input to SH Output Latency Diagram

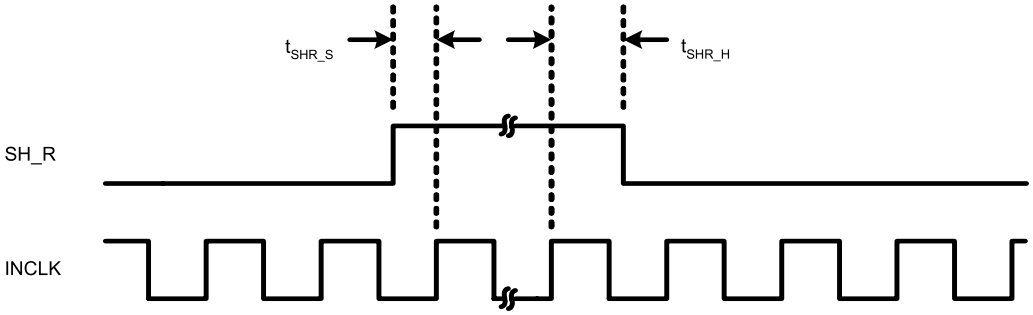


Figure 49. SH_R to INCLK (PIXCLK or ADCCLK) Timing

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CCD Timing Generator Pixel Position Definition

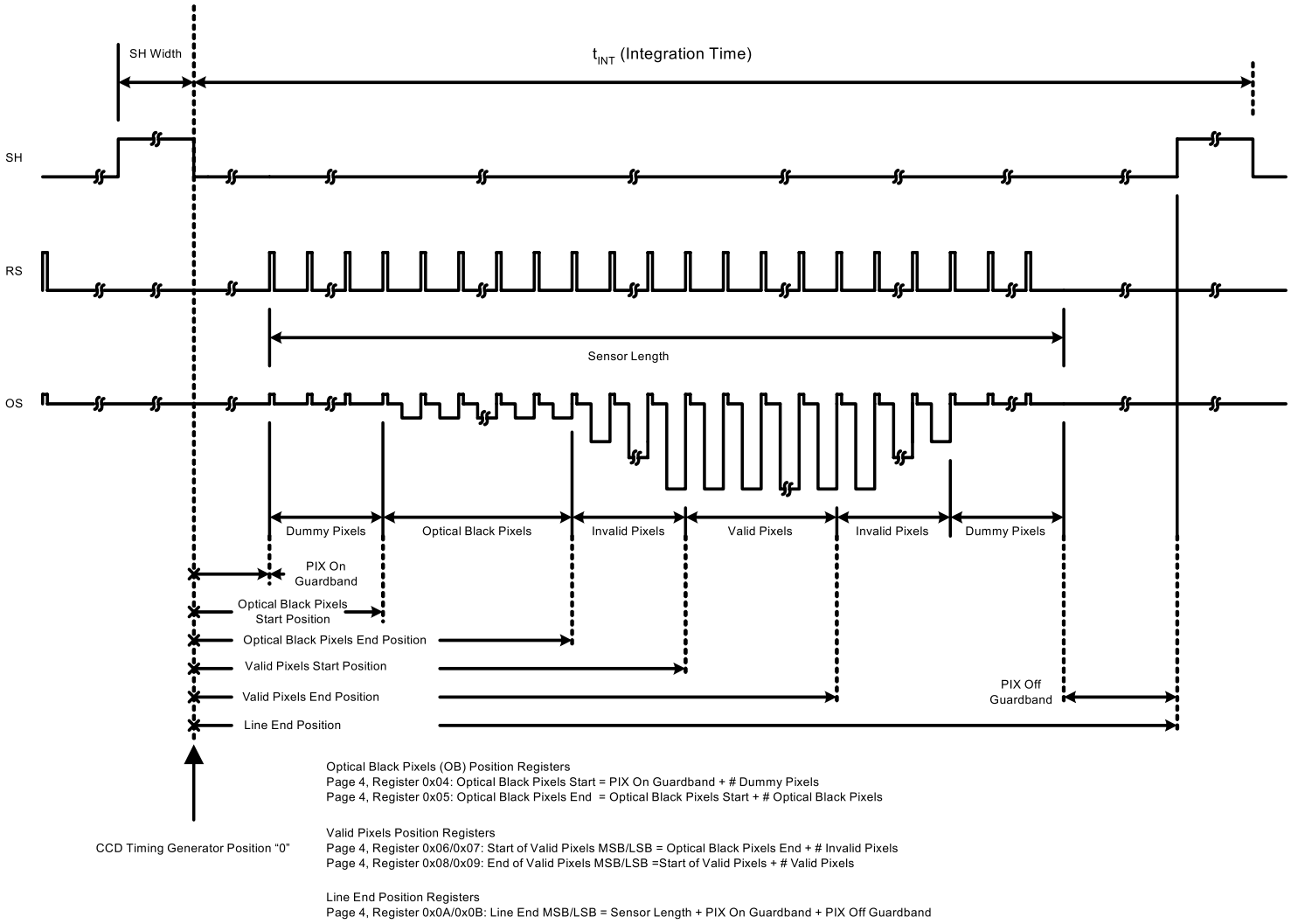

Figure 50.

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LVDS Output Mode

LVDS OUTPUT FORMAT

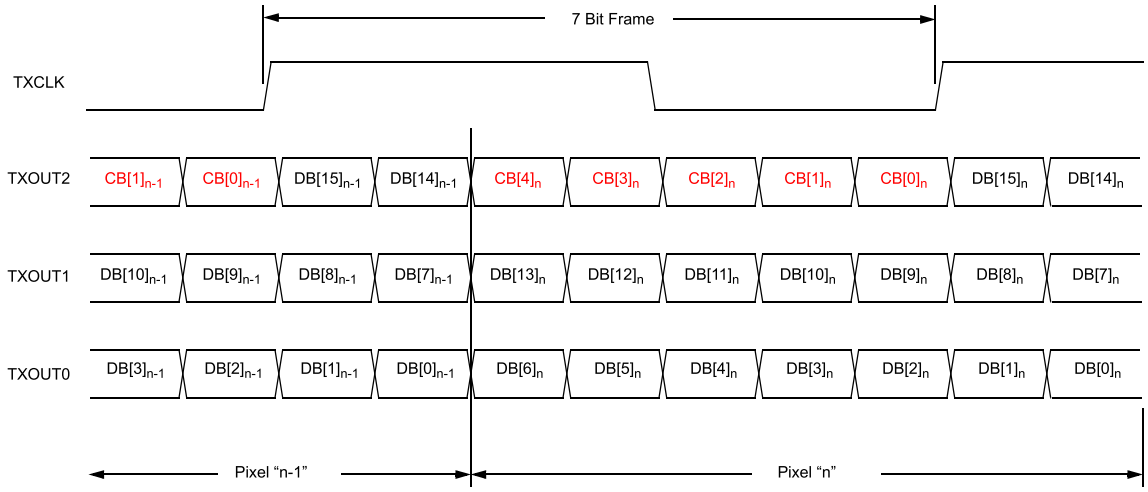

Figure 51. LVDS Output Bit Alignment and Data Format

LVDS Output Timing Details

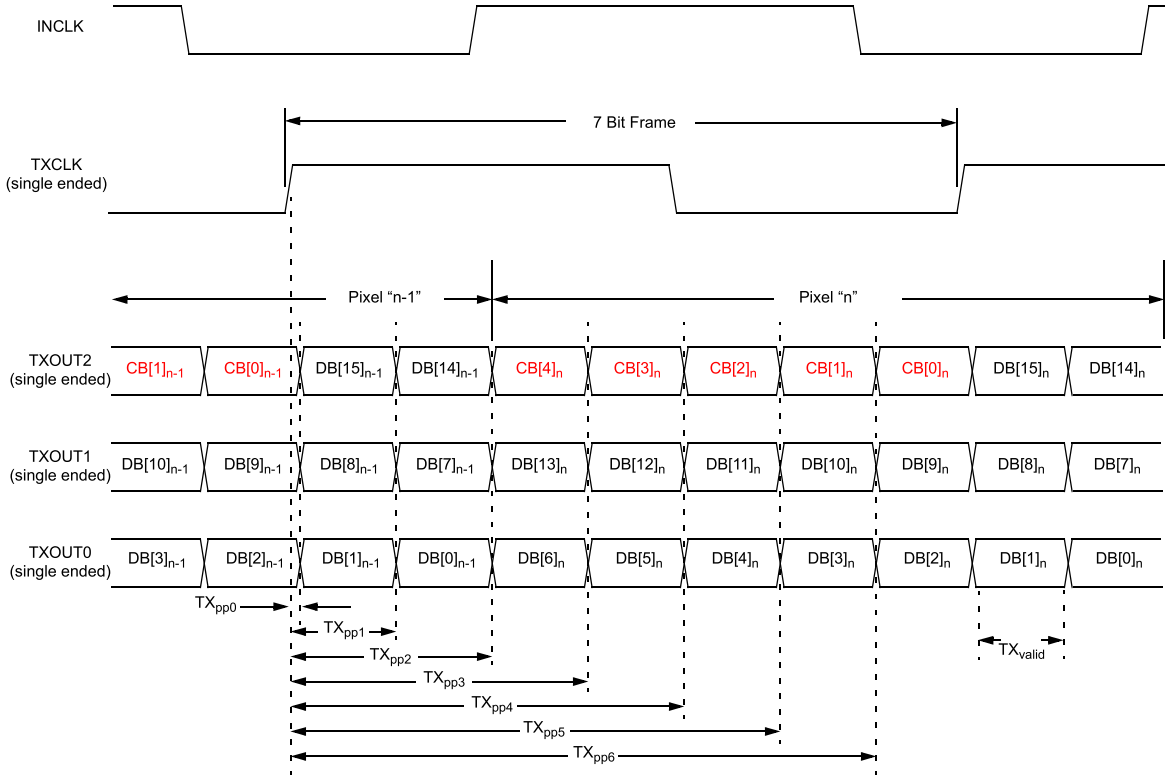

Figure 52. LVDS Data Output Mode Specification Diagram

LVDS CONTROL BIT CODING

The 5 control bits included in the LVDS data stream are coded as follows:

The "active" and "black" pixel tags are programmable tags that the LM98714 provides in order to identify how many pixels have been processed since the falling edge of SH.

Which pixels are given "active" and "black" CB tags is controlled by Page 4, registers 0x08 through 0x0D (Optical Black Pixels Start, Optical Black Pixels End, Start of Valid Pixels, and End of Valid Pixels).

The LM98714 counts the number of pixel periods after the falling edge of SH: If the number of pixel periods after the falling edge of SH is between "optical black pixels start" and "optical black pixels end" the CB bits will indicate that the pixel is a black pixel. If the number of pixel periods after the falling edge of SH is between "start of valid pixels" and "end of valid pixels" the CB bits will indicate that the pixel is an active pixel.

Table 8.

CB[4]	Description
0	Not the beginning of line
1	Beginning of Line
	(This bit is high for as many pixels as SH pulse is active)

Table 9.

CB[3:0]	Description
0	Dummy Pixels
1	Red Active Pixels
10	Green Active Pixels
11	Blue Active Pixels
100	IR1 Active Pixels
101	IR2 Active Pixels
110	Red Black Pixels
111	Green Black Pixels
1000	Blue Black Pixels
1001	IR1 Black Pixels
1010	IR2 Black Pixels
1111	Beginning of Scan

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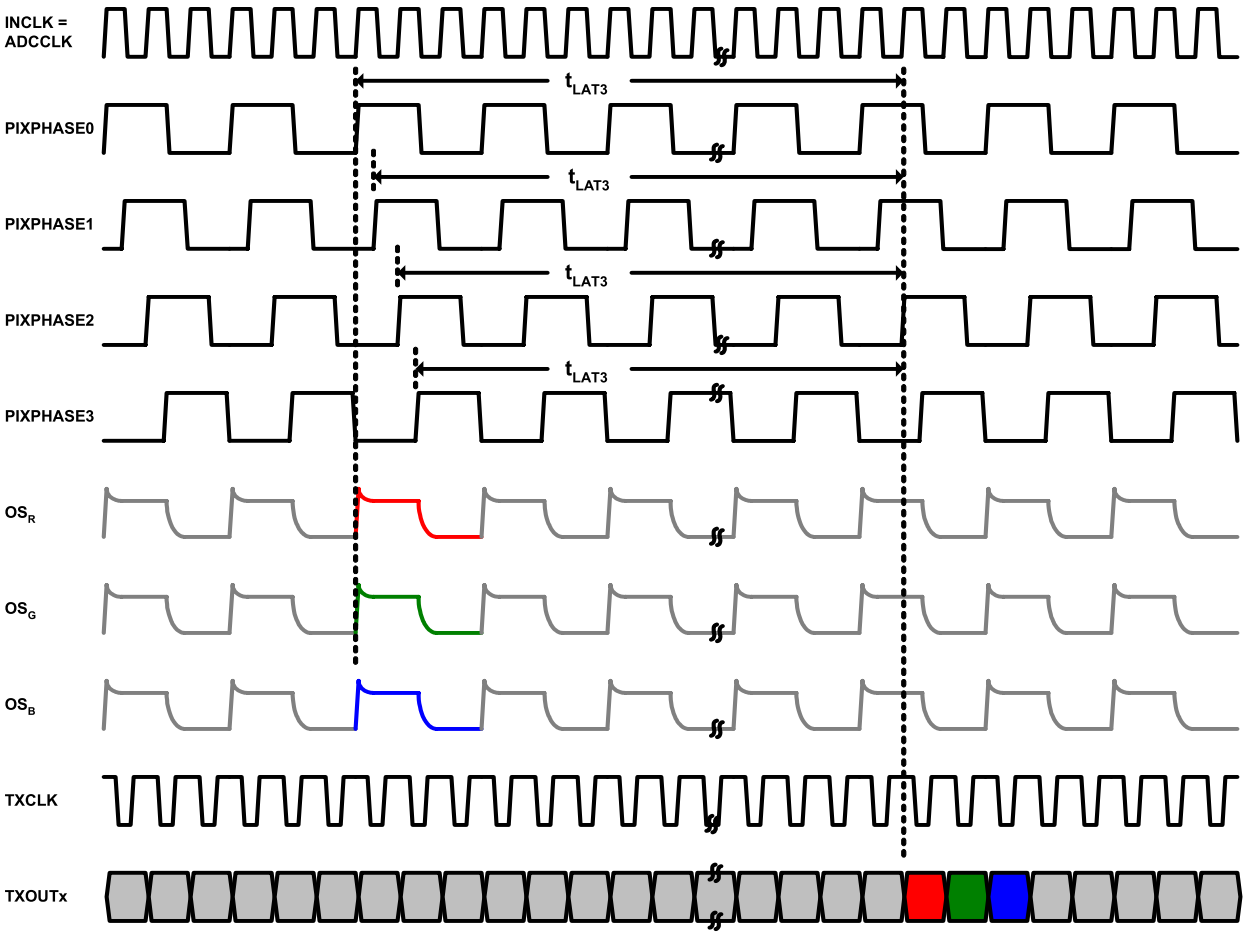
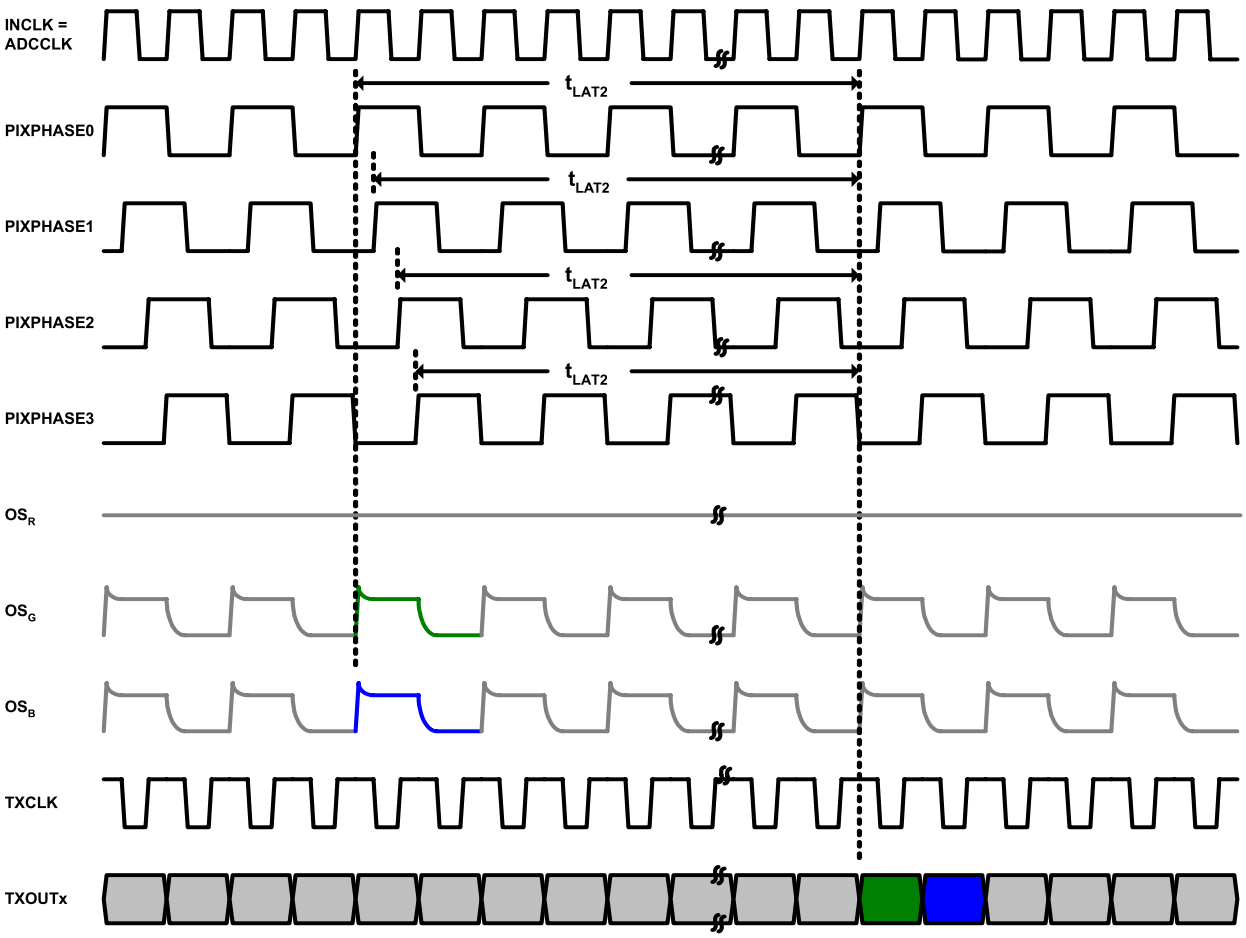
LVDS DATA LATENCY DIAGRAMS



Data latency shown is for Mode 3 in relation to PIXPHASE0 with the processing order set to $OS_R \leftrightarrows OS_G \leftrightarrows OS_B$. If the incoming pixels are not aligned with PIXPHASE0, one of the remaining PIXPHASEs can be selected as the sampling phase without effecting the output data location.

Figure 53. Mode 3 LVDS Data Latency



Data latency shown is for Mode 2 in relation to PIXPHASE0 with the processing order set to OS_G⇆OS_B. If the incoming pixels are not aligned with PIXPHASE0, one of the remaining PIXPHASEs can be selected as the sampling phase without effecting the output data location.

Figure 54. Mode 2 LVDS Data Latency

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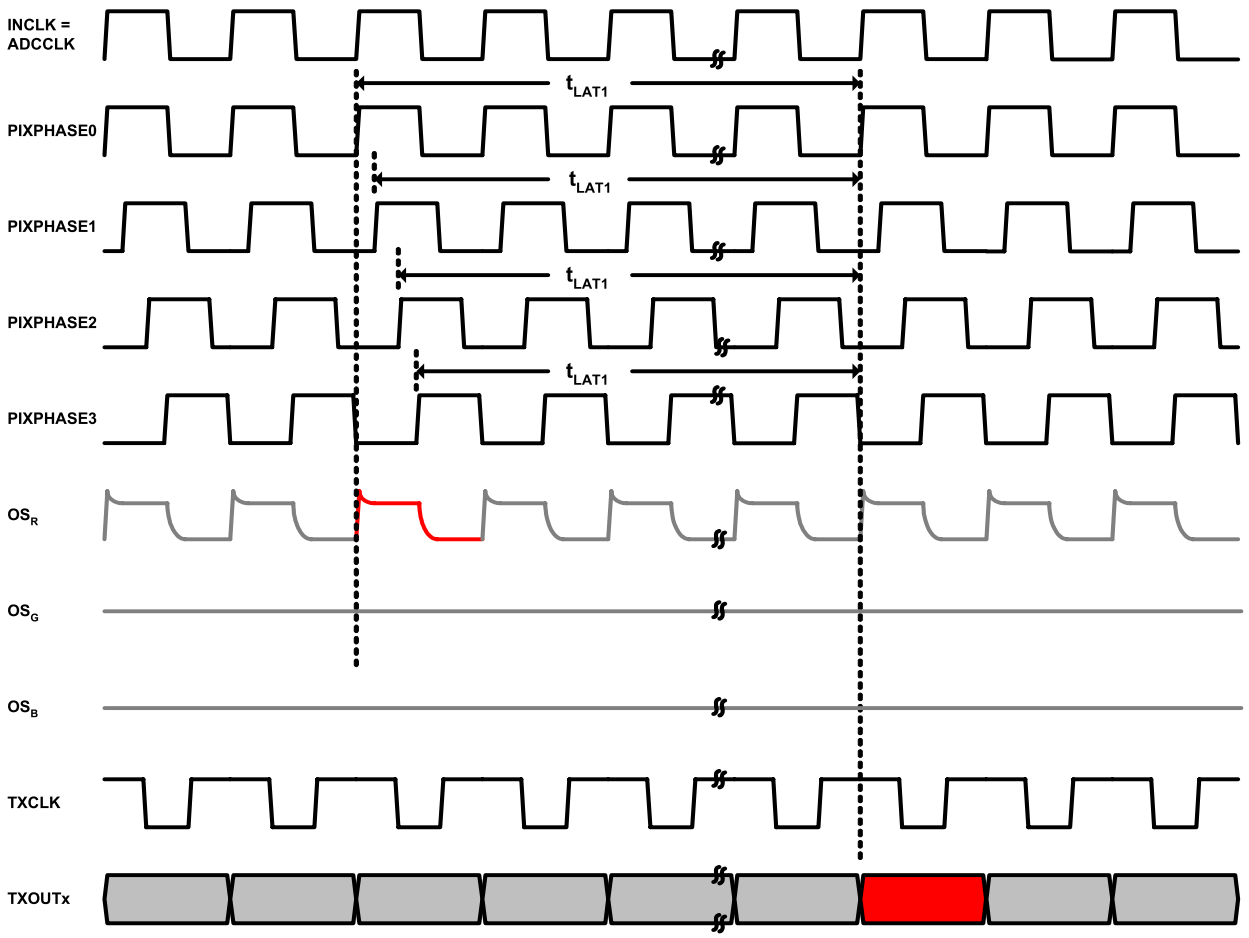

Data latency shown is for Mode 1 in relation to PIXPHASE0 with the processing channel configured to OS_R. If the incoming pixels are not aligned with PIXPHASE0, one of the remaining PIXPHASEs can be selected as the sampling phase without effecting the output data location.

Figure 55. Mode 1 LVDS Data Latency

LVDS TEST MODES

The LVDS test modes present several different data patterns to the input of the LVDS serializer block. All 21 bits are used and there is no control bit coding present. The SH signal resets the LVDS test pattern and the pattern will resume only after SH is deasserted. If no SH signal is sent, the pattern continues indefinitely.

Test Mode 1 - Worst Case Transitions

This test mode provides an LVDS output with the maximum possible transitions. This mode is useful for system EMI evaluations, and for ATE timing tests.

The effective data values are an alternating pattern between 21'b101010101010101010101 (0x155555) and 21'b010101010101010101010 (0x0AAAAA). This test pattern resets to 0x155555 after the SH signal.

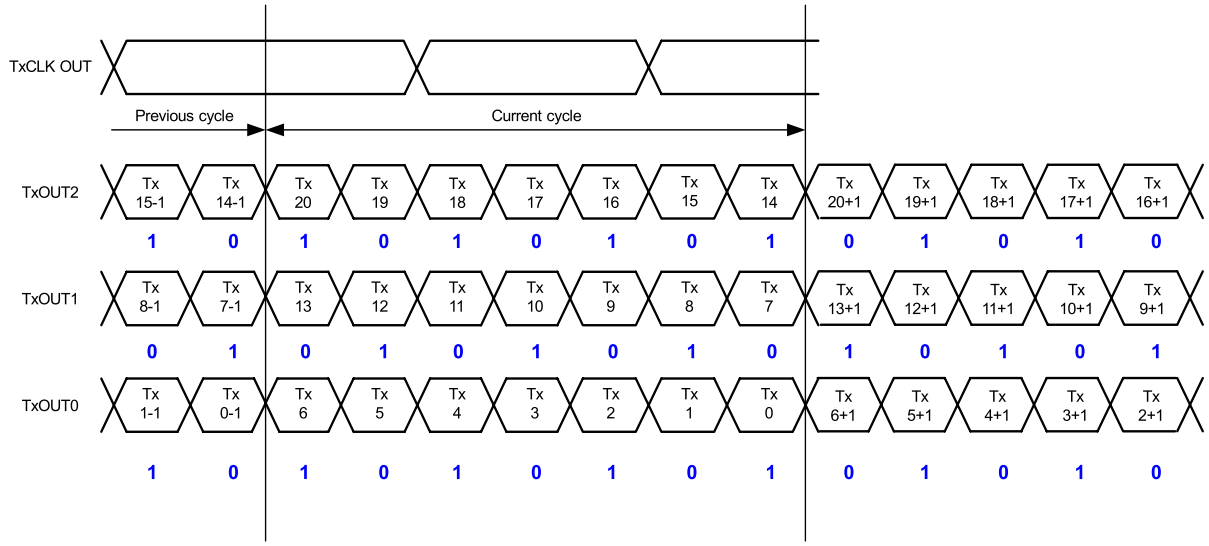

Figure 56. LVDS Test Pattern

Test Mode 2 - Ramp

This mode provides LVDS data that progresses from 0x00000 to the full scale output 0x1FFFFF incrementing by 1 per LVDS Clock. When the LVDS ramp test pattern is selected, the ramp begins immediately and counts from zero to the full scale value, and then repeats.

Test Mode 3 - Fixed Output Data

This mode allows a fixed data value to be output. The value is set via. Upcounter Register 1, 2 and 3. The 21 bit value taken from these registers is repetitively sent out over the LVDS link. This is useful for system debugging of the LVDS link and receiver circuitry.

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CMOS Output Mode

CMOS Output Data Format

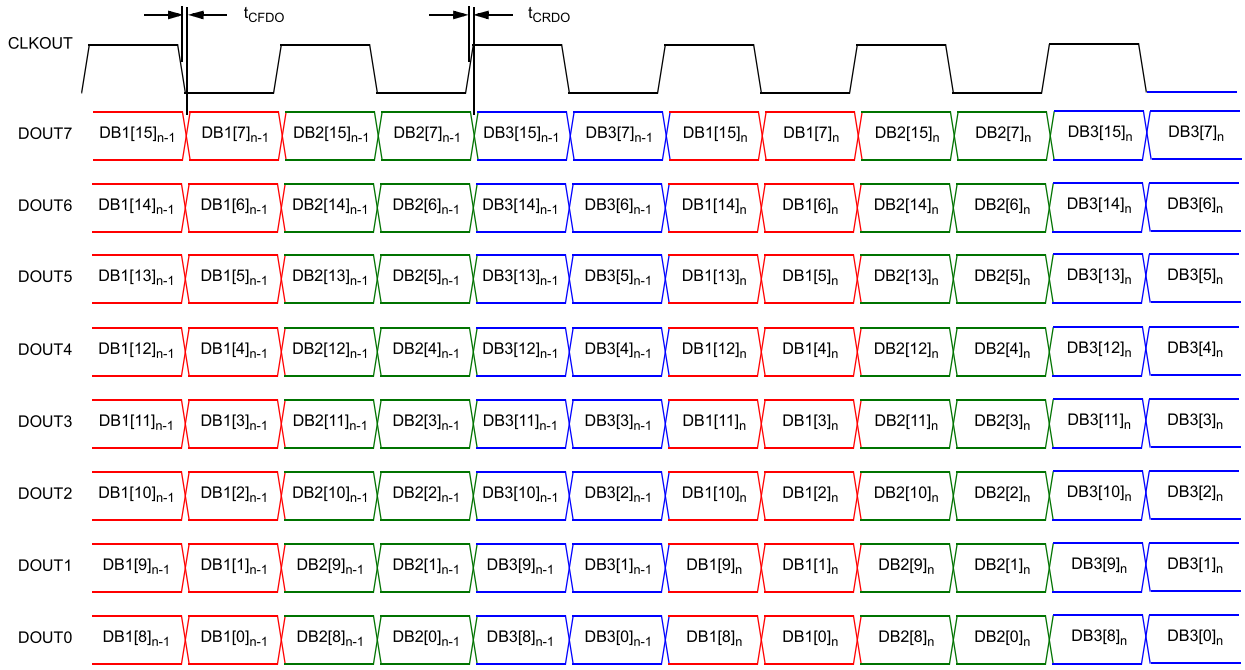
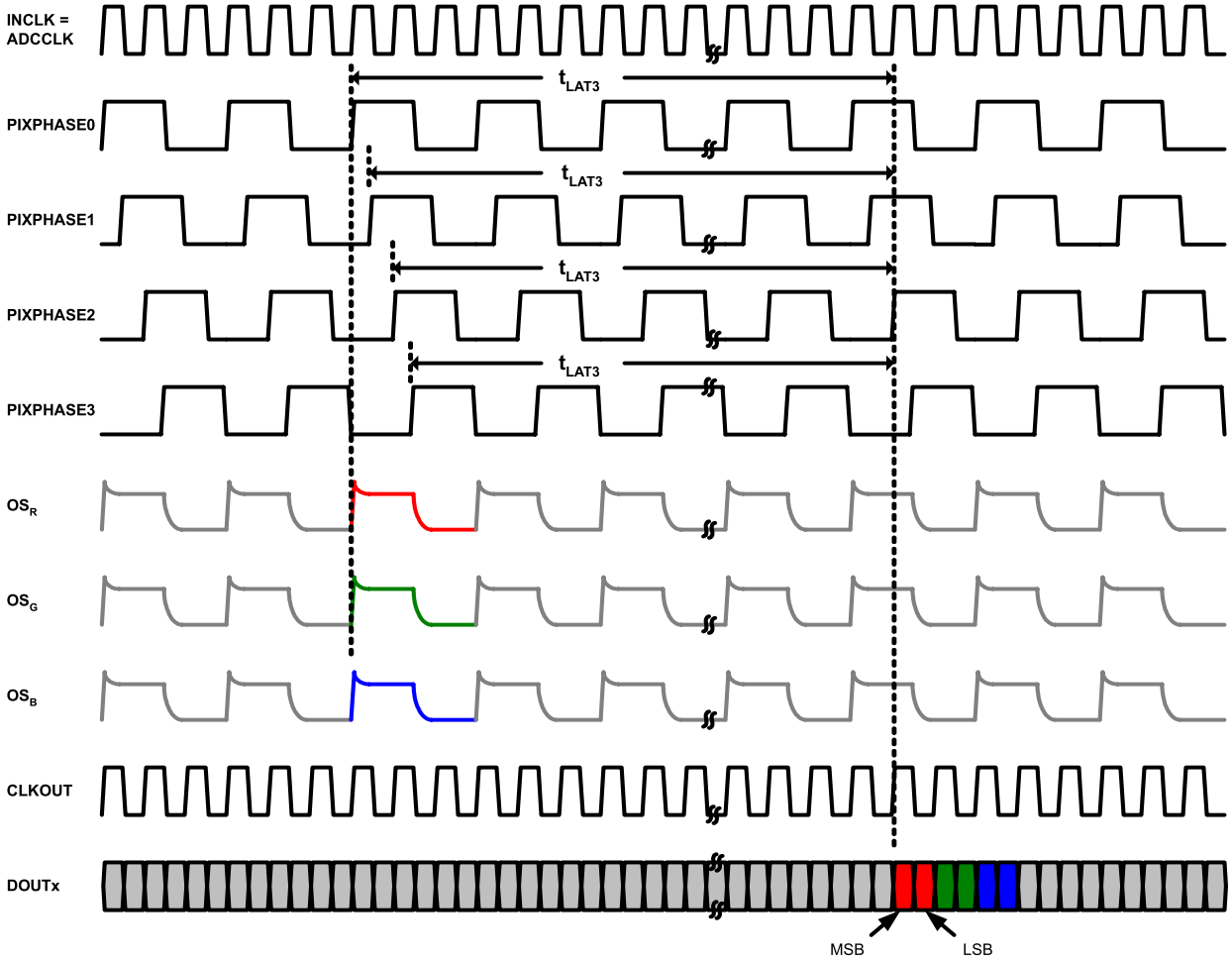


Figure 57. CMOS Data Output Format (Mode 3 Shown)

CMOS Output Data Latency Diagrams



Data latency shown is for Mode 3 in relation to PIXPHASE0 with the processing order set to $OS_R \leftrightarrows OS_G \leftrightarrows OS_B$. If the incoming pixels are not aligned with PIXPHASE0, one of the remaining PIXPHASEs can be selected as the sampling phase without effecting the output data location.

Figure 58. Mode 3 CMOS Output Latency

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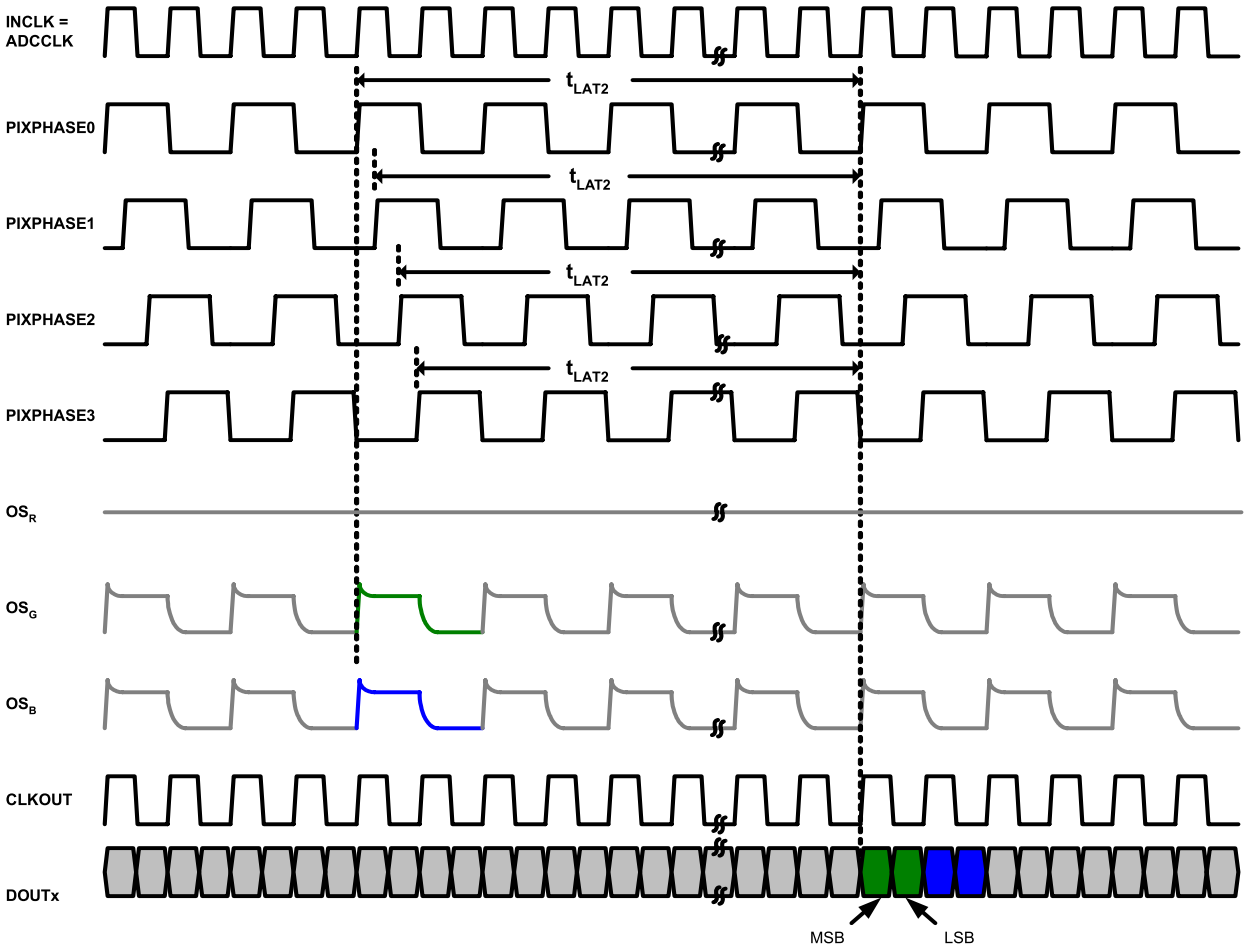
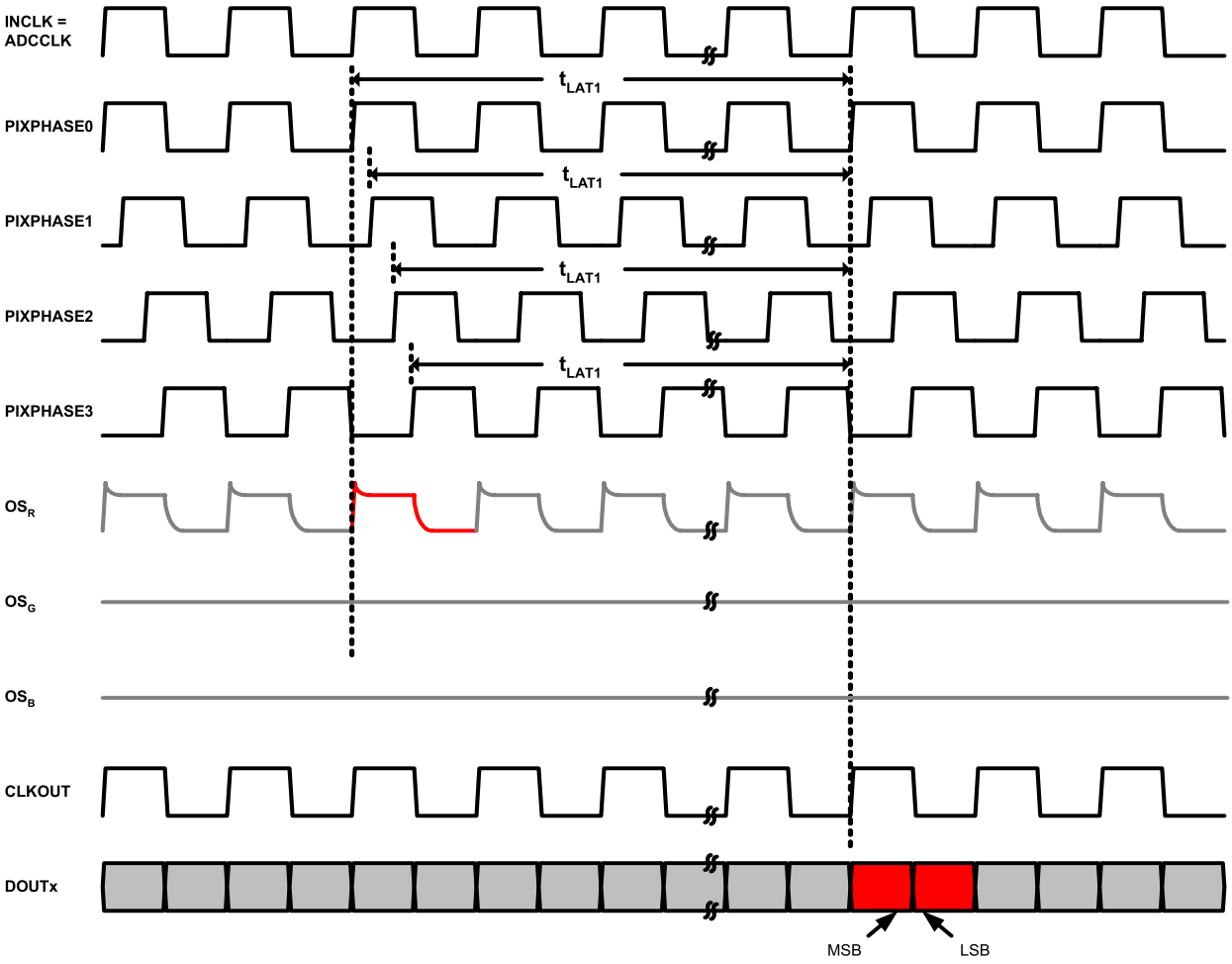


Data latency shown is for Mode 2 in relation to PIXPHASE0 with the processing order set to OS_G⇆OS_B. If the incoming pixels are not aligned with PIXPHASE0, one of the remaining PIXPHASEs can be selected as the sampling phase without effecting the output data location.

Figure 59. Mode 2 CMOS Output Latency



Data latency shown is for Mode 1 in relation to PIXPHASE0 with the processing channel configured to OS_R. If the incoming pixels are not aligned with PIXPHASE0, one of the remaining PIXPHASEs can be selected as the sampling phase without effecting the output data location.

Figure 60. Mode 1 CMOS Output Latency

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Serial Interface

A serial interface is used to write and read the configuration registers. The interface is a three wire interface using SCLK, SEN, and SDIO connections. The main input clock (INCLK) to the LM98714 must be active during all Serial Interface commands.

WRITING TO THE SERIAL REGISTERS

To write to the serial registers, the timing diagram shown in Figure 61 must be met. First, SEN is toggled low. The LM98714 assumes control of the SDIO pin during the first eight clocks of the command. During this period, data is clocked out of the device at the rising edge of SCLK. The eight bit value clocked out is the contents of the previously addressed register, regardless if the previous command was a read or a write. At the rising edge of ninth clock, the LM98714 releases control of the SDIO pin. At the falling edge of the ninth clock period, the master should assume control of the SDIO pin and begin issuing the new command. SDIO is clocked into the LM98714 at the rising edge of SCLK. The remaining bits are composed of the “write” command bit (a zero), two device address bits (zeros for the LM98714), five bit register address to be written, and the eight bit register value to be written. When SEN toggles high, the register is written to, and the LM98714 now functions with this new data.

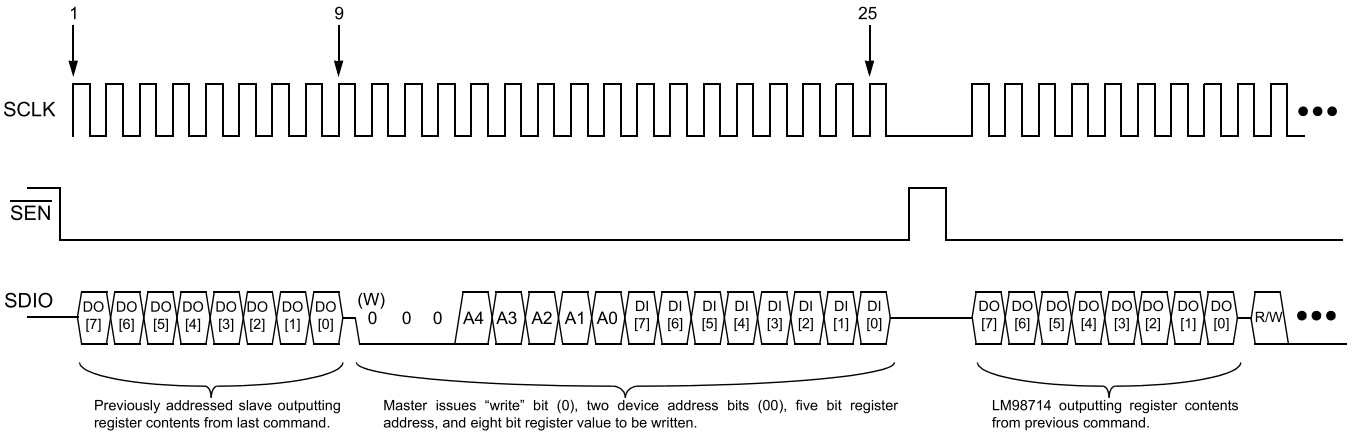

Figure 61. Serial Write

READING THE SERIAL REGISTERS

To read to the serial registers, the timing diagram shown in Figure 62 must be met. First, SEN is toggled low. The LM98714 assumes control of the SDIO pin during the first eight clocks of the command. During this period, data is clocked out of the device at the rising edge of SCLK. The eight bit value clocked out is the contents of the previously addressed register, regardless if the previous command was a read or a write. At the rising edge of ninth clock, the LM98714 releases control of the SDIO pin. At the falling edge of the ninth clock period, the master should assume control of the SDIO pin and begin issuing the new command. SDIO is clocked into the LM98714 at the rising edge of SCLK. The remaining bits are composed of the “read” command bit (a one), two device address bits (zeros for the LM98714), five bit register address to be read, and the eight bit “don’t care” bits. When SEN toggles high, the register is not written to, but its contents are staged to be outputted at the beginning of the next command.

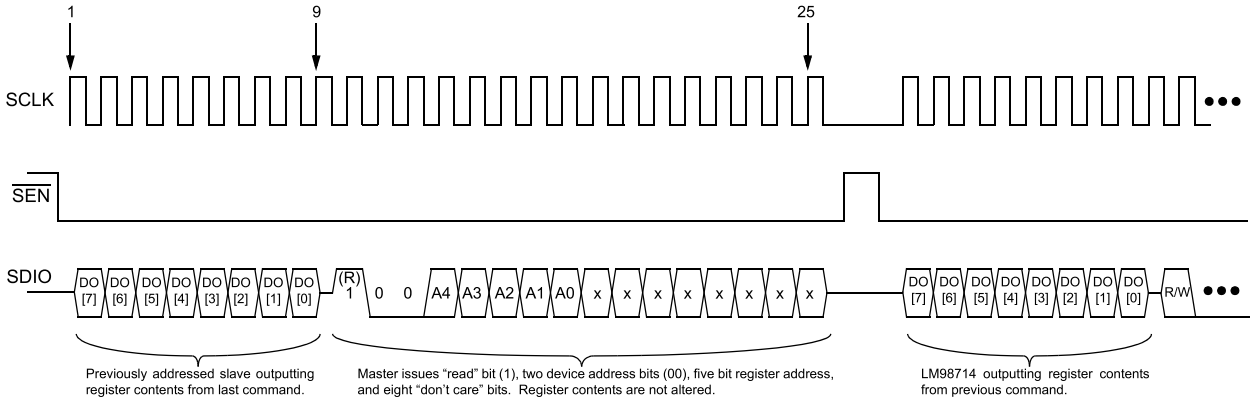

Figure 62. Serial Read

Serial Interface Timing Details

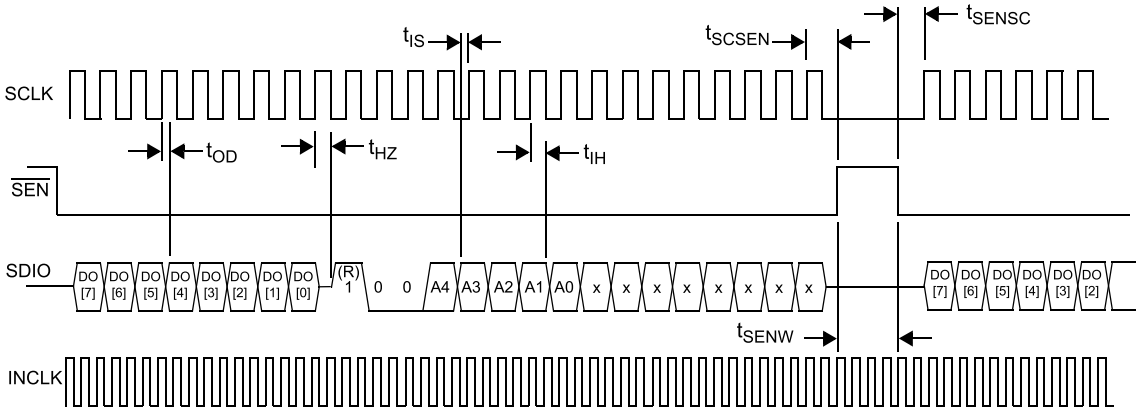

Figure 63. Serial Interface Specification Diagram

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Configuration Registers

The LM98714 operation is very flexible to support a wide variety of sensors and system designs. This flexibility is controlled through configuration registers which are first summarized, then described in full in the following tables. Because the serial interface only allows 5 address bits, a register paging system is used to support the larger number of required registers.

A page register is present at the highest address (1Fh or 11111b). The power on default setting of the page register is 00. Writing other values to this register allows the other pages to be accessed. The page register is mirrored, and is accessible at the highest address on each page.

Figure 64 shows the proper sequence of operation for the LM98714.

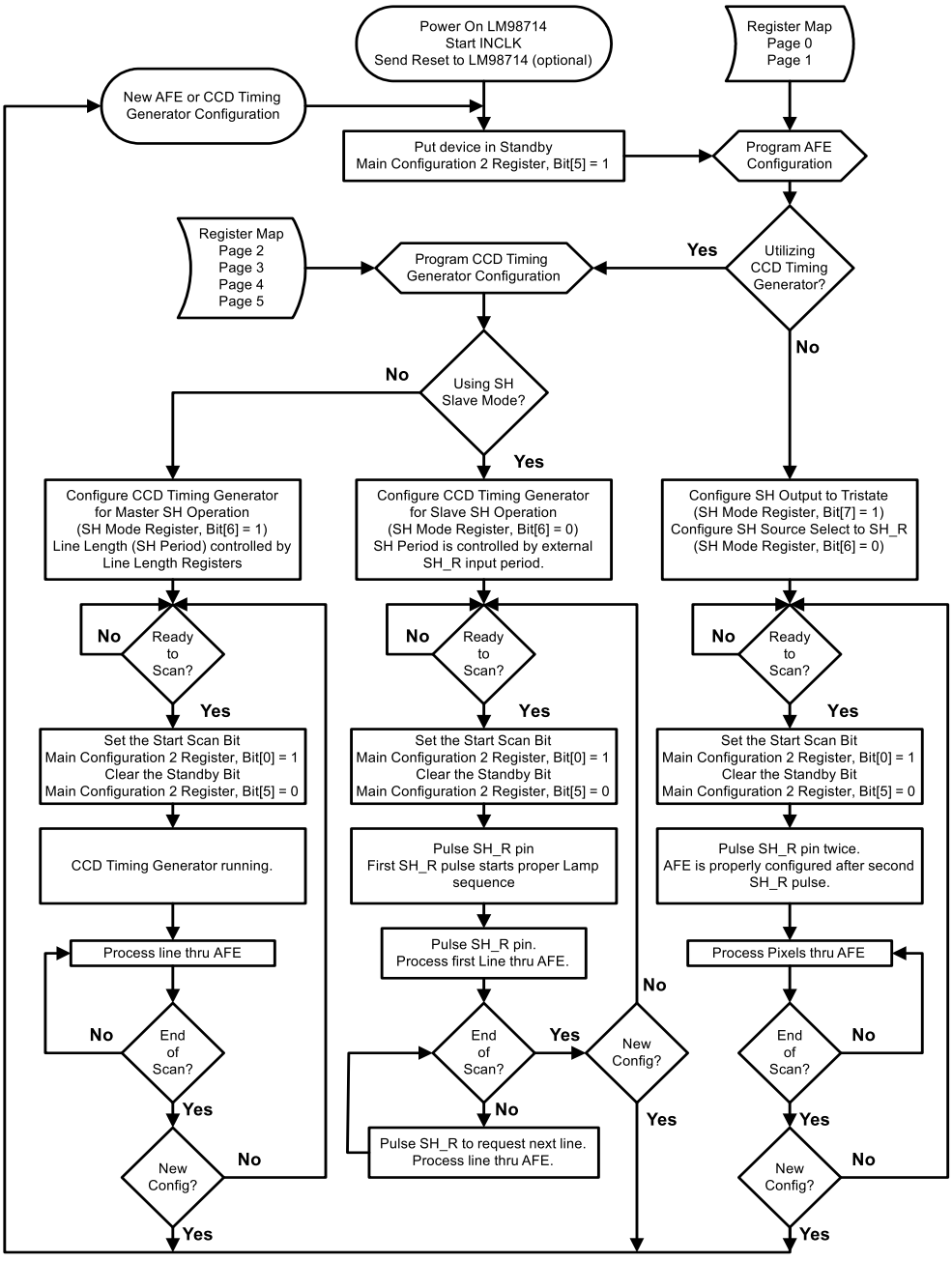

Figure 64. LM98714 Proper Sequence of Operation

PAGE 0 REGISTER TABLE - MAIN ANALOG FRONT END CONFIGURATION

Table 10.

Address (Binary)	Register Title (Mnemonic)	Default (Binary)	Register/Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Note: The active register page is selected by writing the desired value to the page select register 1Fh. This register is mirrored on all register pages.										
Page 0	Page Register 1F = 0000 0000									
00000	Main Configuration 0	1111 0001	Operating Mode Select							
00001	Main Configuration 1	0101 0000	Source Follower Enable	Input Bias Enable	Input Polarity	Sampling Mode Select	Output Format	PIXCLK/ ADCCLK Config.	Pixel Phase Clock Select	
00010	Main Configuration 2	0000 0000	Not Used		$\overline{\text{Active}}$/ Standby	Gain Mode Select	Output Enable	Power-down	Soft Reset	Start Scan
00011	Main Configuration 3	0000 0111					Processing Channel Override	Reserved		
00100	Main Configuration 4	0000 0000	Not Used				Upcount Enable	LVDS Test Mode		
00101	Input Clamp Control	0000 0000	Not Used				Auto CLPIN Width		Auto CLPIN Enable	CLPIN Gating
00110	Auto CLPIN Position	0010 0111	MSB							LSB
00111	VCLP Configuration	0010 0000	Not Used		VCLP Reference Select		VCLP DAC Bits			
01000	Black Level Clamp Control	0000 0000	Line Averaging		Pixel Averaging		Offset Integration		BLKCLP Mode Select	
01001	Auto Black Level Clamp Position	0000 0000	Not Used	MSB						LSB
01010	Target Black Level MSB	0010 0000	MSB							LSB+2
01011	Target Black Level LSB	0000 0000	Not Used						LSB+1	LSB
01100	OS_R CLAMP Control	0000 0000	Not Used			$CLAMP_R$ Position				
01101	OS_G CLAMP Control	0000 0000	Not Used			$CLAMP_G$ Position				
01110	OS_B CLAMP Control	0000 0000	Not Used			$CLAMP_B$ Position				
01111	OS_R SAMPLE Control	0000 0000	Not Used	$SAMPLE_R$ Position						
10000	OS_G SAMPLE Control	0000 0000	Not Used	$SAMPLE_G$ Position						
10001	OS_B SAMPLE Control	0000 0000	Not Used	$SAMPLE_B$ Position						
10010	Upcounter Register 1	0000 0000	Count Value LSBs							
10011	Upcounter Register 2	0000 0000	Count Value Middle 8 Bits							
10100	Upcounter Register 3	0000 0000	Not Used			Count Value MSBs				
10101										
10110										
10111										

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Table 10. (continued)

Address (Binary)	Register Title (Mnemonic)	Default (Binary)	Register/Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11000										
11001										
11010										
11011										
11100										
11101										
11110		0000 0100								
11111	Page Register	0000 0000	Reserved (program all zeros)					LSB+2	LSB+1	LSB

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PAGE 1 REGISTER TABLE - OFFSET AND GAIN SETTINGS

Table 11.

Address (Binary)	Register Title (Mnemonic)	Default (Binary)	Register/Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Note: The active register page is selected by writing the desired value to the page select register 1Fh. This register is mirrored on all register pages.										
Page 1	Page Register 1F = 0000 0001									
00000	Color 1 PGA	0101 0100	MSB							LSB
00001	Color 2 PGA	0101 0100	MSB							LSB
00010	Color 3 PGA	0101 0100	MSB							LSB
00011	Color 4 PGA	0101 0100	MSB							LSB
00100	Color 5 PGA	0101 0100	MSB							LSB
00101	Color 1 Black Level Offset DAC MSB	1000 0000	MSB							LSB+2
00110	Color 1 Black Level Offset DAC LSB	0000 0000	Not Used						LSB+1	LSB
00111	Color 2 Black Level Offset DAC MSB	1000 0000	MSB							LSB+2
01000	Color 2 Black Level Offset DAC LSB	0000 0000	Not Used						LSB+1	LSB
01001	Color 3 Black Level Offset DAC MSB	1000 0000	MSB							LSB+2
01010	Color 3 Black Level Offset DAC LSB	0000 0000	Not Used						LSB+1	LSB
01011	Color 4 Black Level Offset DAC MSB	1000 0000	MSB							LSB+2
01100	Color 4 Black Level Offset DAC LSB	0000 0000	Not Used						LSB+1	LSB
01101	Color 5 Black Level Offset DAC MSB	1000 0000	MSB							LSB+2
01110	Color 5 Black Level Offset DAC LSB	0000 0000	Not Used						LSB+1	LSB
01111	Color 1 Digital Offset	0100 0000	Not Used	MSB						LSB
10000	Color 2 Digital Offset	0100 0000	Not Used	MSB						LSB
10001	Color 3 Digital Offset	0100 0000	Not Used	MSB						LSB
10010	Color 4 Digital Offset	0100 0000	Not Used	MSB						LSB
10011	Color 5 Digital Offset	0100 0000	Not Used	MSB						LSB
10100										
10101										

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Table 11. (continued)

Address (Binary)	Register Title (Mnemonic)	Default (Binary)	Register/Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10110										
10111										
11000										
11001										
11010										
11011										
11100										
11101										
11110		0000 0100								
11111	Page Register	0000 0000	Reserved (program all zeros)					LSB+2	LSB+1	LSB

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PAGE 2 REGISTER TABLE - CCD/CIS TIMING GENERATOR CONTROL 1

Table 12.

Address (Binary)	RegisterTitle (Mnemonic)	Default (Binary)	Register/Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Note: The active register page is selected by writing the desired value to the page select register 1Fh. This register is mirrored on all register pages.										
Page 2	Page Register 1F = 0000 0010									
00000	SH Mode	0000 0000	SH Output Enable	SH Source Select	SH Mode		SH Delay			
00001	SH Pulse Width	0010 0111	SH Pulse Width							
00010	PIX1/2 Control	1100 1000	PIX1 Activity	PIX1 Polarity	PIX1 Frequency	PIX1 Activity During SH	PIX2 Activity	PIX2 Polarity	PIX2 Frequency	PIX2 Activity During SH
00011	PIX3/4 Control	1000 1000	PIX3 Activity	PIX3 Polarity	PIX3 Frequency	PIX3 Activity During SH	PIX4 Activity	PIX4 Polarity	PIX4 Frequency	PIX4 Activity During SH
00100	PIX5/6 Control	0000 0000	PIX5 Activity	PIX5 Polarity	PIX5 Frequency	PIX5 Activity During SH	PIX6 Activity	PIX6 Polarity	PIX6 Frequency	PIX6 Activity During SH
00101	PIX7/8 Control	0000 0000	PIX7 Activity	PIX7 Polarity	PIX7 Frequency	PIX7 Activity During SH	PIX8 Activity	PIX8 Polarity	PIX8 Frequency	PIX8 Activity During SH
00110	Line Clamp Enable	0000 0000	PIX8 Line Clamp Enable	PIX7 Line Clamp Enable	PIX6 Line Clamp Enable	PIX5 Line Clamp Enable	PIX4 Line Clamp Enable	PIX3 Line Clamp Enable	PIX2 Line Clamp Enable	PIX1 Line Clamp Enable
00111	PIX1 Start	0000 0000	Reserved	MSB						LSB
01000	PIX1 End	0001 0101	Reserved	MSB						LSB
01001										
01010	PIX2 Start	0000 0000	Reserved	MSB						LSB
01011	PIX2 End	0001 0101	Reserved	MSB						LSB
01100										
01101	PIX3 Start	0000 1011	Reserved	MSB						LSB
01110	PIX3 End	0000 1101	Reserved	MSB						LSB
01111										
10000	PIX4 Start	0001 0000	Reserved	MSB						LSB
10001	PIX4 End	0001 0011	Reserved	MSB						LSB
10010										
10011	PIX5 Start	0000 0000	Reserved	MSB						LSB
10100	PIX5 End	0000 0000	Reserved	MSB						LSB
10101										
10110	PIX6 Start	0000 0000	Reserved	MSB						LSB
10111	PIX6 End	0000 0000	Reserved	MSB						LSB
11000										

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Table 12. (continued)

Address (Binary)	RegisterTitle (Mnemonic)	Default (Binary)	Register/Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11001	PIX7 Start	0000 0000	Reserved	MSB						LSB
11010	PIX7 End	0000 0000	Reserved	MSB						LSB
11011										
11100	PIX8 Start	0000 0000	Reserved	MSB						LSB
11101	PIX8 End	0000 0000	Reserved	MSB						LSB
11110	CMOS Data Mode Status Bit Enable	0000 0000	Reserved		CLK10/ CLKOUT	CLK9/ CB[4]	CLK8/ CB[3]	CLK7/ CB[2]	CLK6/ CB[1]	CLK5/ CB[0]
11111	Page Register	0000 0000	Reserved (program all zeros)					LSB+2	LSB+1	LSB

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PAGE 3 REGISTER TABLE - CCD/CIS TIMING GENERATOR CONTROL 2

Table 13.

Address (Binary)	Register Title (Mnemonic)	Default (Binary)	Register/Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Note: The active register page is selected by writing the desired value to the page select register 1Fh. This register is mirrored on all register pages.										
Page 3	Page Register 1F = 0000 0011									
00000	Output Mapping CLK1/CLK2	0000 0000	Output Mapping for CLK1 Pin				Output Mapping for CLK2 Pin			
00001	Output Mapping CLK3/CLK4	0000 0000	Output Mapping for CLK3 Pin				Output Mapping for CLK4 Pin			
00010	Output Mapping CLK5/CLK6	0000 0000	Output Mapping for CLK5 Pin				Output Mapping for CLK6 Pin			
00011	Output Mapping CLK7/CLK8	0000 0000	Output Mapping for CLK7 Pin				Output Mapping for CLK9 Pin			
00100	Output Mapping CLK9/(CLKOUT/ CLK10)	0000 0000	Output Mapping for CLK9 Pin				Output Mapping for CLKOUT/CLK10 Pin			
00101	Illumination Mode	0000 0000	$LAMP_R$ Normal State	$LAMP_G$ Normal State	$LAMP_B$ Normal State	LampIR1 Normal State	LampIR2 Normal State	Reserved		SH/LAMP Overlap Enable
00110	Line 1 Lamp Selection	0000 0000				Red Lamp Enable	Green Lamp Enable	Blue Lamp Enable	IR1 Lamp Enable	IR2 Lamp Enable
00111	Line 2 Lamp Selection	0000 0000				Red Lamp Enable	Green Lamp Enable	Blue Lamp Enable	IR1 Lamp Enable	IR2 Lamp Enable
01000	Line 3 Lamp Selection	0000 0000				Red Lamp Enable	Green Lamp Enable	Blue Lamp Enable	IR1 Lamp Enable	IR2 Lamp Enable
01001	Line 4 Lamp Selection	0000 0000				Red Lamp Enable	Green Lamp Enable	Blue Lamp Enable	IR1 Lamp Enable	IR2 Lamp Enable
01010	Line 5 Lamp Selection	0000 0000				Red Lamp Enable	Green Lamp Enable	Blue Lamp Enable	IR1 Lamp Enable	IR2 Lamp Enable
01011	$LAMP_R$ On - MSB	0000 0000	Reserved			SH_OR Enable	MSB			
01100	$LAMP_R$ On - LSB	0001 0001								LSB
01101	$LAMP_R$ Off - MSB	0000 0011	Reserved				MSB			
01110	$LAMP_R$ Off - LSB	0000 0110								LSB
01111	$LAMP_G$ On - MSB	0000 0000	Reserved			SH_OR Enable	MSB			
010000	$LAMP_G$ On - LSB	0001 0010								LSB
10001	$LAMP_G$ Off - MSB	0000 0011	Reserved				MSB			
10010	$LAMP_G$ Off - LSB	0000 0000								LSB

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Table 13. (continued)

Address (Binary)	Register Title (Mnemonic)	Default (Binary)	Register/Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10011	$LAMP_B$ On - MSB	0000 0000	Reserved			SH_OR Enable	MSB			
10100	$LAMP_B$ On - LSB	0001 0011								LSB
10101	$LAMP_B$ Off - MSB	0000 0011	Reserved				MSB			
10110	$LAMP_B$ Off - LSB	0011 0000								LSB
10111	$LAMP_{IR1}$ On - MSB	0000 0000	Reserved			SH_OR Enable	MSB			
11000	$LAMP_{IR1}$ On - LSB	0001 0100								LSB
11001	$LAMP_{IR1}$ Off - MSB	0000 0011	Reserved				MSB			
11010	$LAMP_{IR1}$ Off - LSB	0011 0000								LSB
11011	$LAMP_{IR2}$ On - MSB	0000 0000	Reserved			SH_OR Enable	MSB			
11100	$LAMP_{IR2}$ On - LSB	0001 0101								LSB
11101	$LAMP_{IR2}$ Off - MSB	0000 0011	Reserved				MSB			
11110	$LAMP_{IR2}$ Off - LSB	0011 0000								LSB
11111	Page Register	0000 0000	Reserved (program all zeros)					LSB+2	LSB+1	LSB

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PAGE 4 REGISTER TABLE - CCD/CIS TIMING GENERATOR CONTROL 3

Table 14.

Address (Binary)	Register Title (Mnemonic)	Default (Binary)	Register/Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Note: The active register page is selected by writing the desired value to the page select register 1Fh. This register is mirrored on all register pages.										
Page 4	Page Register 1F = 0000 0100									
00000	Mode On - MSB	0000 0010	Reserved				MSB			
00001	Mode On - LSB	0000 0000								LSB
00010	Mode Off - MSB	0000 0011	Reserved				MSB			
00011	Mode Off - LSB	0000 0001								LSB
00100	Optical Black Pixels Start	0000 0000	MSB							LSB
00101	Optical Black Pixels End	0000 0000	MSB							LSB
00110	Start of Valid Pixels - MSB	0000 0000	Reserved		MSB					
00111	Start of Valid Pixels - LSB	0000 0001								LSB
01000	End of Valid Pixels - MSB	0011 1111	Reserved		MSB					
01001	End of Valid Pixels - LSB	1111 1110								LSB
01010	Line End - MSB	0011 1111	Reserved		MSB					
01011	Line End - LSB	1111 1111								LSB
01100	Sample Timing Monitor 1	1111 1111								
01101	Sample Timing Monitor 2	1111 1111								
01110	Sample Timing Monitor 3	1111 1111								
01111	SH2/SH3 Control	0000 0000					SH3 Select	SH2 Select		
10000	PIX OR/NOR Control 1	0000 0000								
10001	PIX OR/NOR Control 2	0000 0000								
11111	Page Register	0000 0000	Reserved (program all zeros)					LSB+2	LSB+1	LSB

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PAGE 5 REGISTER TABLE - CCD/CIS TIMING GENERATOR CONTROL 4

Table 15.

Address (Binary)	Register Title (Mnemonic)	Default (Binary)	Register/Bit Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Note: The active register page is selected by writing the desired value to the page select register 1Fh. This register is mirrored on all register pages.										
Page 5	Page Register 1F = 0000 0101									
00000	PIX1/SH On Guardbands	0000 1111	PIX1 On Guardband							
00001	PIX1/SH Off Guardbands	0000 0111	PIX1 Off Guardband							
00010	PIX2/SH On Guardbands	0000 1111	PIX2 On Guardband							
00011	PIX2/SH Off Guardbands	0000 0111	PIX2 Off Guardband							
00100	PIX3/SH On Guardbands	0000 1111	PIX3 On Guardband							
00101	PIX3/SH Off Guardbands	0000 0111	PIX3 Off Guardband							
00110	PIX4/SH On Guardbands	0000 1111	PIX4 On Guardband							
00111	PIX4/SH Off Guardbands	0000 0111	PIX4 Off Guardband							
01000	PIX5/SH On Guardbands	0000 1111	PIX5 On Guardband							
01001	PIX5/SH Off Guardbands	0000 0111	PIX5 Off Guardband							
01010	PIX6/SH On Guardbands	0000 1111	PIX6 On Guardband							
01011	PIX6/SH Off Guardbands	0000 0111	PIX6 Off Guardband							
01100	PIX7/SH On Guardbands	0000 1111	PIX7 On Guardband							
01101	PIX7/SH Off Guardbands	0000 0111	PIX7 Off Guardband							
01110	PIX8/SH On Guardbands	0000 1111	PIX8 On Guardband							
01111	PIX8/SH Off Guardbands	0000 0111	PIX8 Off Guardband							
11111	Page Register	0000 0000	Reserved (program all zeros)					LSB+2	LSB+1	LSB

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REGISTER DEFINITION

Table 16.

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
Registers below are in register page 0.						
0	0 0000	Main Configuration 0	1111 0001	[7:0]	Main Configuration Register 0	
				[7:6]	Mode Select Bits.	
					11 Mode 3 (Default) (3 Channel Mode)	
					10 Mode 2 (2 Channel Mode)	
					01 Mode 1a (1 Channel Mode, 1 Channel sampled for all lines)	
					00 Mode 1b (3 Channel Line rate mode, 1 Channel sampled per line)	
				[5:4]	Color Select Bits. Used to determine the inputs sampled during a scan.	
					11 All three channels sampled (Default)	
					10 Mode 2 = OS_R & OS_B Mode 1 = OS_B	
					01 Mode 2 = OS_G & OS_B Mode 1 = OS_G	
					00 Mode 2 = OS_R & OS_G Mode 1 = OS_R	
				[3]	Color Order. Configures the sequence of the pixel processing.	
					0 Forward (default)	
					1 Reverse	
				[2:0]	Color Sequence Length. Used in Mode 1a only to determine the number of lines of colors sequenced during a scan.	
					111 Not valid	
					110 Not Valid	
					101 Five color (line) sequence	
					100 Four color (line) sequence	
					011 Three color (line) sequence	
					010 Two color (line) sequence	
					001 One color (line) sequence (Default)	
					000 Not Valid	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
0	0 0001	Main Configuration 1	0101 0000	[7:0]	Main Configuration Register 1	
				[7]	Source Follower Enable.	
					0 Disable (Default)	
					1 Enable	
				[6]	Input Bias Enable. Enables the Input Bias Resistor ladder.	
					0 Disable	
					1 Enable (Default)	
				[5]	Input Polarity. Configures the polarity mode of the input signal.	
					0 Negative going input relative to reference (Default)	
					1 Positive going input relative to reference	
				[4]	Sampling Mode Select.	
					0 Sample and Hold Mode	
					1 Correlated Double Sampling Mode (Default)	
				[3]	Output Format.	
					0 LVDS (Default)	
					1 CMOS	
				[2]	PIXCLK/ADCCLK Configuration. Selects appropriate multiplier for given input clock frequency.	
					Mode 3: ADC Frequency = 3x Pixel Frequency	
					Mode 2: ADC Frequency = 2x Pixel Frequency	
					Mode 1: ADC Frequency = 1x Pixel Frequency	
					0 ADCCLK User supplies ADC rate clock, LM98714 performs no multiplication	
					1 PIXCLK User supplies Pixel rate clock, LM98714 performs clock multiplication	
					Mode 3: PIXCLK internally multiplied by 3 to get ADC clock	
					Mode 2: PIXCLK internally multiplied by 2 to get ADC clock	
					Mode 1: PIXCLK = ADCCLK. This bit is not used for Mode 1	
				[1:0]	Pixel Phase Clock Select. Coarse adjustment for Pixel phase relative to INCLK. Useful in systems where Pixel inputs arrive with significant delay relative to INCLK.	
					00 PIXPHASE0. Pixel phase aligned with INCLK	
					01 PIXPHASE1. Pixel phase delayed by ($T_{ADC\ Clock}$* 3/7)	
					10 PIXPHASE2. Pixel phase delayed by ($T_{ADC\ Clock}$)	
					11 PIXPHASE3. Pixel phase delayed by ($T_{ADC\ Clock}$ * (1 + 3/7))	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
0	0 0010	Main Configuration 2	0000 0000	[7:0]	Main Configuration 2	
				[7:6]	Not Used	
				[5]	$\overline{\text{Active}}$/Standby	
				[4]	Gain Mode Select. Selects either a 1x or 2x gain mode in the CDS/Sample/Hold Block.	
					0 1x Gain in the CDS/Sample/Hold Block (Default)	
					1 2x Gain in the CDS/Sample/Hold Block	
				[3]	Output Enable. Enables the Data Output pins.	
					0 Disabled (Default)	
					1 Enable	
				[2]	Powerdown	
					0 Device fully powered (Default)	
					1 Powerdown. Power down of major analog blocks	
				[1]	Software Reset. Performs a system reset when set to a 1. Self clearing.	
				[0]	Start Scan (BOS)	
					0 Ready (Default)	
					1 Start Scan. Control bit is self clearing	
0	0 0011	Main Configuration 3	0000 0111	[7:0]	Main Configuration 3	
				[7:4]	Not Used	
				[3]	Processing Channel Override. Used in Mode 1 to determine the analog processing path for the selected inputs.	
					0 Multiplex all selected inputs into the Red Channel analog path (Default)	
					1 Process each selected input thru its respective analog path	
				[2:0]	Reserved Set to 111	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
0	0 0100	Main Configuration 4	0000 0000	[7:0]	Main Configuration 4	
				[7:4]	Not Used	
				[3]	Upcount Enable	
				[2:0]	LVDS Test Mode. Activates LVDS test pattern output (when in LVDS output mode only).	
					000 Normal operation, no test pattern output (Default)	
					001 Test pattern 1: Alternating pattern between 0x155555 and 0x0AAAAA	
					010 Test pattern 2: If Upcount Enable Bit set, count from 21h000000 to 21h 1FFFFF	
					011 Test pattern 3. Output Static Count value found represented by the three Upcounter Registers found on page 0	
					Reg 0x14 Bits[4:0] = Count Values 5 MSBs	
					Reg 0x13 Bits[7:0] = Count Values 8 Middle Bits	
					Reg 0x12 Bits[7:0] = Count Values 8 LSBs	
0	0 0101	Input Clamp Control	0000 0000	[7:0]	Input Clamp Control (CLPIN) Configuration Register	
				[7:4]	Reserved	
				[3:2]	Auto CLPIN Width. Width in Pixels of the Auto generated CLPIN pulse.	
					00 4 Pixels (Default)	
					01 8 Pixels	
					10 16 Pixels	
					11 32 Pixels	
				[1]	Auto CLPIN Enable.	
					0 Auto CLPIN Disabled	
					CLPIN Pulse generation Disabled (Default)	
					1 Auto CLPIN	
					CLPIN generated internally with a programmable delay from SH	
				[0]	CLPIN Gating Enable.	
					0 Auto $CLPIN_{GATED}$ not gated by SAMPLE (default)	
					1 Auto $CLPIN_{GATED}$ gated by SAMPLE (= logical and of CLPIN and SAMPLE)	
0	0 0110	Auto CLPIN Position	0010 0111	[7:0]	Auto CLPIN Pulse Position Register	
				[7:0]	Auto CLPIN Pulse Position. Number of pixels in which Auto CLPIN pulse is delayed, relative to the falling edge of SH.	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
0	0 0111	VCLP Configuration	0010 0000	[7:0]	VCLP Configuration Register	
				[7:6]	Reserved	
				[5:4]	VCLP Reference Select.	
					00 External Bias (No Internal Connection to Ladder Resistors or DAC)	
					01 Internal VCLP DAC connection only	
					10 Internal Resistor Ladder connection only (Default)	
					11 Reserved	
				[3:0]	4 Bit nibble for VCLP Reference DAC value.	
0	0 1000	Black Level Clamp Control	0000 0000	[7:0]	Black Level Correction Circuitry Configuration Register	
				[7:6]	Line Averaging. Number of Lines that the correction loop will run. Line Counter is reset during any write to this register. A line beginning is defined by the SH pulse.	
					00 Infinite (Default)	
					01 15 Lines	
					10 31 Lines	
					11 63 Lines	
				[5:4]	Pixel Averaging. Number of Black Level Pixels averaged by the correction loop.	
					00 4 Pixels	
					01 8 Pixels	
					10 16 Pixels	
					11 32 Pixels	
				[3:2]	Offset Integration.	
					00 Divide by 8	
					01 Divide by 16	
					10 Divide by 32	
					11 Divide by 64	
				[1:0]	BLKCLP Mode Select. If Auto Black Clamp pulse is enabled, Offset DAC registers are read only.	
					00 Auto Black Clamp Circuitry Disabled (default)	
					01 Auto Black Clamp pulse delayed from falling edge of SH pulse	
					10 Auto Black Clamp pulse delayed from falling edge of CLPIN pulse	
					11 Reserved	
0	0 1001	Auto Black Level Clamp Position	0000 0000	[7:0]	Auto Black Level Clamp Position Register	
				[7]	Reserved	
				[6:0]	Black Level Clamp Position. Number of pixels in which Auto Black pulse is delayed, relative to selected trigger source.	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
0	0 1010	Target Black Level MSB	0010 0000	[7:0]	The 8 MSBs of the 10 Bit target output code for black pixels when using the Auto Black Level Correction loop.	
0	0 1011	Target Black Level LSB	0000 0000	[7:0]	The target output code for black pixels when using the Auto Black Level Correction loop	
				[7:2]	Reserved	
				[1:0]	The 2 LSBs of the 10 Bit target output code for black pixels when using the Auto Black Level Correction loop.	
0	0 1100	OS_R CLAMP Control	0000 0000	[7:0]		
				[7:5]	Not Used	
				[4:0]	$CLAMP_R$ Position. A value of 0 will force the position of this pulse to be at the mode dependant default.	
0	0 1101	OS_G CLAMP Control	0000 0000	[7:0]		
				[7:5]	Not Used	
				[4:0]	$CLAMP_G$ Position. A value of 0 will force the position of this pulse to be at the mode dependant default.	
0	0 1110	OS_B CLAMP Control	0000 0000	[7:0]		
				[7:5]	Not Used	
				[4:0]	$CLAMP_B$ Position. A value of 0 will force the position of this pulse to be at the mode dependant default.	
0	0 1111	OS R SAMPLE Control	0000 0000	[7:0]		
				[7]	Not Used	
				[6:0]	$SAMPLE_R$ Position. A value of 0 will force the position of this pulse to be at the mode dependant default.	
0	1 0000	OS_G SAMPLE Control	0000 0000	[7:0]		
				[7]	Not Used	
				[6:0]	$SAMPLE_G$ Position. A value of 0 will force the position of this pulse to be at its mode dependant default.	
0	1 0001	OS_B SAMPLE Control	0000 0000	[7:0]		
				[7]	Not Used	
				[6:0]	$SAMPLE_B$ Position. A value of 0 will force the position of this pulse to be at its mode dependant default.	
0	1 1111	Page Register	0000 0000	[7:0]	Used to select desired page of registers being accessed.	
Registers below are in register page 1.						
1	0 0000	Color 1 PGA	0101 0100	[7:0]	The eight bit byte selected by the 5:1 PGA MUX in Mode 1a during Color 1 lines.	
					In Mode 1b, Mode 2 or Mode 3, the register used to define the PGA setting for the OS_R input.	
1	0 0001	Color 2 PGA	0101 0100	[7:0]	The eight bit byte selected by the 5:1 PGA MUX in Mode 1a during Color 2 lines.	
					In Mode 1b, Mode 2 or Mode 3, the register used to define the PGA setting for the OS_G input.	
1	0 0010	Color 3 PGA	0101 0100	[7:0]	The eight bit byte selected by the 5:1 PGA MUX in Mode 1a during Color 3 lines.	
					In Mode 1b, Mode 2 or Mode 3, the register used to define the PGA setting for the OS_B input.	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
1	0 0011	Color 4 PGA	0101 0100	[7:0]	The eight bit byte selected by the 5:1 PGA MUX in Mode 1a during Color 4 lines.	
					Not used in Mode 1b, Mode 2 or Mode 3.	
1	0 0100	Color 5 PGA	0101 0100	[7:0]	The eight bit byte selected by the 5:1 PGA MUX in Mode 1a during Color 5 lines.	
					Not used in Mode 1b, Mode 2 or Mode 3.	
1	0 0101	Color 1 Black Level DAC MSB	1000 0000	[7:0]	The MSBs selected by the 5:1 DAC MUX in Mode 1a during Color 1 lines.	
					In Mode 1b/c, Mode 2 or Mode 3, the register used to define the DAC setting for the OS_R input. The DAC value is in offset Binary format.	
1	0 0110	Color 1 Black Level DAC LSB	0000 0000	[7:0]	Color 1 Black Level DAC LSB	
				[7:2]	Not Used	
				[1:0]	The LSBs selected by the 5:1 DAC MUX in Mode 1a during Color 1 lines.	
					In Mode 1b, Mode 2 or Mode 3, the register used to define the DAC setting for the OS_R input. The DAC value is in offset Binary format.	
1	0 0111	Color 2 Black Level DAC MSB	1000 0000	[7:0]	The MSBs selected by the 5:1 DAC MUX in Mode 1a during Color 2 lines.	
					In Mode 1b, Mode 2 or Mode 3, the register used to define the DAC setting for the OS_G input. The DAC value is in offset Binary format.	
1	0 1000	Color 2 Black Level DAC LSB	0000 0000	[7:0]	Color 2 Black Level DAC LSB	
				[7:2]	Not Used	
				[1:0]	The LSBs selected by the 5:1 DAC MUX in Mode 1a during Color 2 lines.	
					In Mode 1b, Mode 2 or Mode 3, the register used to define the DAC setting for the OS_G input. The DAC value is in offset Binary format.	
1	0 1001	Color 3 Black Level DAC MSB	1000 0000	[7:0]	The MSBs selected by the 5:1 DAC MUX in Mode 1a during Color 3 lines.	
					In Mode 1b, Mode 2 or Mode 3, the register used to define the DAC setting for the OS_B input. The DAC value is in offset Binary format.	
1	0 1010	Color 3 Black Level DAC LSB	0000 0000	[7:0]	Color 3 Black Level DAC LSB	
				[7:2]	Not Used	
				[1:0]	The LSBs selected by the 5:1 DAC MUX in Mode 1a during Color 3 lines.	
					In Mode 1b, Mode 2 or Mode 3, the register used to define the DAC setting for the OS_B input. The DAC value is in offset Binary format.	
1	0 1011	Color 4 Black Level DAC MSB	1000 0000	[7:0]	The MSBs selected by the 5:1 DAC MUX in Mode 1a during Color 4 lines.	
					Not used in Mode 1b, Mode 2 or Mode 3. The DAC value is in offset Binary format.	
1	0 1100	Color 4 Black Level DAC LSB	0000 0000	[7:0]	Color 4 Black Level DAC LSB	
				[7:2]	Not Used	
				[1:0]	The LSBs selected by the 5:1 DAC MUX in Mode 1a during Color 4 lines.	
					Not used in Mode 1b, Mode 2 or Mode 3. The DAC value is in offset Binary format.	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
1	0 1101	Color 5 Black Level DAC MSB	1000 0000	[7:0]	The MSBs selected by the 5:1 DAC MUX in Mode 1a during Color 5 lines.	
					Not used in Mode 1b, Mode 2 or Mode 3. The DAC value is in offset Binary format.	
1	0 1110	Color 5 Black Level DAC LSB	0000 0000	[7:0]	Color 5 Black Level DAC LSB	
				[7:2]	Not Used	
				[1:0]	The LSBs selected by the 5:1 DAC MUX in Mode 1a during Color 5 lines.	
					Not used in Mode 1b/c, Mode 2 or Mode 3. The DAC value is in offset Binary format.	
1	0 1111	Color 1 Digital Offset	0100 0000	[7:0]	Color 1 Digital Offset	
				[7]	Not Used	
				[6:0]	The Digital Offset applied to the ADC result in Mode 1a during Color 1 lines.	
					In Mode 1b/c, Mode 2 or Mode 3, the register used to define the Digital Offset setting for the OS_R input. The DAC value is in offset Binary format.	
1	1 0000	Color 2 Digital Offset	0100 0000	[7:0]	Color 2 Digital Offset	
				[7]	Not Used	
				[6:0]	The Digital Offset applied to the ADC result in Mode 1a during Color 2 lines.	
					In Mode 1b/c, Mode 2 or Mode 3, the register used to define the DAC setting for the OS_G input. The DAC value is in offset Binary format.	
1	1 0001	Color 3 Digital Offset	0100 0000	[7:0]	Color 3 Digital Offset	
				[7]	Not Used	
				[6:0]	The Digital Offset applied to the ADC result in Mode 1a during Color 3 lines.	
					In Mode 1b/c, Mode 2 or Mode 3, the register used to define the DAC setting for the OS_B input. The DAC value is in offset Binary format.	
1	1 0010	Color 4 Digital Offset	0100 0000	[7:0]	Color 4 Digital Offset	
				[7]	Not Used	
				[6:0]	The Digital Offset applied to the ADC result in Mode 1a during Color 4 lines.	
					Not used in Mode 1b/c, Mode 2 or Mode 3. The DAC value is in offset Binary format.	
1	1 0011	Color 5 Digital Offset	0100 0000	[7:0]	Color 5 Digital Offset	
				[7]	Not Used	
				[6:0]	The Digital Offset applied to the ADC result in Mode 1a during Color 5 lines.	
					Not used in Mode 1b/c, Mode 2 or Mode 3. The DAC value is in offset Binary format.	
1	1 1111	Page Register	0000 0000	[7:0]	Used to select desired page of registers being accessed.	
Registers below are in register page 2.						

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
2	0 0000	SH Mode	0000 0000	[7]	SH Output Enable.	
					0 Enable SH Output	
					1 SH Output Tristate	
				[6]	SH Master/Slave Select.	
					0 External SH_R input. CCD Timing Generator runs in Slave mode, with SH triggered by an external pulse on the SH_R pin.	
					1 Auto generated SH. CCD Timing Generator runs in Master mode, with SH generated internally with a programmable period and width.	
				[5:4]	SH Output Mode.	
					00 SH Output = SH	
					01 SH Output = SH	
					10 SH Output = 0	
					11 SH Output = 1	
				[3:0]	SH Delay from SH_R	
					Additional delay	
2	0 0001	SH Pulse Width	0010 0111	[7:0]	SH Pulse Width	
					SH Pulse Width = (2 * [7:0]) + 1	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
2	0 0010	PIX1/2 Control	1100 1000	[7]	PIX1 Activity	
					0 Disabled	
					1 Enabled	
				[6]	PIX1 Polarity	
					0 Normal - Low when off	
					1 Inverted - High when off	
				[5]	PIX1 Frequency	
					0 Pixel Rate	
					1 1/2 Pixel Rate	
				[4]	PIX1 Activity During SH	
					0 Inactive	
					1 Active	
				[3]	PIX2 Activity	
					0 Disabled	
					1 Enabled	
				[2]	PIX2 Polarity	
					0 Normal - Low when off	
					1 Inverted - High when off	
				[1]	PIX2 Frequency	
					0 Pixel Rate	
					1 1/2 Pixel Rate	
				[0]	PIX2 Activity During SH	
					0 Inactive	
					1 Active	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
2	0 0011	PIX3/4 Control	1000 1000	[7]	PIX3 Activity	
					0 Disabled	
					1 Enabled	
				[6]	PIX3 Polarity	
					0 Normal - Low when off	
					1 Inverted - High when off	
				[5]	PIX3 Frequency	
					0 Pixel Rate	
					1 1/2 Pixel Rate	
				[4]	PIX3 Activity During SH	
					0 Inactive	
					1 Active	
				[3]	PIX4 Activity	
					0 Disabled	
					1 Enabled	
				[2]	PIX4 Polarity	
					0 Normal - Low when off	
					1 Inverted - High when off	
				[1]	PIX4 Frequency	
					0 Pixel Rate	
					1 1/2 Pixel Rate	
				[0]	PIX4 Activity During SH	
					0 Inactive	
					1 Active	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
2	0 0100	PIX5/6 Control	0000 0000	[7]	PIX5 Activity	
					0 Disabled	
					1 Enabled	
				[6]	PIX5 Polarity	
					0 Normal - Low when off	
					1 Inverted - High when off	
				[5]	PIX5 Frequency	
					0 Pixel Rate	
					1 1/2 Pixel Rate	
				[4]	PIX5 Activity During SH	
					0 Inactive	
					1 Active	
				[3]	PIX6 Activity	
					0 Disabled	
					1 Enabled	
				[2]	PIX6 Polarity	
					0 Normal - Low when off.	
					1 Inverted - High when off.	
				[1]	PIX6 Frequency	
					0 Pixel Rate	
					1 1/2 Pixel Rate	
				[0]	PIX6 Activity During SH	
					0 Inactive	
					1 Active	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
2	0 0101	PIX7/8 Control	0000 0000	[7]	PIX7 Activity	
					0 Disabled	
					1 Enabled	
				[6]	PIX7 Polarity	
					0 Normal - Low when off	
					1 Inverted - High when off	
				[5]	PIX7 Frequency	
					0 Pixel Rate	
					1 1/2 Pixel Rate	
				[4]	PIX7 Activity During SH	
					0 Inactive	
					1 Active	
				[3]	PIX8 Activity	
					0 Disabled	
					1 Enabled	
				[2]	PIX8 Polarity	
					0 Normal - Low when off	
					1 Inverted - High when off	
				[1]	PIX8 Frequency	
					0 Pixel Rate	
					1 1/2 Pixel Rate	
				[0]	PIX8 Activity During SH	
					0 Inactive	
					1 Active	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
2	0 0110	Line Clamp Enable	0000 0000	[7]	PIX8 Line Clamp Enable. Enables single Line Clamp pulse per line from PIX8.	
					0 Disabled. PIX generator functions as normal.	
					1 Enabled. PIX generates a single clock per line for Line Clamp function.	
				[6]	PIX7 Line Clamp Enable. Enables single Line Clamp pulse per line from PIX7.	
					0 Disabled. PIX generator functions as normal.	
					1 Enabled. PIX generates a single clock per line for Line Clamp function.	
				[5]	PIX6 Line Clamp Enable. Enables single Line Clamp pulse per line from PIX6.	
					0 Disabled. PIX generator functions as normal.	
					1 Enabled. PIX generates a single clock per line for Line Clamp function.	
				[4]	PIX5 Line Clamp Enable. Enables single Line Clamp pulse per line from PIX5.	
					0 Disabled. PIX generator functions as normal.	
					1 Enabled. PIX generates a single clock per line for Line Clamp function.	
					PIX4 Line Clamp Enable. Enables single Line Clamp pulse per line from PIX4.	
				[3]	0 Disabled. PIX generator functions as normal.	
					1 Enabled. PIX generates a single clock per line for Line Clamp function.	
					PIX3 Line Clamp Enable. Enables single Line Clamp pulse per line from PIX3.	
				[2]	0 Disabled. PIX generator functions as normal.	
					1 Enabled. PIX generates a single clock per line for Line Clamp function.	
					PIX2 Line Clamp Enable. Enables single Line Clamp pulse per line from PIX2.	
				[1]	0 Disabled. PIX generator functions as normal.	
					1 Enabled. PIX generates a single clock per line for Line Clamp function.	
					PIX1 Line Clamp Enable. Enables single Line Clamp pulse per line from PIX1.	
				[0]	0 Disabled. PIX generator functions as normal.	
					1 Enabled. PIX generates a single clock per line for Line Clamp function.	
2	0 0111	PIX1 Start	0000 0000	[7]	Reserved. Set to 0.	
				[6:0]	PIX1 on point. Defines when the PIX1 signal turns on within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	0 1000	PIX1 End	0001 0101	[7]	Reserved. Set to 0.	
				[6:0]	PIX1 off point. Defines when the PIX1 signal turns off within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	0 1010	PIX2 Start	0000 0000	[7]	Reserved. Set to 0.	
				[6:0]	PIX2 on point. Defines when the PIX2 signal turns on within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
2	0 1011	PIX2 End	0001 0101	[7]	Reserved. Set to 0.	
				[6:0]	PIX2 off point. Defines when the PIX2 signal turns off within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	0 1101	PIX3 Start	0000 1011	[7]	Reserved. Set to 0.	
				[6:0]	PIX3 on point. Defines when the PIX3 signal turns on within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	0 1110	PIX3 End	0000 1101	[7]	Reserved. Set to 0.	
				[6:0]	PIX3 off point. Defines when the PIX3 signal turns off within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	1 0000	PIX4 Start	0001 0000	[7]	Reserved. Set to 0.	
				[6:0]	PIX4 on point. Defines when the PIX4 signal turns on within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	1 0001	PIX4 End	0001 0011	[7]	Reserved. Set to 0.	
				[6:0]	PIX4 off point. Defines when the PIX4 signal turns off within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	1 0011	PIX5 Start	0000 0000	[7]	Reserved. Set to 0.	
				[6:0]	PIX5 on point. Defines when the PIX5 signal turns on within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	1 0100	PIX5 End	0000 0000	[7]	Reserved. Set to 0.	
				[6:0]	PIX5 off point. Defines when the PIX5 signal turns off within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	1 0110	PIX6 Start	0000 0000	[7]	Reserved. Set to 0.	
				[6:0]	PIX6 on point. Defines when the PIX6 signal turns on within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	1 0111	PIX6 End	0000 0000	[7]	Reserved. Set to 0.	
				[6:0]	PIX6 off point. Defines when the PIX6 signal turns off within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	1 1001	PIX7 Start	0000 0000	[7]	Reserved. Set to 0.	
				[6:0]	PIX7 on point. Defines when the PIX7 signal turns on within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	1 1010	PIX7 End	0000 0000	[7]	Reserved. Set to 0.	
				[6:0]	PIX7 off point. Defines when the PIX7 signal turns off within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	1 1100	PIX8 Start	0000 0000	[7]	Reserved. Set to 0.	
				[6:0]	PIX8 on point. Defines when the PIX8 signal turns on within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
2	1 1101	PIX8 End	0000 0000	[7]	Reserved. Set to 0	
				[6:0]	PIX8 off point. Defines when the PIX8 signal turns off within the pixel period. Can be set to any available edge within the pixel period. (For 1/2 frequency signals, the count can be any available edge within 2 pixel periods)	
2	1 1110	CMOS Data Mode Status Bit Enable	0000 0000	[7:6]	Reserved. Set to 000	
					When mapping the CLK5 to CLK10 pins as either CLKOUT or CB outputs, the Sample Timing Monitor 1 (Page 4, Register 0x0C) cannot be used.	
				[5]	0 - CLK10 mapped normally, 1- CLK10 = CLKOUT	
				[4]	0 - CLK9 mapped normally, 1- CLK9 = CB[4] status bit	
				[3]	0 - CLK8 mapped normally, 1- CLK8 = CB[3] status bit	
				[2]	0 - CLK7 mapped normally, 1- CLK7 = CB[2] status bit	
				[1]	0 - CLK6 mapped normally, 1- CLK6 = CB[1] status bit	
				[0]	0 - CLK5 mapped normally, 1- CLK5 = CB[0] status bit	
2	1 1111	Page Register	0000 0000	[7:0]	Used to select desired page of registers being accessed.	
Registers below are in register page 3.						
3	0 0000	Output Mapping CLK1/CLK 2	0000 0000	These registers set which timing signal is present on the respective CLKn output pin.		
				[7:4] CLK 1	Setting CLKn =	
					0000 Tristate	
					0001 PIX1	
					0010 PIX2	
					0011 PIX3	
					0100 PIX4	
					0101 PIX5	
					0110 PIX6	
					0111 PIX7	
				[3:0] CLK 2	1000 PIX8	
					1001 $LAMP_R$	
					1010 $LAMP_G$	
					1011 $LAMP_B$	
					1100 LAMPIR1	
					1101 LAMPIR2	
					1110 MODE	
					1111 SH	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
3	0 0001	Output Mapping CLK3/CLK 4	0000 0000	These registers set which timing signal is present on the respective CLKn output pin.		
				[7:4] CLK 3	Setting CLKn =	
					0000 Tristate	
					0001 PIX1	
					0010 PIX2	
					0011 PIX3	
					0100 PIX4	
					0101 PIX5	
					0110 PIX6	
					0111 PIX7	
				[3:0] CLK 4	1000 PIX8	
					1001 $LAMP_R$	
					1010 $LAMP_G$	
					1011 $LAMP_B$	
					1100 LAMPIR1	
					1101 LAMPIR2	
					1110 MODE	
					1111 SH	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
3	0 0010	Output Mapping CLK5/CLK 6	0000 0000	These registers set which timing signal is present on the respective CLKn output pin.		
				[7:0] CLK 5	Setting CLKn =	
					0000 Tristate	
					0001 PIX1	
					0010 PIX2	
					0011 PIX3	
					0100 PIX4	
					0101 PIX5	
					0110 PIX6	
					0111 PIX7	
				[3:0] CLK 6	1000 PIX8	
					1001 $LAMP_R$	
					1010 $LAMP_G$	
					1011 $LAMP_B$	
					1100 LAMPIR1	
					1101 LAMPIR2	
					1110 MODE	
					1111 SH	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
3	0 0011	Output Mapping CLK7/CLK 8	0000 0000	These registers set which timing signal is present on the respective CLKn output pin.		
				[7:0] CLK 7	Setting CLKn =	
					0000 Tristate	
					0001 PIX1	
					0010 PIX2	
					0011 PIX3	
					0100 PIX4	
					0101 PIX5	
					0110 PIX6	
					0111 PIX7	
				[3:0] CLK 8	1000 PIX8	
					1001 $LAMP_R$	
					1010 $LAMP_G$	
					1011 $LAMP_B$	
					1100 LAMPIR1	
					1101 LAMPIR2	
					1110 MODE	
					1111 SH	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
3	0 0100	Output Mapping CLK9/CLK 10	0000 0000	These registers set which timing signal is present on the respective CLKn output pin.		
				[7:4] CLK 9	Setting CLKn =	
					0000 Tristate	
					0001 PIX1	
					0010 PIX2	
					0011 PIX3	
					0100 PIX4	
					0101 PIX5	
					0110 PIX6	
					0111 PIX7	
				[3:0] CLK 10	1000 PIX8	
					1001 $LAMP_R$	
					1010 $LAMP_G$	
					1011 $LAMP_B$	
					1100 LAMPIR1	
					1101 LAMPIR2	
					1110 MODE	
					1111 SH	
3	0 0101	Illumination Mode (see also AFE color modes)	0000 0000	[7]	$LAMP_R$ Normal State	
					0 = Low, 1 = High	
				[6]	$LAMP_G$ Normal State	
					0 = Low, 1 = High	
				[5]	$LAMP_B$ Normal State	
					0 = Low, 1 = High	
				[4]	LampIR1 Normal State	
					0 = Low, 1 = High	
				[3]	LampIR2 Normal State	
					0 = Low, 1 = High	
				[2:1]	Reserved	
				[0]	SH/LAMP Overlap Enable	
					0 Disabled	
					1 Overlap Enabled	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
3	0 0110	Line 1 Lamp Selection	0000 0000	[7:5]	Reserved. Set to 000	
				[4]	Red Lamp Enable	
					0 Red Disabled	
					1 Red Enabled	
				[3]	Green Lamp Enable	
					0 Green Disabled	
					1 Green Enabled	
				[2]	Blue Lamp Enable	
					0 Blue Disabled	
					1 Blue Enabled	
				[1]	IR1 Lamp Enable	
					0 IR1 Disabled	
					1 IR1 Enabled	
				[0]	IR2 Lamp Enable	
					0 IR2 Disabled	
					1 IR2 Enabled	
3	0 0111	Line 2 Lamp Selection	0000 0000	[7:5]	Reserved. Set to 000	
				[4]	Red Lamp Enable	
					0 Red Disabled	
					1 Red Enabled	
				[3]	Green Lamp Enable	
					0 Green Disabled	
					1 Green Enabled	
				[2]	Blue Lamp Enable	
					0 Blue Disabled	
					1 Blue Enabled	
				[1]	IR1 Lamp Enable	
					0 IR1 Disabled	
					1 IR1 Enabled	
				[0]	IR2 Lamp Enable	
					0 IR2 Disabled	
					1 IR2 Enabled	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
3	0 1000	Line 3 Lamp Selection	0000 0000	[7:5]	Reserved. Set to 000	
				[4]	Red Lamp Enable	
					0 Red Disabled	
					1 Red Enabled	
				[3]	Green Lamp Enable	
					0 Green Disabled	
					1 Green Enabled	
				[2]	Blue Lamp Enable	
					0 Blue Disabled	
					1 Blue Enabled	
				[1]	IR1 Lamp Enable	
					0 IR1 Disabled	
					1 IR1 Enabled	
				[0]	IR2 Lamp Enable	
					0 IR2 Disabled	
					1 IR2 Enabled	
3	0 1001	Line 4 Lamp Selection	0000 0000	[7:5]	Reserved. Set to 000	
				[4]	Red Lamp Enable	
					0 Red Disabled	
					1 Red Enabled	
				[3]	Green Lamp Enable	
					0 Green Disabled	
					1 Green Enabled	
				[2]	Blue Lamp Enable	
					0 Blue Disabled	
					1 Blue Enabled	
				[1]	IR1 Lamp Enable	
					0 IR1 Disabled	
					1 IR1 Enabled	
				[0]	IR2 Lamp Enable	
					0 IR2 Disabled	
					1 IR2 Enabled	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
3	0 1010	Line 5 Lamp Selection	0000 0000	[7:5]	Reserved. Set to 000	
				[4]	Red Lamp Enable	
					0 Red Disabled	
					1 Red Enabled	
				[3]	Green Lamp Enable	
					0 Green Disabled	
					1 Green Enabled	
				[2]	Blue Lamp Enable	
					0 Blue Disabled	
					1 Blue Enabled	
				[1]	IR1 Lamp Enable	
					0 IR1 Disabled	
					1 IR1 Enabled	
				[0]	IR2 Lamp Enable	
					0 IR2 Disabled	
					1 IR2 Enabled	
3	0 1011	$LAMP_R$ On MSB	0000 0000	[7:5]	Reserved. Set to 000	
				[4]	$LAMP_R$ SH_OR Enable	
					0 No ORing	
					1 $LAMP_R$ uses SH_OR function	
				[3:0]	$LAMP_R$ On Time Most Significant Bits	
					This selects the pixel count at which the $LAMP_R$ output goes high.	
3	0 1100	$LAMP_R$ On LSB	0001 0001	[7:0]	$LAMP_R$ On Time Least Significant Byte	
					This selects the pixel count at which the $LAMP_R$ output goes high.	
3	0 1101	$LAMP_R$ Off MSB	0000 0011	[7:4]	Reserved. Set to 0000	
				[3:0]	$LAMP_R$ Off Time Most Significant Bits	
					This selects the pixel count at which the $LAMP_R$ output goes low.	
3	0 1110	$LAMP_R$ Off LSB	0000 0110	[7:0]	$LAMP_R$ Off Time Least Significant Byte	
					This selects the pixel count at which the $LAMP_R$ output goes low.	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
3	0 1111	$LAMP_G$ On MSB	0000 0000	[7:5]	Reserved. Set to 000	
				[4]	$LAMP_G$ SH_OR Enable.	
					0 No ORing	
					1 $LAMP_G$ uses SH_OR function	
				[3:0]	$LAMP_G$ On Time Most Significant Bits.	
					This selects the pixel count at which the $LAMP_R$ output goes high.	
3	1 0000	$LAMP_G$ On LSB	0001 0010	[7:0]	$LAMP_G$ On Time Least Significant Byte	
					This selects the pixel count at which the $LAMP_R$ output goes high.	
3	1 0001	$LAMP_G$ Off MSB	0000 0011	[7:4]	Reserved. Set to 0000	
				[3:0]	$LAMP_G$ Off Time Most Significant Bits	
					This selects the pixel count at which the $LAMP_R$ output goes low.	
3	1 0010	$LAMP_G$ Off LSB	0000 0000	[7:0]	$LAMP_G$ Off Time Least Significant Byte	
					This selects the pixel count at which the $LAMP_R$ output goes low.	
3	1 0011	$LAMP_B$ On MSB	0000 0000	[7:5]	Reserved. Set to 000	
				[4]	$LAMP_B$ SH_OR Enable	
					0 No ORing	
					1 $LAMP_B$ uses SH_OR function	
				[3:0]	$LAMP_B$ On Time Most Significant Bits	
					This selects the pixel count at which the $LAMP_R$ output goes high.	
3	1 0100	$LAMP_B$ On LSB	0001 0011	[7:0]	$LAMP_B$ On Time Least Significant Byte	
					This selects the pixel count at which the $LAMP_R$ output goes high.	
3	1 0101	$LAMP_B$ Off MSB	0000 0011	[7:4]	Reserved. Set to 0000	
				[3:0]	$LAMP_B$ Off Time Most Significant Bits	
					This selects the pixel count at which the $LAMP_R$ output goes low.	
3	1 0110	$LAMP_B$ Off LSB	0011 0000	[7:0]	$LAMP_B$ Off Time Least Significant Byte	
					This selects the pixel count at which the $LAMP_R$ output goes low.	
3	1 0111	LAMPIR1 On MSB	0000 0000	[7:5]	Reserved. Set to 000	
				[4]	LAMPIR1 SH_OR Enable	
					0 No ORing	
					1 LAMPIR1 uses SH_OR function	
				[3:0]	LAMPIR1 On Time Most Significant Bits	
					This selects the pixel count at which the $LAMP_R$ output goes high.	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
3	1 1000	LAMPIR1 On LSB	0001 0100	[7:0]	LAMPIR1 On Time Least Significant Byte	
					This selects the pixel count at which the $LAMP_R$ output goes high.	
3	1 1001	LAMPIR1 Off MSB	0000 0011	[7:4]	Reserved. Set to 0000	
				[3:0]	LAMPIR1 Off Time Most Significant Bits	
					This selects the pixel count at which the $LAMP_R$ output goes low.	
3	1 1010	LAMPIR1 Off LSB	0011 0000	[7:0]	LAMPIR1 Off Time Least Significant Byte	
					This selects the pixel count at which the $LAMP_R$ output goes low.	
3	1 1011	LAMPIR2 On MSB	0000 0000	[7:5]	Reserved. Set to 000	
				[4]	LAMPIR2 SH_OR Enable.	
					0 No ORing	
					1 LAMPIR2 uses SH_OR function	
				[3:0]	LAMPIR2 On Time Most Significant Bits.	
					This selects the pixel count at which the $LAMP_R$ output goes high.	
3	1 1100	LAMPIR2 On LSB	0001 0101	[7:0]	LAMPIR2 On Time Least Significant Byte	
					This selects the pixel count at which the $LAMP_R$ output goes high.	
3	1 1101	LAMPIR2 Off MSB	0000 0011	[7:4]	Reserved. Set to 0000	
				[3:0]	LAMPIR2 Off Time Most Significant Bits	
					This selects the pixel count at which the $LAMP_R$ output goes low.	
3	1 1110	LAMPIR2 Off LSB	0011 0000	[7:0]	LAMPIR2 Off Time Least Significant Byte	
					This selects the pixel count at which the $LAMP_R$ output goes low.	
3	1 1111	Page Register	0000 0000	[7:0]	Used to select desired page of registers being accessed.	
Registers below are in register page 4.						
4	0 0000	Mode On MSB	0000 0010	[7:4]	Reserved. Set to 0000	
				[3:0]	Mode On Time Most Significant Bits	
					This selects the pixel count at which the Mode output goes high.	
4	0 0001	Mode On LSB	0000 0000	[7:0]	Mode On Time Least Significant Byte	
					This selects the pixel count at which the Mode output goes high.	
4	0 0010	Mode Off MSB	0000 0011	[7:4]	Reserved. Set to 0000	
				[3:0]	Mode Off Time Most Significant Bits	
					This selects the pixel count at which the Mode output goes low.	
4	0 0011	Mode Off LSB	0000 0001	[7:0]	Mode Off Time Least Significant Byte	
					This selects the pixel count at which the Mode output goes low.	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
4	0 0100	Optical Black Pixels Start	0000 0000	[7:0]	Starting point for optical black clamping	
					nnnnnnnn - n pixels (0-255)	
4	0 0101	Optical Black Pixels End	0000 0000	[7:0]	End point for optical black clamping	
					nnnnnnnn - n pixels (0-255)	
4	0 0110	Start of Valid Pixels - MSB	0000 0000	[7:6]	Reserved. Set to 00	
				[5:0]	Start of Valid Pixels - Most Significant Bits.	
					Selects the pixel count where the data status bits begin to indicate valid pixels.	
4	0 0111	Start of Valid Pixels - LSB	0000 0000	[7:0]	Start of Valid Pixels - Least Significant Bits.	
					Selects the pixel count where the data status bits begin to indicate valid pixels.	
4	0 1000	End of Valid Pixels - MSB	0011 1111	[7:6]	Reserved. Set to 00	
				[5:0]	End of Valid Pixels - Most Significant Bits.	
					Selects the pixel count where the data status bits stop indicating valid pixels.	
4	0 1001	End of Valid Pixels - LSB	1111 1110	[7:0]	End of Valid Pixels - Least Significant Bits.	
					Selects the pixel count where the data status bits stop indicating valid pixels.	
4	0 1010	Line End - MSB	0011 1111	[7:6]	Reserved. Set to 00.	
				[5:0]	Line End Value - Most Significant 6 Bits	
					Selects the pixel count where the current line is ended and the next one begins. Con trols the integration time of one line and the period between SH pulses.	
4	0 1011	Line End - LSB	1111 1111	[7:0]	Line End Value Least Significant Byte	
					Selects the pixel count where the current line is ended and the next one begins. Con trols the integration time of one line and the period between SH pulses.	
					n pixels (0 - 16383)	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
4	0 1100	Sample Timing Monitor 1	1111 1111	[7:0]	Enables Sample and Clamp timing signals to be observed on one of the sensor timing control outputs. This function overrides any other settings for sensor control signal mapping.	
					Important Note: Sample Timing Monitor 1 cannot be used if the CMOS Data Mode Status Bit Enable Register (Page 2, Register 0x1E) is being programmed to map CLKOUT to CLK10 or any Control Bit to CLK5-CLK9. Sample Timing Monitors 2 and 3 are not effected by this limitation.	
				[7:4]	Upper 4 bits select timing signal to be monitored.	
					0000 Sample Red	
					0001 Clamp Red	
					0010 Sample Green	
					0011 Clamp Green	
					0100 Sample Blue	
					0101 Clamp Blue	
					1111 No signal monitored	
				[3:0]	Lower 4 bits select which output pin is used as a monitor.	
					0000 CLK1	
					0001 CLK2	
					0010 CLK3	
					0011 CLK4	
					0100 CLK5	
					0101 CLK6	
					0110 CLK7	
					0111 CLK8	
					1000 CLK9	
					1001 CLKOUT/CLK10	
					1111 All outputs normal	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
4	0 1101	Sample Timing Monitor 2	1111 1111	[7:0]	Enables Sample and Clamp timing signals to be observed on one of the sensor timing control outputs. This function overrides any other settings for sensor control signal mapping.	
				[7:4]	Upper 4 bits select timing signal to be monitored.	
					0000 Sample Red	
					0001 Clamp Red	
					0010 Sample Green	
					0011 Clamp Green	
					0100 Sample Blue	
					0101 Clamp Blue	
					1111 No signal monitored	
				[3:0]	Lower 4 bits select which output pin is used as a monitor.	
					0000 CLK1	
					0001 CLK2	
					0010 CLK3	
					0011 CLK4	
					0100 CLK5	
					0101 CLK6	
					0110 CLK7	
					0111 CLK8	
					1000 CLK9	
					1001 CLKOUT/CLK10	
					1111 All outputs normal	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
4	0 1110	Sample Timing Monitor 3	1111 1111	[7:0]	Enables Sample and Clamp timing signals to be observed on one of the sensor timing control outputs. This function overrides any other settings for sensor control signal mapping.	
				[7:4]	Upper 4 bits select timing signal to be monitored.	
					0000 Sample Red	
					0001 Clamp Red	
					0010 Sample Green	
					0011 Clamp Green	
					0100 Sample Blue	
					0101 Clamp Blue	
					1111 No signal monitored	
				[3:0]	Lower 4 bits select which output pin is used as a monitor.	
					0000 CLK1	
					0001 CLK2	
					0010 CLK3	
					0011 CLK4	
					0100 CLK5	
					0101 CLK6	
					0110 CLK7	
					0111 CLK8	
					1000 CLK9	
					1001 CLKOUT/CLK10	
					1111 All outputs normal	
4	0 1111	SH2/SH3 Control	0000 0000	[7:0]	Controls the optional SH2 and SH3 output signals. These signals can override the Lamp IR1 and Lamp IR2 outputs if additional SH signals are required.	
				[7:4]	Not Used.	
				[3]	SH3 Output Select.	
					0 Lamp IR2 output is programmed from Lamp IR2 Generator	
					1 Lamp IR2 output is SH3	
				[2]	SH2 Output Select.	
					0 Lamp IR1 output is programmed from Lamp IR1 Generator	
					1 Lamp IR1 output is SH2	
				[1:0]	Not Used	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
4	1 0000	PIX OR/NOR Control 1	0000 0000	[7:0]	Controls the optional OR and NOR operations on the PIX generator outputs as described below. These signals can override the normal PIX generator outputs to pro vide OR and NOR functionality for uses such as Pixel Lumping. If multiple functions are selected, the order of priority from highest to lowest is PIX OR/NOR Control 1 Bit[0] to Bit [7], then PIX OR/NOR Control 2 Bit[0] to Bit[7] (i.e PIX OR/NOR Control 1 Bit[7] has a higher priority on the PIX5 output than PIX OR/NOR Control 2 Bit[0] or Bit[2]).	
					For reference purposes, the normal, unmodified PIX generator outputs are named pix1 through pix8 (lower case) and the final signal prior to the CLK pins are named PIX1 through PIX8 (upper case).	
				[0]	0 No effect (default); 1 PIX1 = ~(pix1 || pix2)	
				[1]	0 No effect (default); 1 PIX2 = (pix1 || pix2)	
				[2]	0 No effect (default); 1 PIX2 = ~(pix2 || pix3)	
				[3]	0 No effect (default); 1 PIX3 = (pix2 || pix3)	
				[4]	0 No effect (default); 1 PIX3 = ~(pix3 || pix4)	
				[5]	0 No effect (default); 1 PIX4 = (pix3 || pix4)	
				[6]	0 No effect (default); 1 PIX4 = ~(pix4 || pix5)	
				[7]	0 No effect (default); 1 PIX5 = (pix4 || pix5)	
4	1 0001	PIX OR/NOR Control 2	0000 0000	[7:0]	Controls the optional OR and NOR operations on the PIX generator outputs as described below. These signals can override the normal PIX generator outputs to pro vide OR and NOR functionality for uses such as Pixel Lumping. If multiple functions are selected, the order of priority from highest to lowest is PIX OR/NOR Control 1 Bit[0] to Bit [7], then PIX OR/NOR Control 2 Bit[0] to Bit[7] (i.e PIX OR/NOR Control 1 Bit[7] has a higher priority on the PIX5 output than PIX OR/NOR Control 2 Bit[0] or Bit[2]).	
					For reference purposes, the normal, unmodified PIX generator outputs are named pix1 through pix8 (lower case) and the final signal prior to the CLK pins are named PIX1 through PIX8 (upper case).	
				[0]	0 No effect (default); 1 PIX5 = ~(pix5 || pix6)	
				[1]	0 No effect (default); 1 PIX6 = (pix5 || pix6)	
				[2]	0 No effect (default); 1 PIX5 = ~(pix4 || pix5 || pix6)	
				[3]	0 No effect (default); 1 PIX6 = (pix4 || pix5 || pix6)	
				[4]	0 No effect (default); 1 PIX7 = ~(pix3 || pix7 || pix8)	
				[5]	0 No effect (default); 1 PIX8 = (pix3 || pix7 || pix8)	
				[6]	0 No effect (default); 1 PIX7 = ~(pix7 || pix8)	
				[7]	0 No effect (default); 1 PIX8 = (pix7 || pix8)	
4	1 1111	Page Register	0000 0000	[7:0]	Used to select desired page of registers being accessed.	
Registers below are in register page 5.						
5	0 0000	PIX1/SH On Guardbands	0000 1111	[7:0]	PIX1 on guardband. Number of pixel periods from end of SH pulse to start of PIX1.	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
5	0 0001	PIX1/SH Off Guardbands	0000 0111	[7:0]	PIX1 off guardband. Number of pixel periods before start of SH pulse that PIX1 stops.	
5	0 0010	PIX2/SH On Guardbands	0000 1111	[7:0]	PIX2 on guardband. Number of pixel periods from end of SH pulse to start of PIX2.	
5	0 0011	PIX2/SH Off Guardbands	0000 0111	[7:0]	PIX2 off guardband. Number of pixel periods before start of SH pulse that PIX2 stops.	
5	0 0100	PIX3/SH On Guardbands	0000 1111	[7:0]	PIX3 on guardband. Number of pixel periods from end of SH pulse to start of PIX3.	
5	0 0101	PIX3/SH Off Guardbands	0000 0111	[7:0]	PIX3 off guardband. Number of pixel periods before start of SH pulse that PIX3 stops.	
5	0 0110	PIX4/SH On Guardbands	0000 1111	[7:0]	PIX4 on guardband. Number of pixel periods from end of SH pulse to start of PIX4.	
5	0 0111	PIX4/SH Off Guardbands	0000 0111	[7:0]	PIX4 off guardband. Number of pixel periods before start of SH pulse that PIX4 stops.	
5	0 1000	PIX5/SH On Guardbands	0000 1111	[7:0]	PIX5 on guardband. Number of pixel periods from end of SH pulse to start of PIX5.	
5	0 1001	PIX5/SH Off Guardbands	0000 0111	[7:0]	PIX5 off guardband. Number of pixel periods before start of SH pulse that PIX5 stops.	
5	0 1010	PIX6/SH On Guardbands	0000 1111	[7:0]	PIX6 on guardband. Number of pixel periods from end of SH pulse to start of PIX6.	

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Table 16. (continued)

Page	Address (Binary)	Register Title	Default (Binary)	Bit(s)	Description	
5	0 1011	PIX6/SH Off Guardbands	0000 0111	[7:0]	PIX6 off guardband. Number of pixel periods before start of SH pulse that PIX6 stops.	
5	0 1100	PIX7/SH On Guardbands	0000 1111	[7:0]	PIX7 on guardband. Number of pixel periods from end of SH pulse to start of PIX7.	
5	0 1101	PIX7/SH Off Guardbands	0000 0111	[7:0]	PIX7 off guardband. Number of pixel periods before start of SH pulse that PIX7 stops.	
5	0 1110	PIX8/SH On Guardbands	0000 1111	[7:0]	PIX8 on guardband. Number of pixel periods from end of SH pulse to start of PIX8.	
5	0 1111	PIX8/SH Off Guardbands	0000 0111	[7:0]	PIX8 off guardband. Number of pixel periods before start of SH pulse that PIX8 stops.	

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Changes from Original (October 2006) to Revision A **Page**

- Added content to complete full data sheet. 1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM98714BCMT/NOPB	ACTIVE	TSSOP	DGG	48	38	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	LM98714 BCMT	Samples
LM98714BCMTX/NOPB	ACTIVE	TSSOP	DGG	48	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	LM98714 BCMT	Samples
LM98714CCMT/NOPB	ACTIVE	TSSOP	DGG	48	38	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	LM98714 CCMT	Samples
LM98714CCMTX	NRND	TSSOP	DGG	48	1000	TBD	Call TI	Call TI	0 to 70	LM98714 CCMT	
LM98714CCMTX/NOPB	ACTIVE	TSSOP	DGG	48	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	LM98714 CCMT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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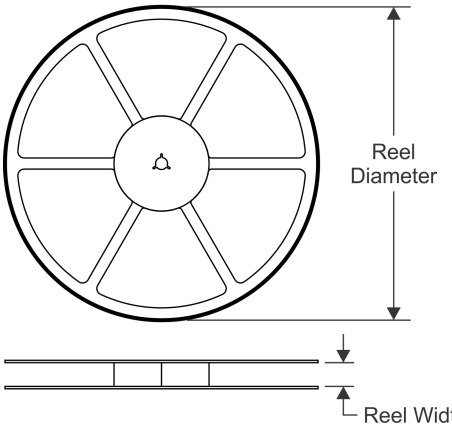
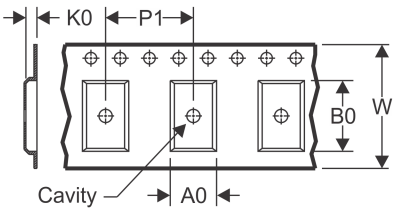
TAPE AND REEL INFORMATION

REEL DIMENSIONS

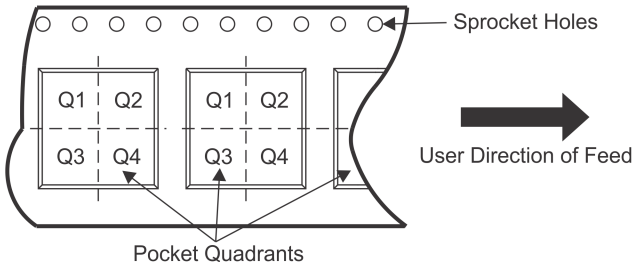


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

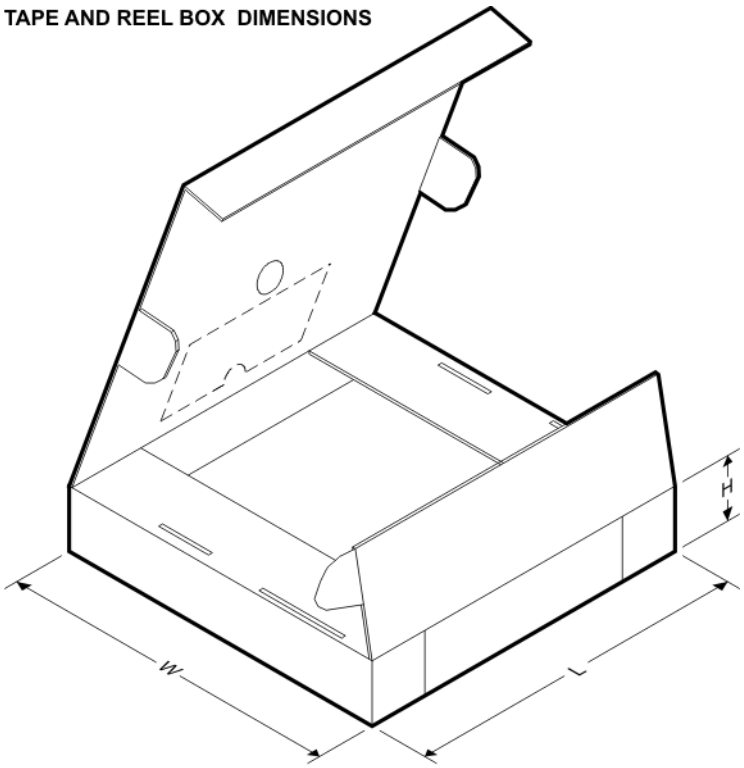
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM98714BCMTX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1
LM98714CCMTX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

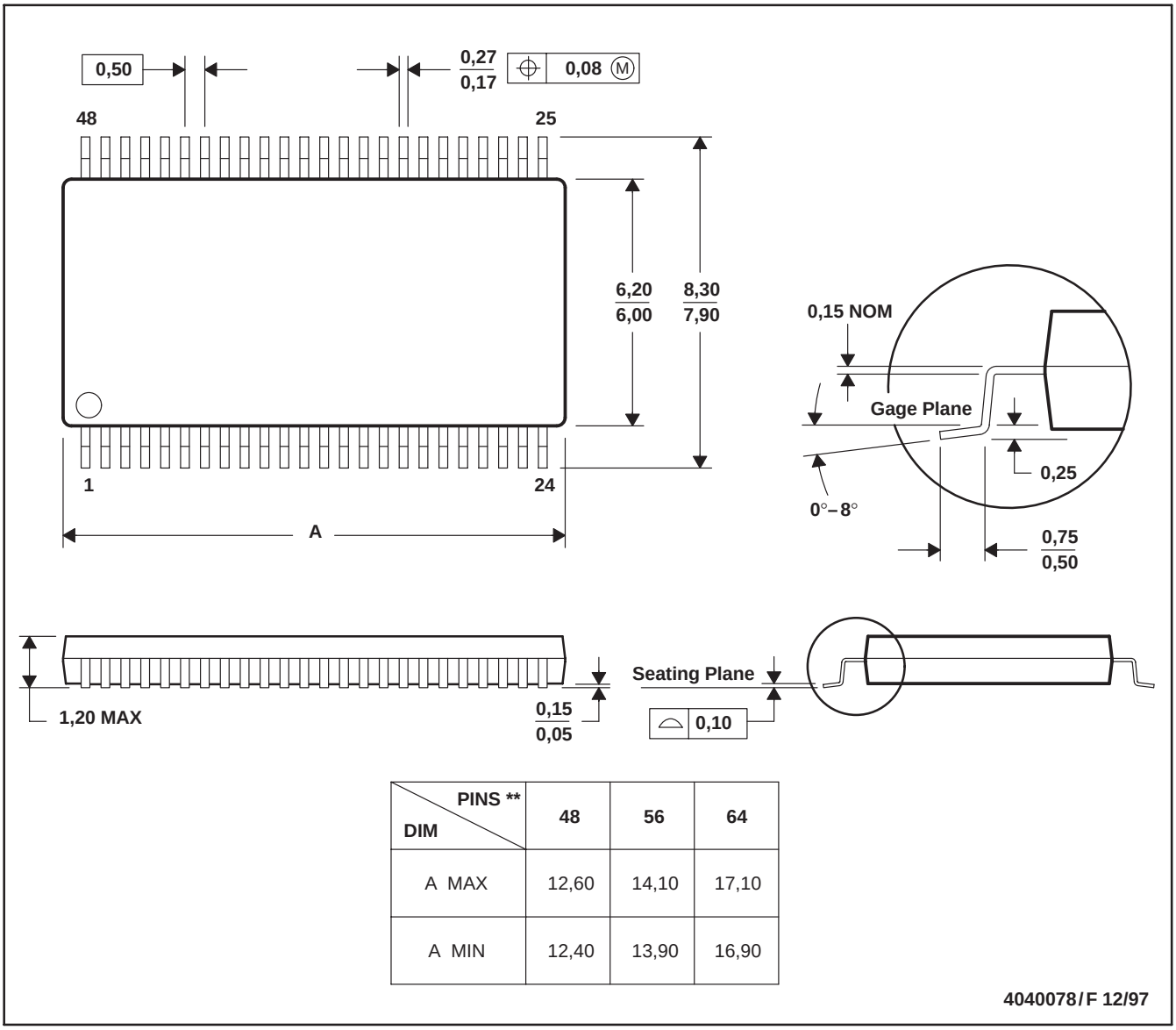


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM98714BCMTX/NOPB	TSSOP	DGG	48	1000	367.0	367.0	45.0
LM98714CCMTX/NOPB	TSSOP	DGG	48	1000	367.0	367.0	45.0

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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