The LME49724 is an ultra-low distortion, low noise, high slew rate fully-differential operational amplifier optimized and fully specified for high performance, high fidelity applications. Combining advanced leading-edge process technology with state of the art circuit design, the LME49724 fully-differential audio operational amplifier delivers superior audio signal amplification for outstanding audio performance. The LME49724 combines extremely low voltage noise density (2.1nV/√Hz) with vanishingly low THD+N (0.00003%) to easily satisfy the most demanding audio applications. To ensure that the most challenging loads are driven without compromise, the LME49724 has a high slew rate of ±18V/μs and an output current capability of ±80mA. Further, dynamic range is maximized by an output stage that drives 600Ω loads to 52V P-P while operating on a ±15V supply voltage.

The LME49724’s outstanding CMRR (102dB), PSRR (125dB), and VOS (0.2mV) results in excellent operational amplifier DC performance. The LME49724 has a wide supply range of ±2.5V to ±18V. Over this supply range the LME49724’s input circuitry maintains excellent common-mode and power supply rejection, as well as maintaining its low input bias current. The LME49724 is unity gain stable. This Fully-Differential Audio Operational Amplifier achieves outstanding AC performance while driving complex loads with capacitive values as high as 100pF.

### Table 1. Key Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage Range</td>
<td>±2.5V to ±18V</td>
</tr>
<tr>
<td>THD+N (A_{in} = 1, V_{OUT} = 3V_{RMS}, f_{IN} = 1kHz)</td>
<td></td>
</tr>
<tr>
<td>R_L = 2kΩ</td>
<td>0.00003% (typ)</td>
</tr>
<tr>
<td>R_L = 600Ω</td>
<td>0.00003% (typ)</td>
</tr>
<tr>
<td>Input Noise Density</td>
<td>2.1nV/√Hz (typ)</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>±18V/μs (typ)</td>
</tr>
<tr>
<td>Gain Bandwidth Product</td>
<td>50 MHz (typ)</td>
</tr>
<tr>
<td>Open Loop Gain (R_L = 600Ω)</td>
<td>125 dB (typ)</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>60nA (typ)</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>0.2mV (typ)</td>
</tr>
<tr>
<td>DC Gain Linearity Error</td>
<td>0.000009%</td>
</tr>
</tbody>
</table>
Typical Application

Figure 1. Typical Application Circuit

Connection Diagram

Figure 2. 8-Pin SO PowerPad
See DDA0008B Package
# PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Pin Function</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V\text{IN-}</td>
<td>Input pin</td>
<td>Analog Input</td>
</tr>
<tr>
<td>2</td>
<td>V\text{OCM}</td>
<td>Sets the output DC voltage. Internally set by a resistor divider to the midpoint of the voltages on the V\text{CC} and V\text{EE} pins. Can be forced externally to a different voltage (50k\Omega input impedance).</td>
<td>Analog Input</td>
</tr>
<tr>
<td>3</td>
<td>V\text{CC}</td>
<td>Positive power supply pin.</td>
<td>Power Supply</td>
</tr>
<tr>
<td>4</td>
<td>V\text{OUT+}</td>
<td>Output pin. Signal is inverted relative to V\text{IN-} where the feedback loop is connected.</td>
<td>Analog Output</td>
</tr>
<tr>
<td>5</td>
<td>V\text{OUT-}</td>
<td>Output pin. Signal is inverted relative to V\text{IN+} where the feedback loop is connected.</td>
<td>Analog Output</td>
</tr>
<tr>
<td>6</td>
<td>V\text{EE}</td>
<td>Negative power supply pin or ground for a single supply configuration.</td>
<td>Power Supply</td>
</tr>
<tr>
<td>7</td>
<td>ENABLE</td>
<td>Enables the LME49724 when the voltage is greater than 2.35V above the voltage on the V\text{EE} pin. Disable the LME49724 by connecting to the same voltage as on the V\text{EE} pin which will reduce current consumption to less than 0.3mA (typ).</td>
<td>Analog Input</td>
</tr>
<tr>
<td>8</td>
<td>V\text{IN+}</td>
<td>Input pin</td>
<td>Analog Input</td>
</tr>
</tbody>
</table>

Exposed Pad: Exposed pad for improved thermal performance. Connect to the same potential as the V\text{EE} pin or electrically isolate.

---

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

---

## Absolute Maximum Ratings (1)(2)(3)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>$V_s = V_{CC} +</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>$-65^\circ\text{C}$ to $150^\circ\text{C}$</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>$(V_{EE}) - 0.7\text{V}$ to $(V_{CC}) + 0.7\text{V}$</td>
</tr>
<tr>
<td>Output Short Circuit</td>
<td>Continuous</td>
</tr>
<tr>
<td>Power Dissipation (4)</td>
<td>Internally Limited</td>
</tr>
<tr>
<td>ESD Rating (5)</td>
<td>$2000\text{V}$</td>
</tr>
<tr>
<td>ESD Rating (6)</td>
<td>$200\text{V}$</td>
</tr>
<tr>
<td>Junction Temperature (T\text{MAX})</td>
<td>$150^\circ\text{C}$</td>
</tr>
<tr>
<td>Soldering Information</td>
<td>Vapor Phase (60sec.)</td>
</tr>
<tr>
<td></td>
<td>Infrared (60sec.)</td>
</tr>
<tr>
<td></td>
<td>$215^\circ\text{C}$</td>
</tr>
<tr>
<td></td>
<td>$220^\circ\text{C}$</td>
</tr>
<tr>
<td>Thermal Resistance (θ\text{JA})</td>
<td>$49.6^\circ\text{C/W}$</td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The Electrical Characteristics tables list specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{\text{JMAX}}$, $\theta_{\text{JA}}$, and the ambient temperature, $T_{\text{A}}$. The maximum allowable power dissipation is $P_{\text{DMAX}} = (T_{\text{JMAX}} - T_{\text{A}}) / \theta_{\text{JA}}$ or the number given in Absolute Maximum Ratings, whichever is lower.

(5) Human body model, applicable std. JESD22-A114C.

(6) Machine model, applicable std. JESD22-A115-A.
Operating Ratings (1)(2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LME49724</th>
<th>Units (Limits)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>POWER SUPPLY</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_S$ Operating Power Supply</td>
<td>$V_S = 0V, I_S = 0mA$</td>
<td>10</td>
<td>15 mA (max)</td>
</tr>
<tr>
<td>$I_{CCQ}$ Total Quiescent Current</td>
<td>$V_S = \pm 5V$ to $\pm 15V$ (5)</td>
<td>0.3</td>
<td>0.5 mA (max)</td>
</tr>
<tr>
<td>$PSRR$ Power Supply Rejection Ratio</td>
<td>$V_S = \pm 5V$ to $\pm 15V$ (5)</td>
<td>125</td>
<td>95 dB (min)</td>
</tr>
<tr>
<td>$V_{ENIH}$ Enable High Input Voltage</td>
<td>Device active, $T_A = 25^\circ C$ (6)</td>
<td>$V_{EE} + 2.35$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{ENIL}$ Enable Low Input Voltage</td>
<td>Device disabled, $T_A = 25^\circ C$ (6)</td>
<td>$V_{EE} + 1.75$</td>
<td>V</td>
</tr>
<tr>
<td><strong>DYNAMIC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>THD+N Total Harmonic Distortion + Noise</td>
<td>$A_V = 1$, $V_{OUT} = 3V_{RMS}$</td>
<td>0.00003</td>
<td>0.00009 % (max)</td>
</tr>
<tr>
<td>IMD Intermodulation Distortion</td>
<td>$A_V = 1$, $V_{OUT} = 3V_{RMS}$</td>
<td>0.0005</td>
<td>%</td>
</tr>
<tr>
<td>GBWP Gain Bandwidth Product</td>
<td>$V_{OUT} = 1V_{p-p}$, $3$dB referenced to output magnitude</td>
<td>50</td>
<td>35 MHz (min)</td>
</tr>
<tr>
<td>FPBW Full Power Bandwidth</td>
<td>$V_{OUT} = 1V_{p-p}$, $3$dB referenced to output magnitude</td>
<td>13</td>
<td>MHz</td>
</tr>
<tr>
<td>SR Sew Rate</td>
<td>$R_L = 2k\Omega$</td>
<td>$\pm 18$</td>
<td>$\pm 13$ V/μs (min)</td>
</tr>
<tr>
<td>$t_s$ Settling time</td>
<td>$A_V = -1.10V$ step, $C_L = 100\mu F$, settling time to 0.1%</td>
<td>0.2</td>
<td>μs</td>
</tr>
<tr>
<td>$A_{VOL}$ Open-Loop Voltage Gain</td>
<td>$-10V &lt; V_{OUT} &lt; 10V$, $R_L = 600\Omega$</td>
<td>125</td>
<td>100 dB (min)</td>
</tr>
<tr>
<td></td>
<td>$-10V &lt; V_{OUT} &lt; 10V$, $R_L = 2k\Omega$</td>
<td>125</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$-10V &lt; V_{OUT} &lt; 10V$, $R_L = 10k\Omega$</td>
<td>125</td>
<td>dB</td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The Electrical Characteristics tables list specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

(3) Typical values represent most likely parametric norms at $T_A = +25^\circ C$, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

(4) Datasheet min/max specification limits are specified by test or statistical analysis.

(5) PSRR is measured as follows: $V_{OS}$ is measured at two supply voltages, $\pm 5V$ and $\pm 15V$. PSRR = $20log(|\Delta V_{OS}|/\Delta V_S)$ |.

(6) The ENABLE threshold voltage is determined by $V_{EE}$ voltages and will therefore vary with temperature. The typical values represent the most likely parametric norms at $T_A = +25^\circ C$. 

(5) $V_{EE}$ voltages are measured with respect to the ground pin, unless otherwise specified.
Electrical Characteristics (1)(2) (continued)
The following specifications apply for $V_S = \pm 15V$, $R_L = 2k\Omega$, $f_N = 1kHz$, and $T_A = 25^\circ C$, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LME49724</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$e_N$</td>
<td>Equivalent Input Noise Voltage</td>
<td>$f_{BW} = 20Hz$ to $20kHz$</td>
<td>0.30</td>
<td>$\mu V_{RMS}$ (max)</td>
</tr>
<tr>
<td>$e_N$</td>
<td>Equivalent Input Noise Density</td>
<td>$f = 1kHz$</td>
<td>2.1</td>
<td>nV/$\sqrt{Hz}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 10Hz$</td>
<td>3.7</td>
<td></td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Offset Voltage</td>
<td></td>
<td>$\pm 0.2$</td>
<td>$\pm 1$ mV (max)</td>
</tr>
<tr>
<td>$\Delta V_{OS}/\Delta Temp$</td>
<td>Average Input Offset Voltage Drift vs Temperature</td>
<td>$-40^\circ C \leq T_A \leq 85^\circ C$</td>
<td>0.5</td>
<td>$\mu V/^\circ C$</td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input Bias Current</td>
<td>$V_{CM} = 0V$</td>
<td>60</td>
<td>nA (max)</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current</td>
<td>$V_{CM} = 0V$</td>
<td>10</td>
<td>65 nA (max)</td>
</tr>
<tr>
<td>$\Delta I_{OS}/\Delta Temp$</td>
<td>Input Bias Current Drift vs Temperature</td>
<td>$-40^\circ C \leq T_A \leq 85^\circ C$</td>
<td>0.1</td>
<td>nA/$^\circ C$</td>
</tr>
<tr>
<td>$V_{IN-CM}$</td>
<td>Common-Mode Input Voltage Range</td>
<td></td>
<td>$\pm 14$</td>
<td>$V_{CC} = 1.5$ $V_{EE} = 1.5$ V (min) V (min)</td>
</tr>
<tr>
<td>$CMRR$</td>
<td>Common-Mode Rejection</td>
<td>$-10V &lt; V_{CM} &lt; 10V$</td>
<td>102</td>
<td>95 dB (min)</td>
</tr>
<tr>
<td>$Z_{IN}$</td>
<td>Differential Input Impedance</td>
<td></td>
<td>16</td>
<td>k$\Omega$</td>
</tr>
<tr>
<td></td>
<td>Common-Mode Input Impedance</td>
<td>$-10V &lt; V_{CM} &lt; 10V$</td>
<td>500</td>
<td>M$\Omega$</td>
</tr>
<tr>
<td>$V_{OUTMAX}$</td>
<td>Maximum Output Voltage Swing</td>
<td>$R_L = 600\Omega$</td>
<td>52</td>
<td>50 $V_{P-P}$ (min)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 2k\Omega$</td>
<td>52</td>
<td>$V_{P-P}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 10k\Omega$</td>
<td>53</td>
<td>$V_{P-P}$</td>
</tr>
<tr>
<td>$I_{OUT-CC}$</td>
<td>Instantaneous Short Circuit Current</td>
<td></td>
<td>80</td>
<td>mA</td>
</tr>
<tr>
<td>$R_{OUT}$</td>
<td>Output Impedance</td>
<td>$f_N = 10kHz$ Closed-Loop</td>
<td>0.01</td>
<td>$\Omega$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Open-Loop</td>
<td>23</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$C_{LOAD}$</td>
<td>Capacitive Load Drive Overshoot</td>
<td>$C_L = 100pF$</td>
<td>5</td>
<td>%</td>
</tr>
</tbody>
</table>
Typical Performance Characteristics

THD+N vs Frequency

\( V_S = \pm 2.5V, V_O = 0.5V_{RMS} \), Differential Input
\( R_L = 600\Omega, 2k\Omega, 10k\Omega, 80kHz \) BW

Figure 3.

THD+N vs Frequency

\( V_S = \pm 2.5V, V_O = 0.8V_{RMS} \), Differential Input
\( R_L = 600\Omega, 2k\Omega, 10k\Omega, 80kHz \) BW

Figure 4.

THD+N vs Frequency

\( V_S = \pm 15V, V_O = 3V_{RMS} \), Differential Input
\( R_L = 600\Omega, 2k\Omega, 10k\Omega, 80kHz \) BW

Figure 5.

THD+N vs Frequency

\( V_S = \pm 15V, V_O = 10V_{RMS} \), Differential Input
\( R_L = 600\Omega, 2k\Omega, 10k\Omega, 80kHz \) BW

Figure 6.

THD+N vs Frequency

\( V_S = \pm 18V, V_O = 3V_{RMS} \), Differential Input
\( R_L = 600\Omega, 2k\Omega, 10k\Omega, 80kHz \) BW

Figure 7.

THD+N vs Frequency

\( V_S = \pm 18V, V_O = 10V_{RMS} \), Differential Input
\( R_L = 600\Omega, 2k\Omega, 10k\Omega, 80kHz \) BW

Figure 8.
Typical Performance Characteristics (continued)

**THD+N vs Output Voltage**

**Figure 9.**

\[
V_S = \pm 2.5\text{V}, R_L = 600\Omega, \text{Differential Input}
\]

\[
f = 20\text{Hz}, 1\text{kHz}, 20\text{kHz}, 80\text{kHz BW}
\]

**Figure 10.**

\[
V_S = \pm 15\text{V}, R_L = 600\Omega, \text{Differential Input}
\]

\[
f = 20\text{Hz}, 1\text{kHz}, 20\text{kHz}, 80\text{kHz BW}
\]

**Figure 11.**

\[
V_S = \pm 18\text{V}, R_L = 2k\Omega, \text{Differential Input}
\]

\[
f = 20\text{Hz}, 1\text{kHz}, 20\text{kHz}, 80\text{kHz BW}
\]

**Figure 12.**

\[
V_S = \pm 2.5\text{V}, R_L = 2k\Omega, \text{Differential Input}
\]

\[
f = 20\text{Hz}, 1\text{kHz}, 20\text{kHz}, 80\text{kHz BW}
\]

**Figure 13.**

\[
V_S = \pm 15\text{V}, R_L = 2k\Omega, \text{Differential Input}
\]

\[
f = 20\text{Hz}, 1\text{kHz}, 20\text{kHz}, 80\text{kHz BW}
\]

**Figure 14.**

\[
V_S = \pm 18\text{V}, R_L = 2k\Omega, \text{Differential Input}
\]

\[
f = 20\text{Hz}, 1\text{kHz}, 20\text{kHz}, 80\text{kHz BW}
\]
Typical Performance Characteristics (continued)

**THD+N vs Output Voltage**

- **Figure 15.**
  - $V_S = \pm 2.5\text{V}$, $R_L = 10\text{k}\Omega$, Differential Input
  - $f = 20\text{Hz}$, $1\text{kHz}$, $20\text{kHz}$, $80\text{kHz}$ BW

- **Figure 16.**
  - $V_S = \pm 15\text{V}$, $R_L = 10\text{k}\Omega$, Differential Input
  - $f = 20\text{Hz}$, $1\text{kHz}$, $20\text{kHz}$, $80\text{kHz}$ BW

**THD+N vs Output Voltage**

- **Figure 17.**
  - $V_S = \pm 18\text{V}$, $R_L = 10\text{k}\Omega$, Differential Input
  - $f = 20\text{Hz}$, $1\text{kHz}$, $20\text{kHz}$, $80\text{kHz}$ BW

- **Figure 18.**
  - $V_S = \pm 2.5\text{V}$, $V_O = 0.5\text{V}_{\text{RMS}}$, Single-ended Input
  - $R_L = 600\Omega$, $2\text{k}\Omega$, $10\text{k}\Omega$, $80\text{kHz}$ BW

- **Figure 19.**
  - $V_S = \pm 2.5\text{V}$, $V_O = 0.8\text{V}_{\text{RMS}}$, Single-ended Input
  - $R_L = 600\Omega$, $2\text{k}\Omega$, $10\text{k}\Omega$, $80\text{kHz}$ BW

- **Figure 20.**
  - $V_S = \pm 15\text{V}$, $V_O = 3\text{V}_{\text{RMS}}$, Single-ended Input
  - $R_L = 600\Omega$, $2\text{k}\Omega$, $10\text{k}\Omega$, $80\text{kHz}$ BW
Typical Performance Characteristics (continued)

THD+N vs Frequency

**V<sub>S</sub>** = ±15V, **V<sub>O</sub>** = 5V RMS, Single-ended Input

*RL* = 600Ω, 2kΩ, 10kΩ, 80kHz BW

Figure 21.

**V<sub>S</sub>** = ±18V, **V<sub>O</sub>** = 3V RMS, Single-ended Input

*RL* = 600Ω, 2kΩ, 10kΩ, 80kHz BW

Figure 22.

**V<sub>S</sub>** = ±18V, **V<sub>O</sub>** = 5V RMS, Single-ended Input

*RL* = 600Ω, 2kΩ, 10kΩ, 80kHz BW

Figure 23.

**V<sub>S</sub>** = ±18V, **V<sub>O</sub>** = 3V RMS, Single-ended Input

*RL* = 600Ω, 2kΩ, 10kΩ, 80kHz BW

Figure 24.

**V<sub>S</sub>** = ±2.5V, *RL* = 600Ω, Single-ended Input

*f* = 20Hz, 1kHz, 20kHz, 80kHz BW

Figure 25.

**V<sub>S</sub>** = ±15V, *RL* = 600Ω, Single-ended Input

*f* = 20Hz, 1kHz, 20kHz, 80kHz BW

Figure 26.
Typical Performance Characteristics (continued)

**THD+N vs Output Voltage**

- **Output Voltage**
  - $V_S = \pm 2.5V$, $R_L = 2k\Omega$, Single-ended Input
  - $f = 20Hz$, $1kHz$, $20kHz$, $80kHz$ BW

- **Output Voltage**
  - $V_S = \pm 15V$, $R_L = 2k\Omega$, Single-ended Input
  - $f = 20Hz$, $1kHz$, $20kHz$, $80kHz$ BW

- **Output Voltage**
  - $V_S = \pm 18V$, $R_L = 2k\Omega$, Single-ended Input
  - $f = 20Hz$, $1kHz$, $20kHz$, $80kHz$ BW

- **Output Voltage**
  - $V_S = \pm 2.5V$, $R_L = 10k\Omega$, Single-ended Input
  - $f = 20Hz$, $1kHz$, $20kHz$, $80kHz$ BW

- **Output Voltage**
  - $V_S = \pm 15V$, $R_L = 10k\Omega$, Single-ended Input
  - $f = 20Hz$, $1kHz$, $20kHz$, $80kHz$ BW

- **Output Voltage**
  - $V_S = \pm 18V$, $R_L = 10k\Omega$, Single-ended Input
  - $f = 20Hz$, $1kHz$, $20kHz$, $80kHz$ BW

**Figure 27.**

**Figure 28.**

**Figure 29.**

**Figure 30.**

**Figure 31.**

**Figure 32.**
Typical Performance Characteristics (continued)

**PSRR vs Frequency**

V\(_S\) = ±2.5V, R\(_L\) = 600Ω, Inputs to GND
V\(_{\text{RIPPLE}}\) = 200mV\(_{\text{P-P}}\), 80kHz BW

- **Figure 33.**

V\(_S\) = ±15V, R\(_L\) = 600Ω, Inputs to GND
V\(_{\text{RIPPLE}}\) = 200mV\(_{\text{P-P}}\), 80kHz BW

- **Figure 34.**

V\(_S\) = ±18V, R\(_L\) = 600Ω, Inputs to GND
V\(_{\text{RIPPLE}}\) = 200mV\(_{\text{P-P}}\), 80kHz BW

- **Figure 35.**

V\(_S\) = ±2.5V, R\(_L\) = 2kΩ, Inputs to GND
V\(_{\text{RIPPLE}}\) = 200mV\(_{\text{P-P}}\), 80kHz BW

- **Figure 36.**

V\(_S\) = ±15V, R\(_L\) = 2kΩ, Inputs to GND
V\(_{\text{RIPPLE}}\) = 200mV\(_{\text{P-P}}\), 80kHz BW

- **Figure 37.**

V\(_S\) = ±18V, R\(_L\) = 2kΩ, Inputs to GND
V\(_{\text{RIPPLE}}\) = 200mV\(_{\text{P-P}}\), 80kHz BW

- **Figure 38.**
Typical Performance Characteristics (continued)

**PSRR vs Frequency**

- $V_S = \pm 2.5\text{V}$, $R_L = 10\text{k}\Omega$, Inputs to GND
- $V_{\text{RIPPLE}} = 200mV_{\text{P-P}}$, $80\text{kHz BW}$

---

**CMRR vs Frequency**

- $V_S = \pm 15\text{V}$, $V_{\text{CMRR}} = 1V_{\text{P-P}}$
- $R_L = 600\Omega$, $2k\Omega$, $10\text{k}\Omega$

---

Figure 39.

Figure 40.

Figure 41.

Figure 42.

Figure 43.

Figure 44.
Typical Performance Characteristics (continued)

Output Voltage vs Load Resistance

\[
V_S = \pm 2.5V, \quad R_L = 500\Omega - 10k\Omega \\
THD+N \leq 1\%, \quad 80kHz \text{ BW}
\]

Figure 45.

Output Voltage vs Load Resistance

\[
V_S = \pm 15V, \quad R_L = 500\Omega - 10k\Omega \\
THD+N \leq 1\%, \quad 80kHz \text{ BW}
\]

Figure 46.

Output Voltage vs Load Resistance

\[
V_S = \pm 18V, \quad R_L = 500\Omega - 10k\Omega \\
R_L = 600\Omega, 2k\Omega, 10k\Omega, \quad THD+N \leq 1\% \\
80kHz \text{ BW}
\]

Figure 47.

Supply Current vs Supply Voltage

\[
V_{IN} = 0V, \quad R_L = \text{No Load}
\]

Figure 49.
GENERAL OPERATION

The LME49724 is a fully differential amplifier with an integrated common-mode reference input (\(V_{\text{OCM}}\)). Fully differential amplification provides increased noise immunity, high dynamic range, and reduced harmonic distortion products.

Differential amplifiers typically have high CMRR providing improved immunity from noise. When input, output, and supply line trace pairs are routed together, noise pick up is common and easily rejected by the LME49724. CMRR performance is directly proportional to the tolerance and matching of the gain configuring resistors. With 0.1% tolerance resistors the worst case CMRR performance will be about 60dB (20LOG(0.001)).

A differential output has a higher dynamic range than a single-ended output because of the doubling of output voltage. The dynamic range is increased by 6dB as a result of the outputs being equal in magnitude but opposite in phase. As an example, a single-ended output with a 1V\(_{\text{PP}}\) signal will be two 1V\(_{\text{PP}}\) signals with a differential output. The increase is 20LOG(2) = 6dB. Differential amplifiers are ideal for low voltage applications because of the increase in signal amplitude relative to a single-ended amplifier and the resulting improvement in SNR.

Differential amplifiers can also have reduced even order harmonics, all conditions equal, when compared to a single-ended amplifier. The differential output causes even harmonics to cancel between the two inverted outputs leaving only the odd harmonics. In practice even harmonics do not cancel completely, however there still is a reduction in total harmonic distortion.

OUTPUT COMMON-MODE VOLTAGE (\(V_{\text{OCM}}\) pin)

The output common-mode voltage is the DC voltage on each output. The output common-mode voltage is set by the \(V_{\text{OCM}}\) pin. The \(V_{\text{OCM}}\) pin can be driven by a low impedance source. If no voltage is applied to the \(V_{\text{OCM}}\) pin, the DC common-mode output voltage will be set by the internal resistor divider to the midpoint of the voltages on the \(V_{\text{CC}}\) and \(V_{\text{EE}}\) pins. The input impedance of the \(V_{\text{OCM}}\) pin is 50k\(\Omega\). The \(V_{\text{OCM}}\) pin can be driven up to \(V_{\text{CC}} - 1.5V\) and \(V_{\text{EE}} + 1.5V\). The \(V_{\text{OCM}}\) pin should be bypassed to ground with a 0.1\(\mu\)F to 1\(\mu\)F capacitor. The \(V_{\text{OCM}}\) pin should be connected to ground when the desired output common-mode voltage is ground reference. The value of the external capacitor has an effect on the PSRR performance of the LME49724. With the \(V_{\text{OCM}}\) pin only bypassed with a low value capacitor, the PSRR performance of the LME49724 will be reduced, especially at low audio frequencies. For best PSRR performance, the \(V_{\text{OCM}}\) pin should be connected to stable, clean reference. Increasing the value of the bypass capacitor on the \(V_{\text{OCM}}\) pin will also improve PSRR performance.

ENABLE FUNCTION

The LME49724 can be placed into standby mode to reduce system current consumption by driving the ENABLE pin below \(V_{\text{EE}} + 1.75V\). The LME49724 is active when the voltage on the ENABLE pin is above \(V_{\text{EE}} + 2.35V\). The ENABLE pin should not be left floating. For best performance under all conditions, drive the ENABLE pin to the \(V_{\text{EE}}\) pin voltage to enter standby mode and to ground for active operation when operating from split supplies. When operating from a single supply, drive the ENABLE pin to ground for standby mode and to \(V_{\text{CC}}\) for active mode.
FULLY DIFFERENTIAL OPERATION

The LME49724 performs best in a fully differential configuration. The circuit shown in Figure 50 is the typical fully differential configuration.

![Figure 50. Fully Differential Configuration](image)

The closed-loop gain is shown in Equation 1 below.

\[ A_V = \frac{R_F}{R_i} \text{ (V/V)} \]

where

- \( R_{F1} = R_{F2} \)
- \( R_{i1} = R_{i2} \)
- Using low value resistors will give the lowest noise performance \( (1) \)

SINGLE-ENDED TO DIFFERENTIAL CONVERSION

For many applications, it is required to convert a single-ended signal to a differential signal. The LME49724 can be used for a high performance, simple single-to-differential converter. Figure 51 shows the typical single-to-differential converter circuit configuration.

![Figure 51. Single-Ended Input to Differential Output](image)
SINGLE SUPPLY OPERATION

The LME49724 can be operated from a single power supply, as shown in Figure 52. The supply voltage range is limited to a minimum of 5V and a maximum of 36V. The common-mode output DC voltage will be set to the midpoint of the supply voltage. The V\text{OCM} pin can be used to adjust the common-mode output DC voltage on the outputs, as described previously, if the supply voltage midpoint is not the desired DC voltage.

![Figure 52. Single Supply Configuration](image)

DRIVING A CAPACITIVE LOAD

The LME49724 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable. Capacitive loads greater than 100pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

THERMAL PCB DESIGN

The LME49724’s high operating supply voltage along with its high output current capability can result in significant power dissipation. For this reason the LME49724 is provided in the exposed DAP SO PowerPad package for improved thermal dissipation performance compared to other surface mount packages. The exposed pad is designed to be soldered to a copper plane on the PCB which then acts as a heat sink. The thermal plane can be on any layer by using multiple thermal vias under and outside the IC package. The vias under the IC should have solder mask openings for the entire pad under the IC on the top layer but cover the vias on the bottom layer. This method prevents solder from being pulled away from the thermal vias during the reflow process resulting in optimum thermal conductivity.

Heat radiation from the PCB plane area is best accomplished when the thermal plane is on the top or bottom copper layers. The LME49724 should always be soldered down to a copper pad on the PCB for both optimum thermal performance as well as mechanical stability.

The exposed pad is for heat transfer and the thermal plane should either be electrically isolated or connected to the same potential as the V\text{EE} pin. For high frequency applications (f > 1MHz) or lower impedance loads, the pad should be connected to a plane that is connected to the V\text{EE} potential.
SUPPLY BYPASSING

The LME49724 should have its supply leads bypassed with low-inductance capacitors such as leadless surface mount (SMT) capacitors located as close as possible to the supply pins. It is recommended that a 10μF tantalum or electrolytic capacitor be placed in parallel with a 0.1μF ceramic or film type capacitor on each supply pin. These capacitors should be star routed with a dedicated ground return plane or large trace for best THD performance. Placing capacitors too far from the power supply pins, especially with thin connecting traces, can lead to excessive inductance, resulting in degraded high-frequency bypassing. Poor high-frequency bypassing can result in circuit instabilities. When using high bandwidth power supplies, the value and number of supply bypass capacitors should be reduced for optimal power supply performance.

BALANCE CABLE DRIVER

With high peak-to-peak differential output voltage and plenty of low distortion drive current, the LME49724 makes an excellent balanced cable driver. Combining the single-to-differential configuration with a balanced cable driver results in a high performance single-ended input to balanced line driver solution.

Although the LME49724 can drive capacitive loads up to 100pF, cable loads exceeding 100pF can cause instability. For such applications, series resistors are needed on the outputs before the capacitive load.

ANALOG-TO-DIGITAL CONVERTER (ADC) APPLICATION

Figure 53 is a typical fully differential application circuit for driving an analog-to-digital converter (ADC). The additional components of R₅, R₆, and C₇ are optional components and are for stability and proper ADC sampling. ADC’s commonly use switched capacitor circuitry at the input. When the ADC samples the signal the current momentarily increases and may disturb the signal integrity at the sample point causing a signal glitch. Component C₇ is significantly larger than the input capacitance of a typical ADC and acts as a charge reservoir greatly reducing the effect of the signal sample by the ADC. Resistors R₅ and R₆ decouple the capacitive load, C₇, for stability. The values shown are general values. Specific values should be optimized for the particular ADC loading requirements.

The output reference voltage from the ADC can be used to drive the V_{OCM} pin to set the common-mode DC voltage on the outputs of the LME49724. A buffer may be needed to drive the LME49724’s V_{OCM} pin if the ADC cannot drive the 50kΩ input impedance of the V_{OCM} pin.

In order to minimize circuit distortion when using capacitors in the signal path, the capacitors should be comprised of either NPO ceramic, polystyrene, polypropylene or mica composition. Other types of capacitors may provide a reduced distortion performance but for a cost improvement, so capacitor selection is dependent upon design requirements. The performance/cost tradeoff for a specific application is left up to the user.
DISTORTION MEASUREMENTS

The vanishing low residual distortion produced by the LME49724 is below the capabilities of commercially available equipment. This makes distortion measurements more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49724’s low residual distortion is an input referred internal error. As shown in Figure 54, adding a resistor connected between the amplifier’s inputs changes the amplifier’s noise gain. The result is that the error signal (distortion) is increased. Although the amplifier’s closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced, which means that measurement resolution increases. To ensure minimum effects on distortion measurements, keep the value of $R_5$ low. The distortion reading on the audio analyzer must be divided by a factor of $(R_3 + R_4)/R_5$, where $R_1 = R_2$ and $R_3 = R_4$, to get the actual measured distortion of the device under test. The values used for the LME49724 measurements were $R_1$, $R_2$, $R_3$, $R_4 = 1k\Omega$ and $R_5 = 20\Omega$.

This technique is verified by duplicating the measurements with high closed-loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment’s capabilities.
PERFORMANCE VARIATIONS

The LME49724 has excellent performance with little variation across different supply voltages, load impedances, and input configuration (single-ended or differential). Inspection of the THD+N vs Frequency and THD+N vs Output Voltage performance graphs (See Typical Performance Characteristics reveals only minimal differences with different load values. Figure 55 and Figure 56 below show the performance across different supply voltages with the same output signal level and load. Figure 55 has plots at ±5V, ±12V, ±15V, and ±18V with a 3V RMS output while Figure 56 has plots at ±12V, ±15V, and ±18V with a 10V RMS output. Both figures use a 600Ω load. The performance for each different supply voltage under the same conditions is so similar it is nearly impossible to discern the different plots lines.

Figure 55. THD+N vs FREQUENCY with R_L = 600Ω
V_{OUT} = 3V_{RMS}, Differential Input, 80kHz BW
V_S = ±5V, ±12V, ±15V, and ±18V
Figure 56. THD+N vs FREQUENCY with $R_L = 600\,\Omega$
$V_{OUT} = 10\,V_{RMS}$, Differential Input, 80kHz BW
$V_S = \pm12V, \pm15V, \text{and} \pm18V$

Whether the input configuration is single-ended or differential has only a minimal affect on THD+N performance at higher audio frequencies or higher signal levels. For easy comparison, Figure 57 and Figure 58 are a combination of the performance graphs found in Typical Performance Characteristics.

Figure 57. THD+N vs FREQUENCY with $R_L = 10k\,\Omega$
$V_{OUT} = 3\,V_{RMS}$, $V_S = \pm15V$, 80kHz BW
Single-ended and Differential Input
Figure 58. THD+N vs OUTPUT VOLTAGE with $R_L = 10k\Omega$

$f = 20Hz, 1kHz, 20kHz, V_S = \pm 15V, 80kHz BW$

Single-ended and Differential Input

Power Supply Rejection Ratio does not vary with load value nor supply voltage. For easy comparison, Figure 59 and Figure 60 below are created by combining performance graphs found in Typical Performance Characteristics.

Figure 59. PSRR vs FREQUENCY with $R_L = 600\Omega$

$V_S = \pm 2.5V, \pm 15V, \text{ and } \pm 18V, 80kHz BW$
Although supply current may not be a critical specification for many applications, there is also no real variation in supply current with no load or with a 600Ω load. This is a result of the extremely low offset voltage, typically less than 1mV. Figure 61 shows the supply current under the two conditions with no real difference discernable.
Demo Board Schematic

Figure 62. Demonstration Board Circuit

Build of Materials

Table 2. Reference Demo Board Bill of Materials

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<thead>
<tr>
<th>Designator</th>
<th>Value</th>
<th>Tolerance</th>
<th>Part Description</th>
<th>Comment</th>
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## REVISION HISTORY

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<td>Initial release.</td>
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<td>Changed layout of National Data Sheet to TI format.</td>
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## Packaging Information

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<th>Package Qty</th>
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<th>Op Temp (°C)</th>
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- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

*All dimensions are nominal.*

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### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
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**TBD**: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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---|---|---|---|---|---|---|---|---|---|---|---|---
LME49724MRX/NOPB | SO | DDA | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1

*All dimensions are nominal.*

**Tape Dimensions**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**Reel Dimensions**

- **Reel Diameter**
- **Reel Width** (W1)

**Quadrant Assignments for Pin 1 Orientation in Tape**

- **Pocket Quadrants**
- **Sprocket Holes**
- **User Direction of Feed**

---

*www.ti.com 8-Apr-2013*
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LME49724MRX/NOPB</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12. Board assembly site may have different recommendations for stencil design.
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