LM48822 Boomer ™ Ground-Referenced, Ultra High PSRR, Ultra Low Noise, 35mW/Channel Stereo Headphone Amplifier with Common Mode Sense, and I²C Volume Control

Check for Samples: LM48822, LM48822TLEVAL

FEATURES

- **Ground Referenced Outputs – Eliminates Output Coupling Capacitors**
- **Common-Mode Sense**
- **Ultra-High PSRR**
- **I²C Volume and Mode Control**
- **High Output Impedance in Shutdown**
- **Differential Inputs**
- **Advanced Click-and-Pop Suppression**
- **Low Supply Current**
- **Minimum External Components**
- **Micro-Power Shutdown**
- **Available in Space-Saving 16-Bump DSBGA Package**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Notebook PCs**
- **Portable Electronic Devices**
- **MP3 Players**

KEY SPECIFICATIONS

- **Output Power/Channel at V_{DD} = 3.6V**
  - **R_L = 16Ω, THD+N ≤ 1%: 35mW (typ)**
- **Output Power/Channel at V_{DD} = 3.6V**
  - **R_L = 32Ω, THD+N ≤ 1%: 40mW (typ)**
- **Quiescent Power Supply Current at 3.6V: 3.5mA (typ)**
- **PSRR at 217Hz: 110dB (typ)**
- **Shutdown Current: 0.06µA (typ)**

DESCRIPTION

The LM48822 is a single supply, ground-referenced stereo headphone amplifier designed for portable devices, such as cell phones, where board space is at a premium. The LM48822 features TI's ground-referenced architecture, which eliminates the large DC blocking capacitor required by traditional headphone amplifiers, saving board space and minimizing system cost.

The LM48822 features common-mode sensing that corrects for any differences between the amplifier ground and the potential at the headphone return terminal, minimizing noise created by any ground mismatches.

The LM48822 delivers 35mW/channel into a 16Ω load with <1% THD+N with a 3.6V supply. High power supply rejection ratio (PSRR), of 110dB at 217Hz, allows the device to operate in noisy environments without additional power supply conditioning. Flexible power supply requirements allow operation from 2.4V to 5.5V. The LM48822 has a differential inputs for improved noise rejection. High output impedance in Shutdown mode, combined with a charge pump-only mode allows the LM48822's outputs to be driven by an external source without degrading the source signal. Additionally, the LM48822 features a 64-step I²C volume control and mute function. The low power Shutdown mode reduces supply current consumption to 0.06µA.

Superior click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM48822 is available in an ultra-small 16-bump DSBGA package (2mmx2mm).

Typical Application

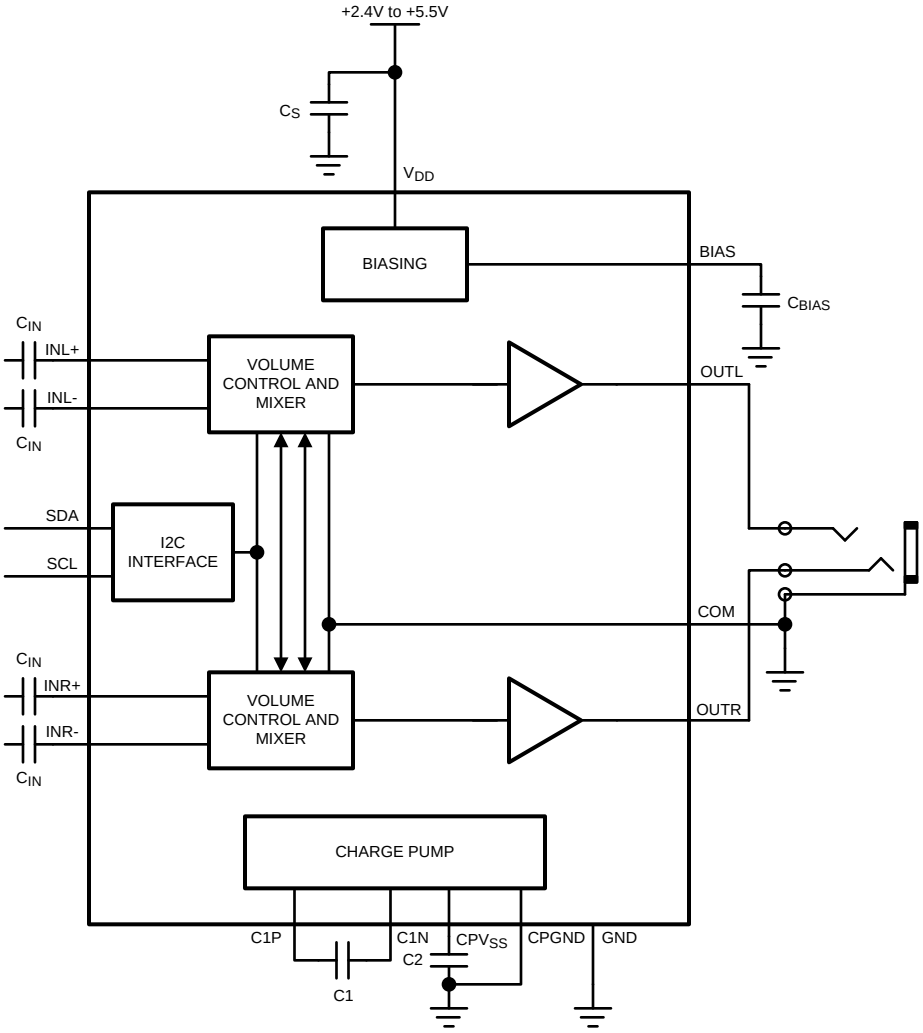


Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Top View

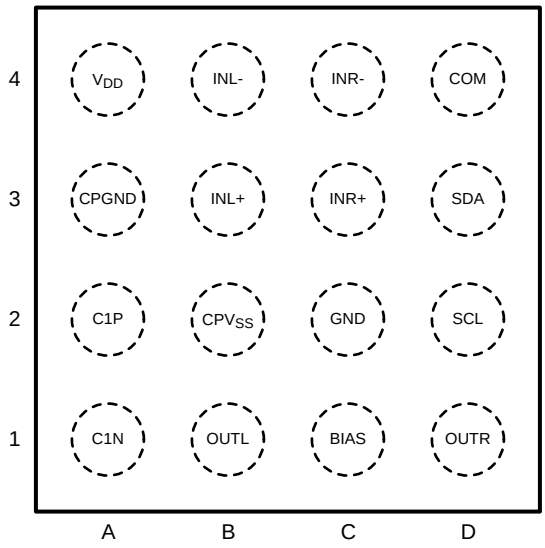


Figure 2. DSBGA Package
2mm x 2mm x 0.8mm
See Package Number YZR001611A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

Supply Voltage[1]	6V
Storage Temperature	−65°C to +150°C
Input Voltage	-0.3V to V_{DD} + 0.3V
Power Dissipation[4]	Internally Limited
ESD Rating[5]	2000V
ESD Rating[6]	150V
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} YZR001611A	63°C/W
Soldering Information See AN-1112 “DSBGA Wafer Level Chip Scale package”	

(1) *“Absolute Maximum Ratings”* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings*Ratings or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(4) Maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

(5) Human body model, applicable std. JESD22-A114C.

(6) Machine model, applicable std. JESD22-A115-A.

Operating Ratings

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage (V_{DD})	$2.4V \le V_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 3.6V(1)(2)

The following specifications apply for A_V = 0dB, R_L = 16Ω, f = 1kHz, unless otherwise specified. Limits apply to T_A = 25°C.

Parameter		Test Conditions	LM48822		Units (Limits)
			Typ(3)	Limit(4)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, both channels active R_L = 16Ω R_L = ∞	3.5 3.5	4.5 4.5	mA (max) mA (max)
I_{SD}	Shutdown Current	Shutdown Enabled	0.06	1.2	µA (max)
V_{OS}	Differential Output Offset Voltage	V_{IN} = 0V, R_L = 16Ω	1	5	mV (max)
T_{WU}	Wake Up Time		200		µs
A_V	Voltage Gain	Minimum Gain Setting	–59.5	+0.5 –0.5	dB (max) dB (min)
		Maximum Gain Setting	3.8	+0.5 –0.5	dB (max) dB (min)
R_{IN}	Input Resistance	A_V = 4dB A_V = –60dB	25 60	30 70	kΩ (max) kΩ (max)
P_O	Output Power	R_L= 16Ω, f = 1kHz, THD+N = 1% Single channel Two channels in phase	70 35	27	mW mW (min)
		R_L= 32Ω, f = 1kHz, THD+N = 1% Single channel Two channels in phase	65 40		mW mW
THD+N	Total Harmonic Distortion + Noise	P_O = 50mW, f = 1kHz, R_L = 16Ω single channel	0.04		%
		P_O = 40mW, f = 1kHz, R_L = 32Ω single channel	0.02		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P}, Inputs AC GND C_{IN} = 1µF, input referred, SD_BIAS = 0 f_{RIPPLE} = 217Hz f_{RIPPLE} = 1kHz	110 100	100	dB (min) dB
CMRR	Common Mode Rejection Ratio	V_{RIPPLE} = 1V_{P-P}	95		dB
X_{TALK}	Crosstalk	$R_L \ge$ 16Ω, P_{OUT} = 1.6mW, f = 1kHz	80	70	dB (min)
		$R_L \ge$ 10kΩ, V_{OUT} = 1V_{RMS}, f = 1kHz	95	85	dB (min)
SNR	Signal-to-Noise Ratio	R_L = 16Ω, f = 1kHz	100		dB
$\in_{OS}$	Output Noise	A_V = 4dB, Input referred A-Weighted Filter	7		µV
R_{OUT}	Output Impedance	Charge pump-only mode enabled	40	25	kΩ (min)
V_{OUT}	Maximum Voltage Swing	Voltage applied to amplifier outputs in charge pump-only mode		2	V_{RMS} (min)

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings*Ratings or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not specified.

(4) Datasheet min/max specification limits are ensured by test or statistical analysis.

I^2C Interface Characteristics V_{DD} = 3.6V(1)(2)

The following specifications apply for A_V = 0dB, R_L = 16Ω, f = 1kHz, unless otherwise specified. Limits apply to T_A = 25°C.

Parameter		Test Conditions	LM48822		Units (Limits)
			Typ(3)	Limit(4)	
t_1	SCL Period			2.5	µs (min)
t_2	SDA Setup Time			100	ns (min)
t_3	SDA Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
V_{IH}	Input High Voltage			1.3	V (min)
V_{IL}	Input Low Voltage			0.4	V (max)

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings*Ratings or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not specified.

(4) Datasheet min/max specification limits are ensured by test or statistical analysis.

Bump Descriptions

Pin	Name	Function
A1	C1N	Charge Pump Flying Capacitor Negative Terminal
A2	C1P	Charge Pump Flying Capacitor Positive Terminal
A3	CPGND	Charge Pump Ground
A4	V_{DD}	Power Supply
B1	OUTL	Left Channel Output
B2	CPV_{SS}	Charge Pump Output
B3	INL+	Left Channel Non-Inverting Input
B4	INL-	Left Channel Inverting Input
C1	BIAS	Bias Voltage Bypass
C2	GND	Ground
C3	INR+	Right Channel Non-Inverting Input
C4	INR-	Right Channel Inverting Input
D1	OUTR	Right Channel Output
D2	SCL	I^2C Serial Clock Input
D3	SDA	I^2C Serial Data Input
D4	COM	Common-Mode Sense Input

Typical Performance Characteristics

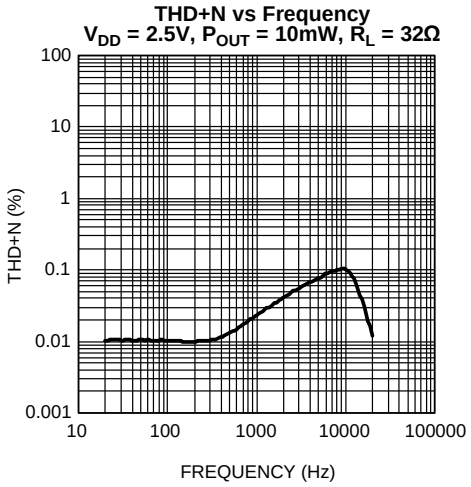


Figure 3.

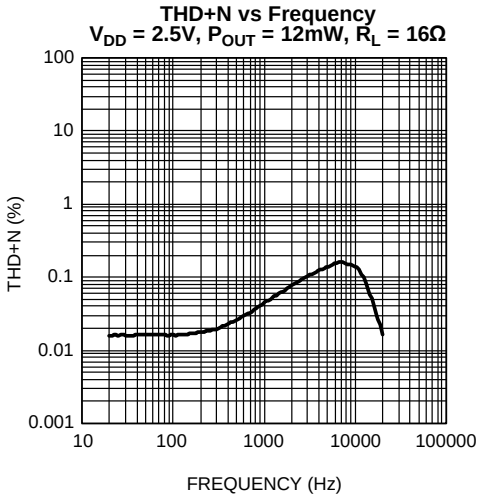


Figure 4.

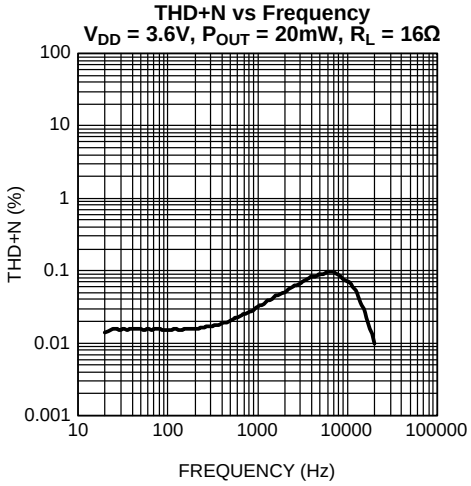


Figure 5.

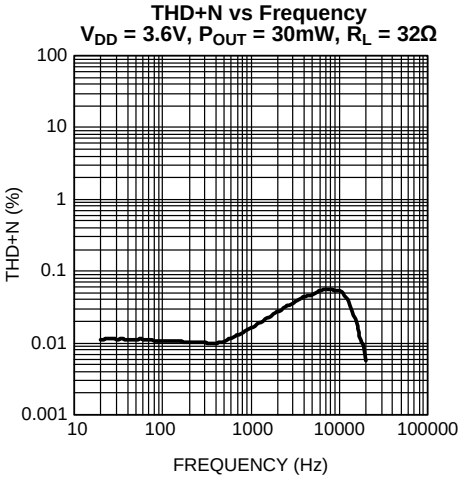


Figure 6.

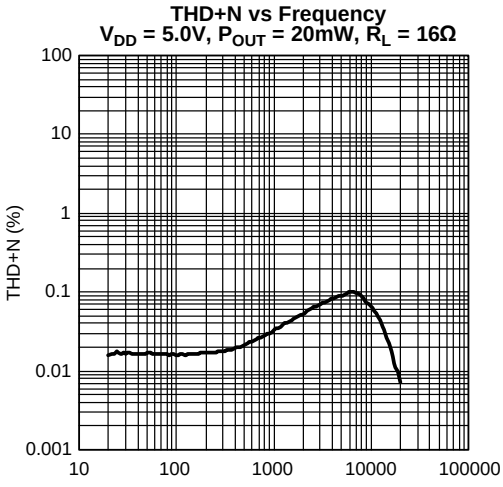


Figure 7.

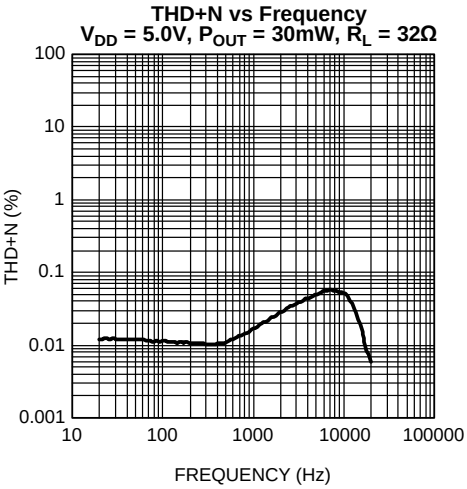


Figure 8.

Typical Performance Characteristics (continued)

THD+N vs Output Power
A_V = 0dB, R_L = 16Ω, f = 1kHz
Both Outputs in Phase

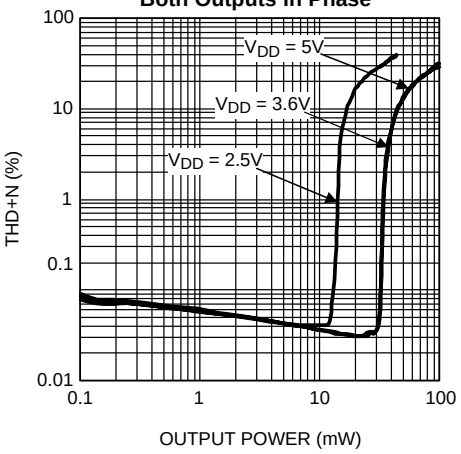


Figure 9.

THD+N vs Output Power
A_V = 0dB, R_L = 32Ω, f = 1kHz
Both Outputs in Phase

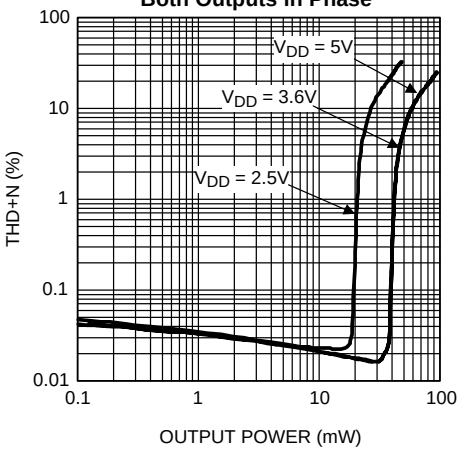


Figure 10.

THD+N vs Output Power
A_V = 9dB, R_L = 16Ω, f = 1kHz
Both Outputs in Phase

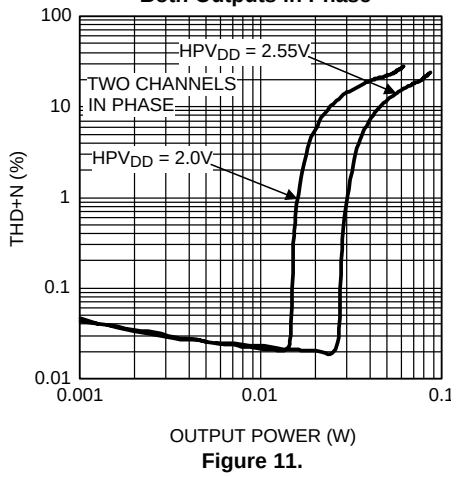


Figure 11.

Power Dissipation vs Output Power
R_L = 16Ω, f = 1kHz

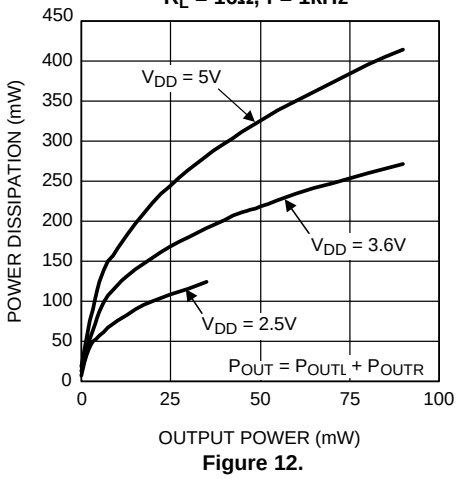


Figure 12.

Power Dissipation vs Output Power
R_L = 32Ω, f = 1kHz

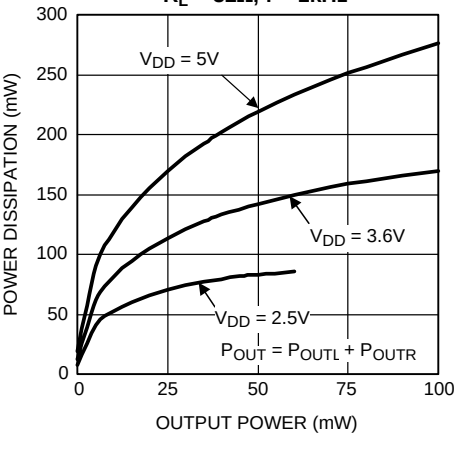


Figure 13.

Output Power vs Supply Voltage
R_L = 16Ω, f = 1kHz

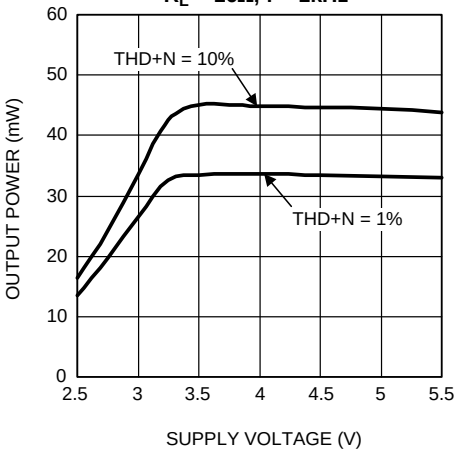


Figure 14.

Typical Performance Characteristics (continued)

Output Power vs Supply Voltage
R_L = 32Ω, f = 1kHz

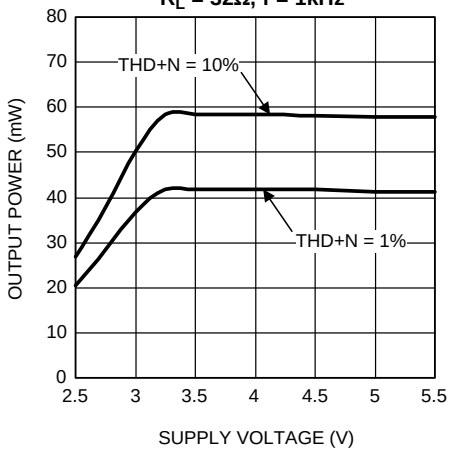


Figure 15.

CMRR vs Frequency
V_{DD} = 3.6V, V_{CM} = 1V_{P-P}, R_L = 32Ω

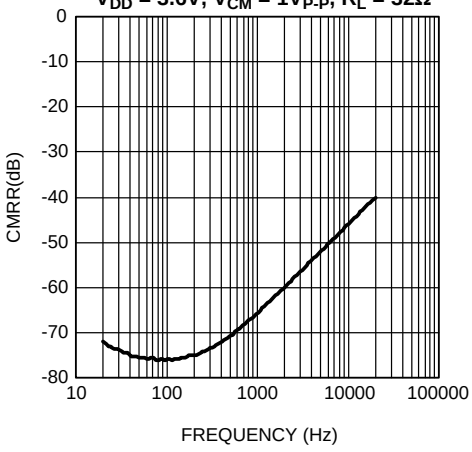


Figure 16.

PSRR vs Frequency
V_{DD} = 3.6V, V_{RIPPLE} = 20mV_{P-P}, R_L = 32Ω

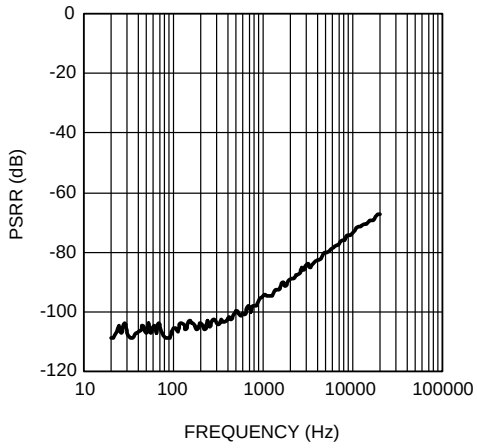


Figure 17.

Crosstalk vs Frequency
V_{DD} = 3.6V, V_{RIPPLE} = 1V_{P-P}, R_L = 32Ω

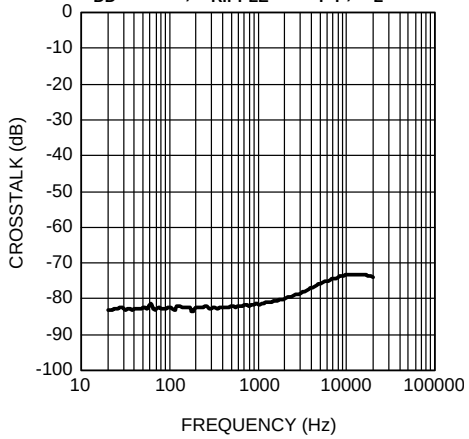


Figure 18.

Ground Noise vs Frequency
V_{DD} = 3.6V, V_{RIPPLE} = 20mV_{P-P}, R_L = 32Ω

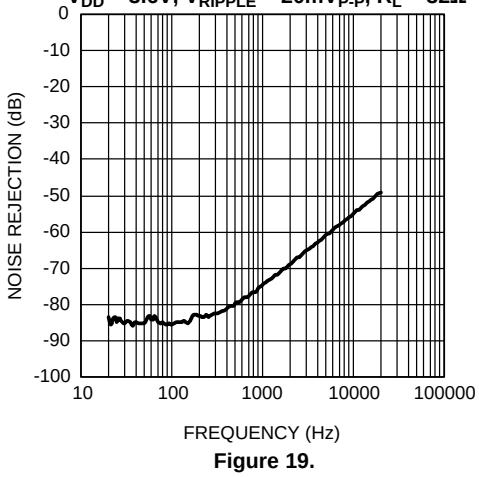


Figure 19.

Supply Current vs Supply Voltage
No Load

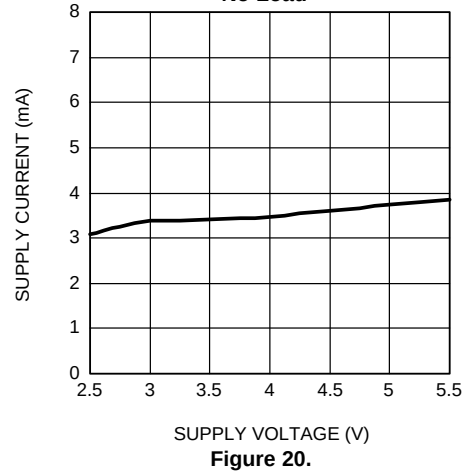


Figure 20.

APPLICATION INFORMATION

I²C COMPATIBLE INTERFACE

The LM48822 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open collector). The LM48822 and the master can communicate at clock rates up to 400kHz. Figure 21 shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48822 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition Figure 22. Each data word, device address and data, transmitted over the bus is 8 bits long as is always followed by an acknowledge pulse (Figure 23). The LM48822 device address is 1100000.

I²C BUS FORMAT

The I²C bus format is shown in Figure 23. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/$\overline{W}$ bit. R/$\overline{W}$ = 0 indicates the master is writing to the slave device, R/$\overline{W}$ = 1 indicates the master wants to read data from the slave device. The LM48822 is a WRITE-ONLY device and will not respond the R/$\overline{W}$ = 1. The data is latched in on the rising edge of the clock. Each address bit must be stable while SDA is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48822 receives the correct address, the device pulls the SDA line low, generating and acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, the LM48822 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high while SDA is high.

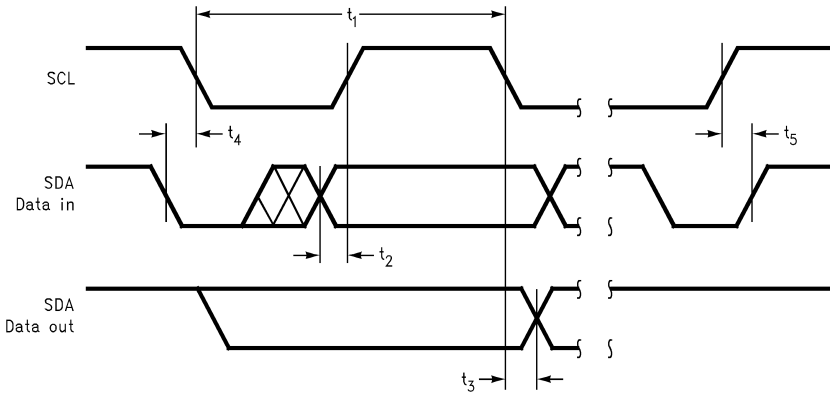


Figure 21. I²C Timing Diagram

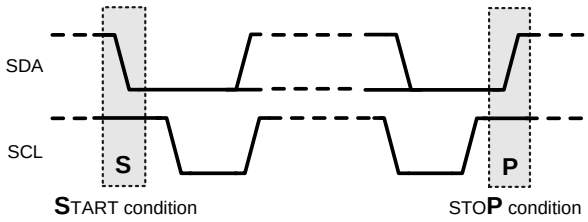


Figure 22. Start and Stop Diagram

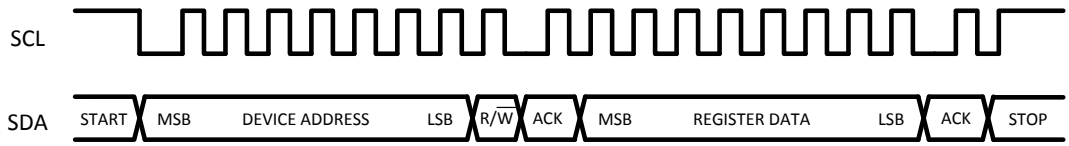


Figure 23. Example I²C Write Cycle

Table 1. Device Address

	B7	B6	B5	B4	B3	B2	B1	B0 (R/$\overline{W}$)
Device Address	1	1	0	0	0	0	0	0

Table 2. I²C Control Registers

Register Address	Register Name	B7	B6	B5	B4	B3	B2	B1	B0
0	MODE CONTROL	0	SDL	SD_BIAS	CP_ONLY	0	MUTE_ LEFT	SDR	MUTE_ RIGHT
1	VOLUME CONTROL	1	SHDN	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0

Table 3. Mode Control Register

Bit	Name	Value	Description
B6	SDL	0	Left channel enabled
		1	Left channel disabled
B5	SD_BIAS	0	Bias enabled
		1	Bias disabled
B4	CP_ONLY	0	Normal operation
		1	Charge-pump only mode. Amplifiers and Bias disabled.
B3	UNUSED	0	Set B3 to 0
B2	MUTE_LEFT	0	Left channel Normal Operation
		1	Left channel Mute
B1	SDR	0	Right channel enabled
		1	Right channel disabled. Right channel audio inputs summed with left channel audio inputs and routed to OUTL
B0	MUTE_RIGHT	0	Right channel Normal Operation
		1	Right channel Mute

GENERAL AMPLIFIER FUNCTION

The LM48822 headphone amplifier feature TI's ground referenced architecture that eliminates the large DC-blocking capacitors required at the outputs of traditional headphone amplifiers. A low-noise inverting charge pump creates a negative supply (CPV_{SS}) from the positive supply voltage (V_{DD}). The headphone amplifiers operate from these bipolar supplies, with the amplifier outputs biased about GND, instead of a nominal DC voltage (typically $V_{DD}/2$), like traditional amplifiers. Because there is no DC component to the headphone output signals, the large DC-blocking capacitors (typically 220µF) are not necessary, conserving board space and system cost, while improving frequency response.

GENERAL AMPLIFIER EXPLANATION

The LM48822 features a differential input stage, which offers improved noise rejection compared to a single-ended input amplifier. Because a differential input amplifier amplifies the difference between the two input signals, any component common to both signals is cancelled. An additional benefit of the differential input structure is the possible elimination of the DC input blocking capacitors. Since the DC component is common to both inputs, and thus cancelled by the amplifier, the LM48822 can be used without input coupling capacitors when configured with a differential input signal.

CHARGE PUMP ONLY MODE

In applications where the headphone jack is used as both an output and input port, signals such as a microphone input can appear on the headphone amplifier output. Traditional charge pump headphone amplifiers can clamp or distort the signals that appear on their output. Without the charge pump active, generating the negative voltage supply, the internal protection diodes of the amplifier clamp the incoming signal, distorting the negative half cycle, see Figure 24. The LM48822 charge pump only mode eliminates this problem. In charge pump only mode, the amplifiers are disabled, while the charge pump remains active. The disabled amplifier outputs present a high impedance (1MΩ) load to the incoming signal. The charge pump maintains the negative rail, allowing the incoming signal to swing between V_{DD} and V_{SS} without any interference from the device.

Set bit B4 (CP_ONLY) of the MODE CONTROL register to 1 for charge pump only mode. Setting CP_ONLY = 1 disables both the left and right channels, regardless of the status of the shutdown control bits. Set CP_ONLY = 0 for normal operation.

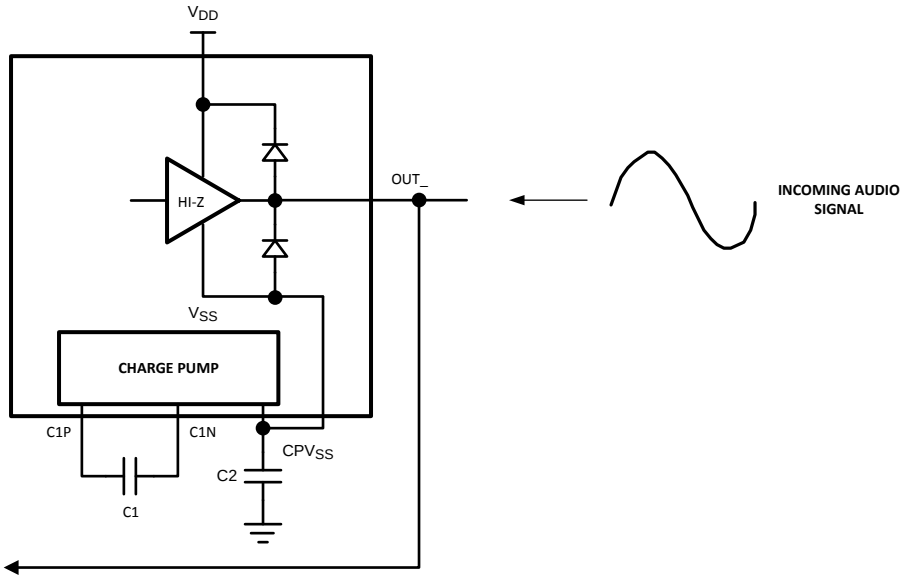


Figure 24. Back-Driving the LM48822 Outputs

COMMON MODE SENSE

The LM48822 features a ground (common mode) sensing feature. In noisy applications, or where the headphone jack is used as a line out to other devices, noise pick up and ground imbalance can degrade audio quality. The LM48822 COM input senses and corrects any noise at the headphone return, or any ground imbalance between the headphone return and device ground, improving audio reproduction. Connect COM directly to the headphone return terminal of the headphone jack Figure 25. No additional external components are required. Connect COM to GND if the common-mode sense feature is not in use.

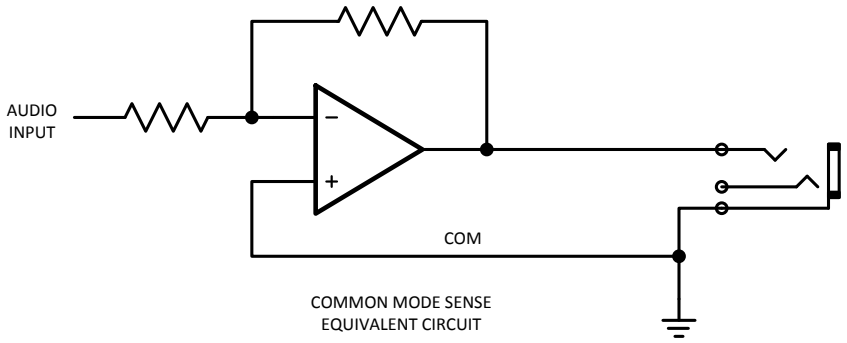


Figure 25. COM Connection Example

VOLUME CONTROL

Table 4. Volume Control Table

VOLUME STEP	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0	HP GAIN (dB)
1	0	0	0	0	0	0	–96
2	0	0	0	0	0	1	–60
3	0	0	0	0	1	0	–57
4	0	0	0	0	1	1	–54
5	0	0	0	1	0	0	–51
6	0	0	0	1	0	1	–48
7	0	0	0	1	1	0	–45
8	0	0	0	1	1	1	–42
9	0	0	1	0	0	0	–39
10	0	0	1	0	0	1	–36
11	0	0	1	0	1	0	–34.5
12	0	0	1	0	1	1	–33
13	0	0	1	1	0	0	–31.5
14	0	0	1	1	0	1	–30
15	0	0	1	1	1	0	–28.5
16	0	0	1	1	1	1	–27
17	0	1	0	0	0	0	–25.5
18	0	1	0	0	0	1	–24
19	0	1	0	0	1	0	–22.5
20	0	1	0	0	1	1	–21
21	0	1	0	1	0	0	–19.5
22	0	1	0	1	0	1	–18
23	0	1	0	1	1	0	–16.5
24	0	1	0	1	1	1	–16
25	0	1	1	0	0	0	–15.5
26	0	1	1	0	0	1	–15
27	0	1	1	0	1	0	–14.5
28	0	1	1	0	1	1	–14
29	0	1	1	1	0	0	–13.5
30	0	1	1	1	0	1	–13
31	0	1	1	1	1	0	–12.5

Table 4. Volume Control Table (continued)

VOLUME STEP	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0	HP GAIN (dB)
32	0	1	1	1	1	1	–12
33	1	0	0	0	0	0	–11.5
34	1	0	0	0	0	1	–11
35	1	0	0	0	1	0	–10.5
36	1	0	0	0	1	1	–10
37	1	0	0	1	0	0	–9.5
38	1	0	0	1	0	1	–9
39	1	0	0	1	1	0	–8.5
40	1	0	0	1	1	1	–8
41	1	0	1	0	0	0	–7.5
42	1	0	1	0	0	1	–7
43	1	0	1	0	1	0	–6.5
44	1	0	1	0	1	1	–6
45	1	0	1	1	0	0	–5.5
46	1	0	1	1	0	1	–5
47	1	0	1	1	1	0	–4.5
48	1	0	1	1	1	1	–4
49	1	1	0	0	0	0	–3.5
50	1	1	0	0	0	1	–3
51	1	1	0	0	1	0	–2.5
52	1	1	0	0	1	1	–2
53	1	1	0	1	0	0	–1.5
54	1	1	0	1	0	1	–1
55	1	1	0	1	1	0	–0.5
56	1	1	0	1	1	1	0
57	1	1	1	0	0	0	0.5
58	1	1	1	0	0	1	1
59	1	1	1	0	1	0	1.5
60	1	1	1	0	1	1	2
61	1	1	1	1	0	0	2.5
62	1	1	1	1	0	1	3
63	1	1	1	1	1	0	3.5
64	1	1	1	1	1	1	4

SHUTDOWN FUNCTION

The LM48822 features three shutdown controls. Bits B6 (SDL) and B1 (SDR) of the MODE CONTROL register control the left and right channels, respectively. Set the control bits to 1 to disable the corresponding channel. When SDR = 1 and SDL = 0, the right channel is disabled, the right and left inputs are summed and output as a mono signal on the OUTL. When SDL = 1 and SDR = 0, the left channel is disabled, while only the right input signal is output on OUTR. Setting both SDL and SDR = 1 disables both channels, while the charge pump remains active. Bit B6 (SHDN) of the VOLUME CONTROL register is the global shutdown control for the entire device. Set SHDN = 1 to disable the entire device; both amplifiers and charge pump are disabled. Set SHDN = 0 for normal operation. SHDN = 1 overrides any other shutdown control bit.

MUTE FUNCTION

Set bits B2 (MUTE_LEFT) and B0 (MUTE_RIGHT) of the MODE CONTROL register to 1 to mute the respective channels. Set MUTE_LEFT and MUTE_RIGHT to 0 for normal operation.

SD_BIAS FUNCTION

The LM48822 BIAS is controlled through the I^2C interface. Set bit B5 (SD_BIAS) of the MODE CONTROL register to 1 to enable the LM48822 BIAS. BIAS provides the voltage for both the amplifiers and the charge pump. When enabled, V_{BIAS} will track V_{DD} for V_{DD} < 3V. Once V_{DD} exceeds 3V, V_{BIAS} remains fixed at 3V, limiting the output swing of the device the $6V_{P-P}$. Set SD_BIAS = 0 to disable BIAS. Disabling BIAS allows the amplifier and charge pump to track V_{DD}, increasing output swing; however, a slight degradation in PSSR will occur. Limit V_{DD} to 4.2V or less when BIAS is disabled.

PROPER SELECTION OF EXTERNAL COMPONENTS

Power Supply Bypassing/Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the supply pins as possible. Place a 1µF ceramic capacitors from V_{DD} to GND. Additional bulk capacitance may be added as required.

Charge Pump Capacitor Selection

Use low ESR ceramic capacitors (less than 100mΩ) for optimum performance.

Charge Pump Flying Capacitor (C1)

The flying capacitor (C1) affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2µF, the $R_{DS(ON)}$ of the charge pump switches and the ESR of C1 and C2 dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Charge Pump Flying Capacitor (C2)

The value and ESR of the hold capacitor (C2) directly affects the ripple on CPV_{SS}. Increasing the value of C2 reduces output ripple. Decreasing the ESR of C2 reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Input Capacitor Selection

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48822. The input capacitors create a high-pass filter with the input resistors R_{IN}. The -3dB point of the high pass filter is found using Equation 1 below.

$$f = 1 / 2\pi R_{IN} C_{IN} \quad (Hz) \tag{1}$$

where:

the value of R_{IN} is given in the Electrical Characteristics Table.

High pass filtering the audio signal helps protect the speakers. When the LM48822 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

SINGLE-ENDED AUDIO AMPLIFIER CONFIGURATION

The LM48822 is compatible with single-ended sources. Figure 26 shows the typical single-ended applications circuit.

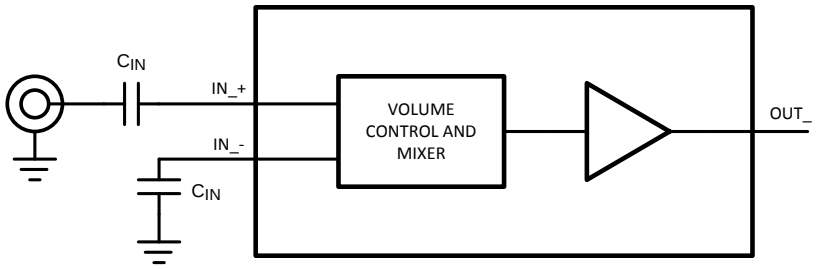


Figure 26. Single-Ended Input Configuration

PCB LAYOUT CONFIGURATION

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM48822 and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

LM48822TL Demoboard of Materials

Table 5. LM48822TL Demoboard Bill of Materials

Designator	Quantity	Description
C1	1	10µF ±10% 16V 500Ω Tantalum Capacitor (B Case) AVX TPSB106K016R0500
C2	1	1µF ±10% 16V X5R Ceramic Capacitor (603) Panasonic ECJ-1VB1C105K
C3, C8, C9	3	2.2µF ±10% 10V X5R Ceramic Capacitor (603) Panasonic ECJ-1VB1A225K
C4 — C7	4	1µF ±10% 16V X7R Ceramic Capacitor (1206) Panasonic ECJ-3YB1C105K
R1, R2	2	5kΩ ±5% 1/10W Thick Film Resistor (603) Vishay CRCW06035R1KJNEA
J1	1	Stereo Headphone Jack
J2	1	16-Pin Boardmount Socket 3M 8516-4500JL
JU1	1	3 Pin Header
JU2	1	2 Pin Header
LM4822TL	1	LM48822TL (16-Bump DSBGA)

Demoboard Schematic

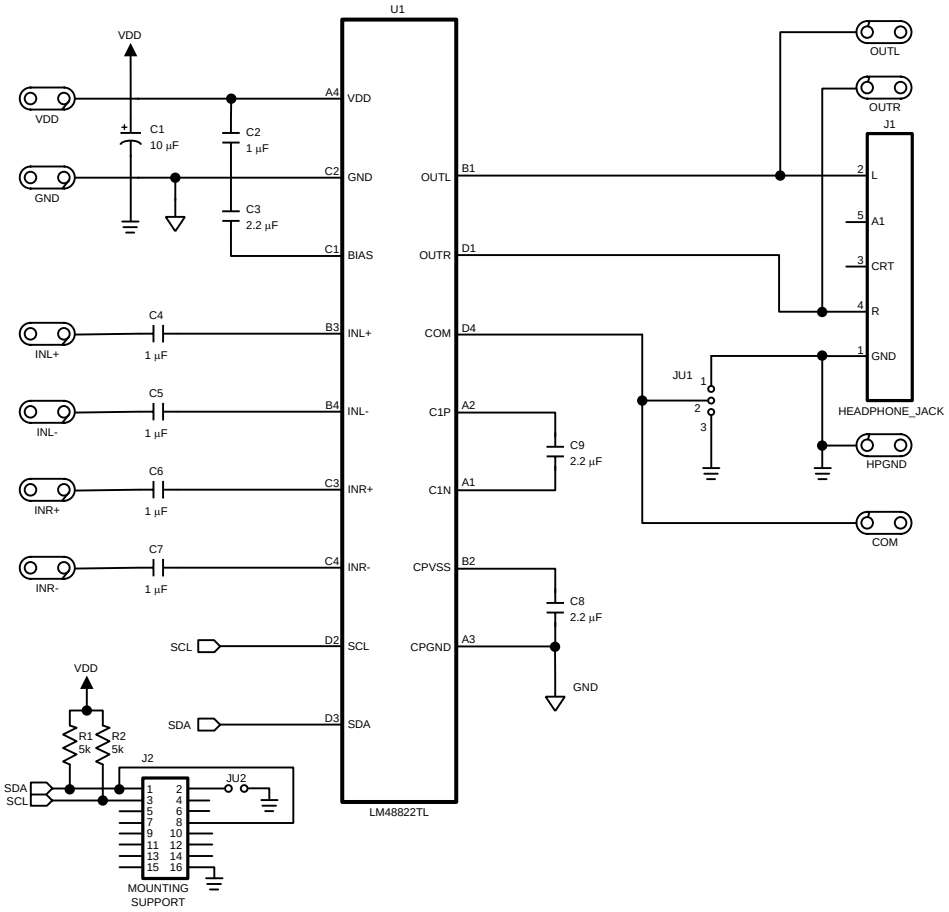


Figure 27. LM48822 Demoboard Schematic

Demonstration Board PCB Layout

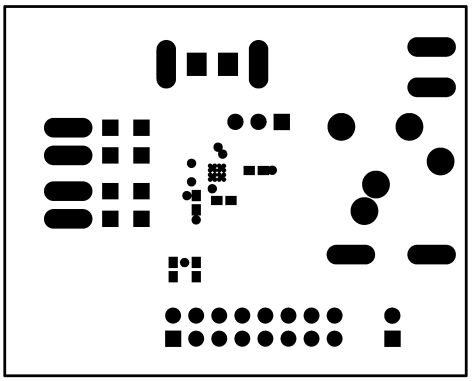


Figure 28. Solder Mask

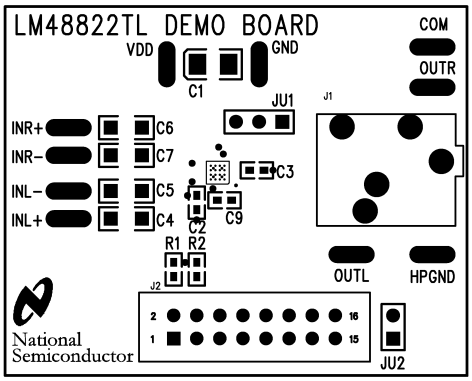


Figure 29. Top Silkscreen

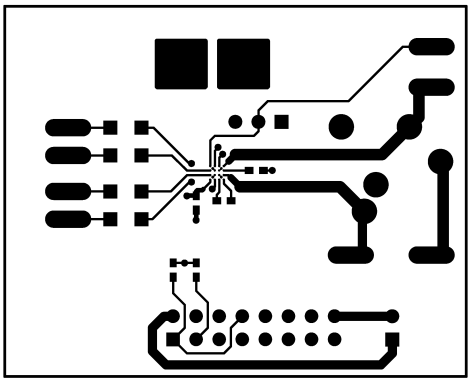


Figure 30. Top Layer

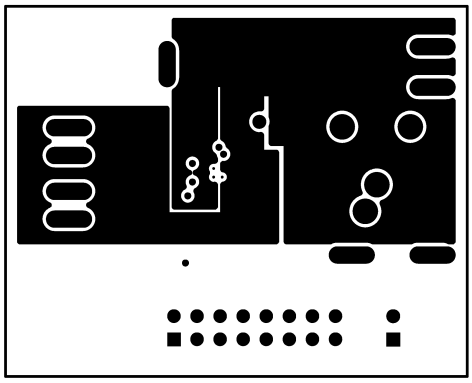


Figure 31. Layer 2 (GND)

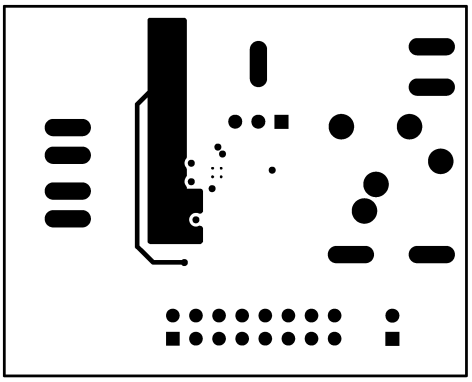


Figure 32. Layer 3 (V_{DD})

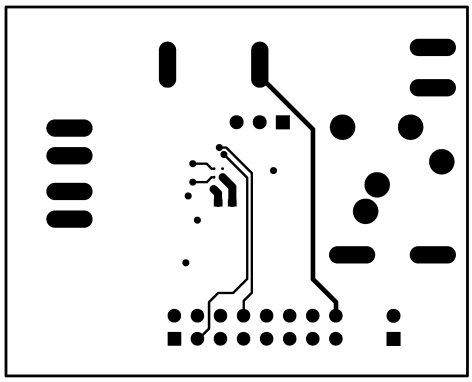


Figure 33. Bottom Layer

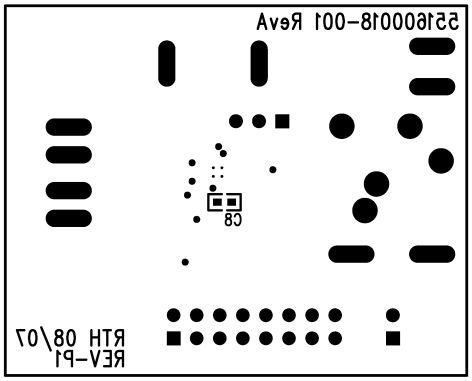


Figure 34. Bottom Silkscreen

Revision History

Rev	Date	Description
0.1	04/15/08	Initial PDF.
0.2	04/23/08	Added the demo boards and schematic.
0.3	04/30/08	Text edits.
0.4	07/10/08	Text edits.
0.5	03/09/11	Changed the bit B7 into B6 under the SHUTDOWN FUNCTION section.
C	05/02/2013	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM48822TL/NOPB	ACTIVE	DSBGA	YZR	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GK1	Samples
LM48822TLX/NOPB	ACTIVE	DSBGA	YZR	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GK1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

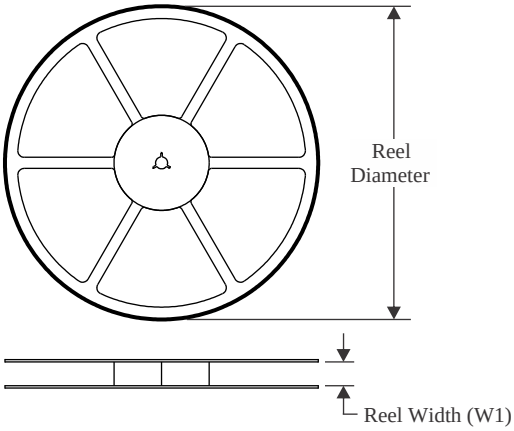
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

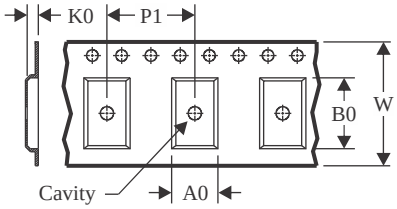
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

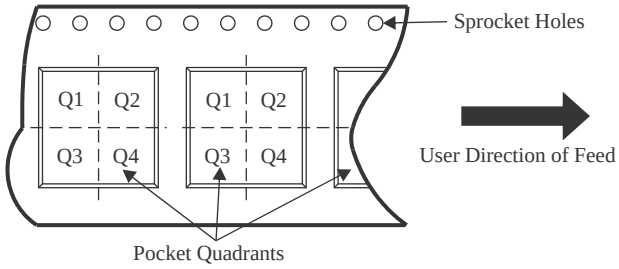


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

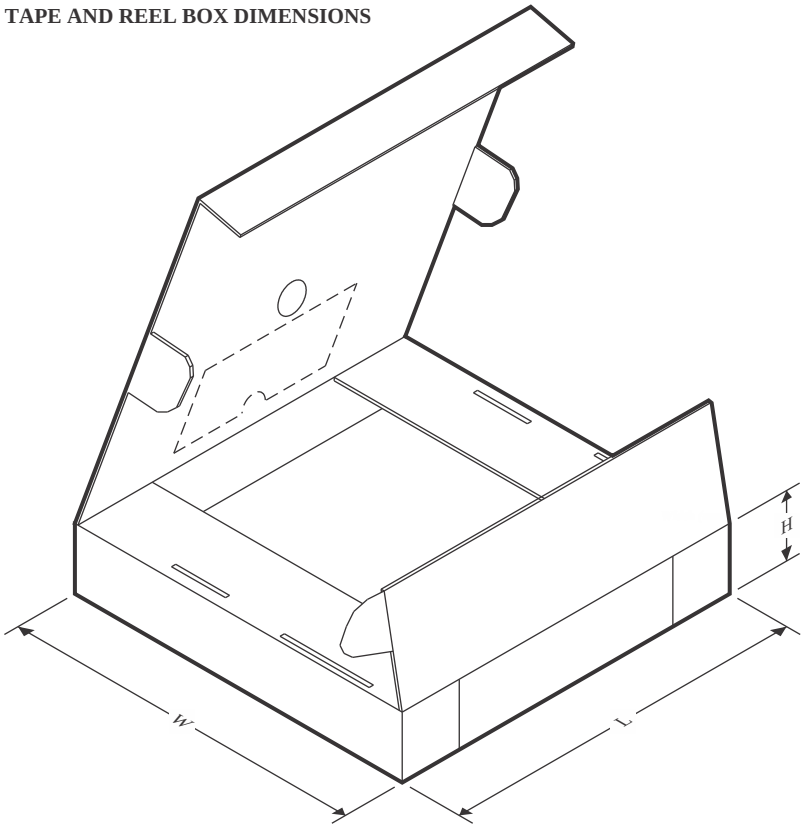
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM48822TL/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM48822TLX/NOPB	DSBGA	YZR	16	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

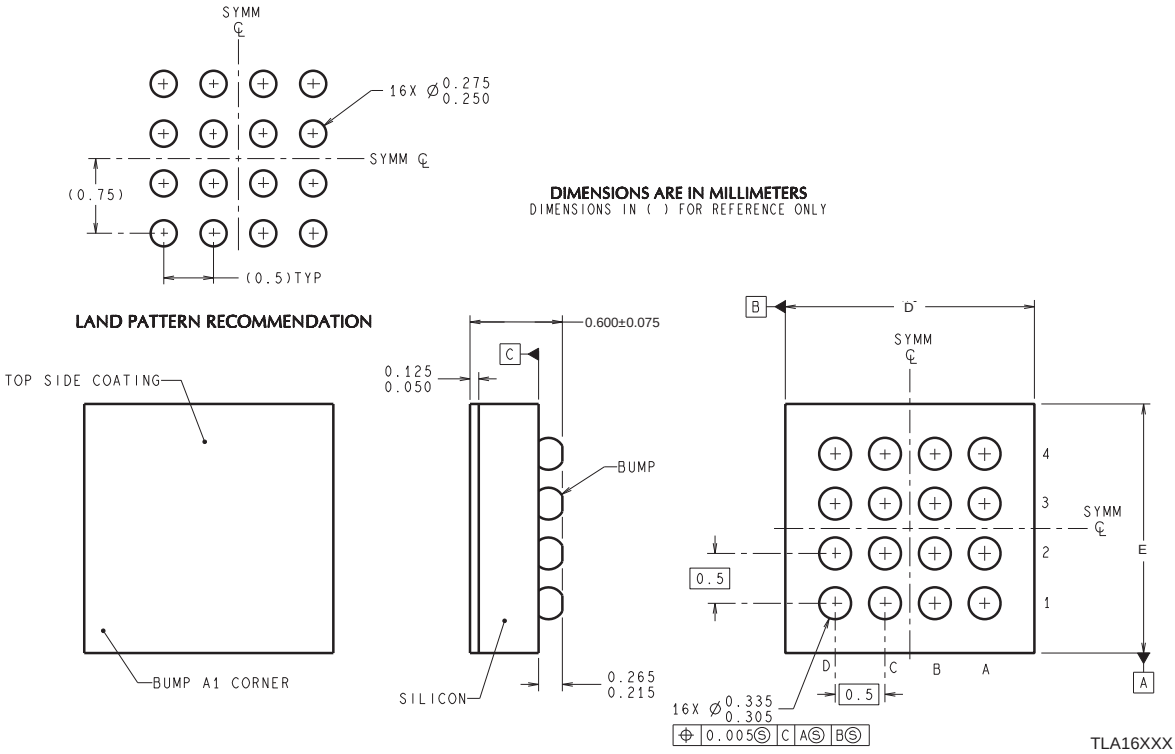
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM48822TL/NOPB	DSBGA	YZR	16	250	208.0	191.0	35.0
LM48822TLX/NOPB	DSBGA	YZR	16	3000	208.0	191.0	35.0

YZR0016



D: Max = 1.99 mm, Min = 1.93 mm

E: Max = 1.99 mm, Min = 1.93 mm

4215051/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265