LM48560 Boomer™ Audio Power Amplifier Series High Voltage Class H Ceramic Speaker Driver With Automatic Level Control

1 Features

- Class H Topology
- Integrated Boost Converter
- Bridge-Tied Load (BTL) Output
- Selectable Differential Inputs
- Selectable Control Interfaces
  - (Hardware or Software mode)
- I^2C Programmable ALC
- Low Supply Current
- Minimum External Components
- Micro-Power Shutdown
- Available in Space-Saving DSBGA Package
- Key Specifications:
  - Output Voltage at V_{DD} = 3.6 V, R_L = 1.5 µF + 10 Ω, THD+N ≤ 1%
    - 30 V_{P-P} (Typical)
  - Quiescent Power Supply Current at 3.6 V (ALC Enabled)
    - 4 mA (Typical)
  - Power Dissipation at 25 V_{P-P}, 1 W (Typical)
  - Shutdown Current, 0.1 µA (Typical)

2 Applications

- Touch Screen Smart Phones
- Tablet PCs
- Portable Electronic Devices
- MP3 Players

3 Description

The LM48560 device is a high voltage, high efficiency, Class H driver for ceramic speakers and piezo actuators. The LM48560 device's Class H architecture offers significant power savings compared to traditional Class AB amplifiers. The device provides 30 V_{P-P} output drive while consuming just 4 mA of quiescent current from a 3.6 V supply.

The LM48560 device features TI's unique automatic level control (ALC) that provides output limiter functionality. The LM48560 device features two fully differential inputs with separate gain settings, and a selectable control interface. In software control mode, the gain control and device modes are configured through the I^2C interface. In hardware control mode, the gain and input mux are configured through a pair of logic inputs.

The LM48560 device has a low power shutdown mode that reduces quiescent current consumption to 0.1 µA. The LM48560 device is available in an ultra-small 16–bump DSBGA package (1.97 mm × 1.97 mm).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM48560	DSBGA (16)	1.97 mm × 1.97 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit

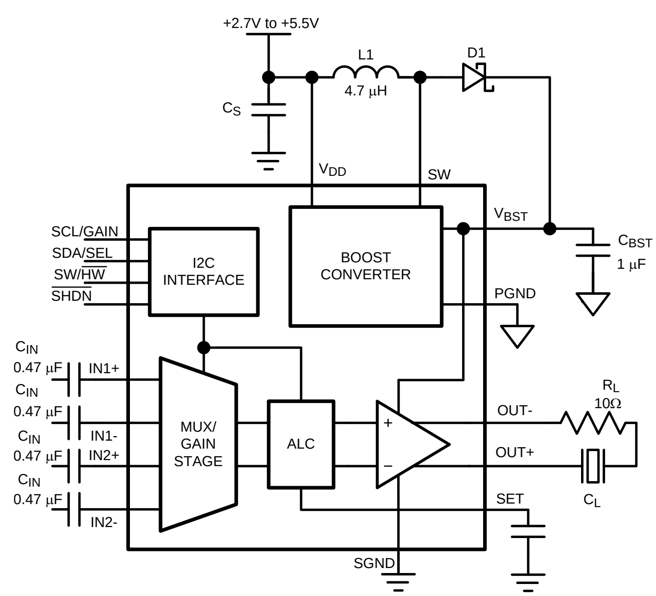


Table of Contents

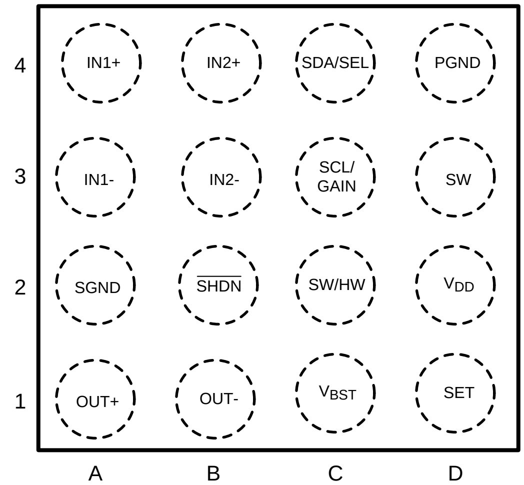
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Rev	Date	Description
1.0	08/16/11	Initial WEB released.
1.01	09/21/11	Input edits under CLASS H OPERATION.
1.02	11/01/11	Edited curves 30150753, 54, 55, 56, and Figure 26 (I^2C Read Cycle).
1.03	11/10/11	Edited Figure 26.
1.04	07/25/12	Input texts/limits edits in the EC table.
1.05	08/22/12	Edited Table 1 and Table 2.
E	05/02/2013	Changed layout of National Data Sheet to TI format.
F	10/21/2015	Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.

5 Pin Configuration and Functions

YZR Package
16-Pin DSBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	OUT+	O	Amplifier Non-Inverting Output
A2	SGND	—	Amplifier Ground
A3	IN1–	I	Amplifier Inverting Input 1
A4	IN1+	I	Amplifier Non-Inverting Input 1
B1	OUT–	O	Amplifier Inverting Output
B2	$\overline{\text{SHDN}}$	I	Active Low Shutdown. Connect $\overline{\text{SHDN}}$ to GND to disable device. Connect $\overline{\text{SHDN}}$ to V_{DD} for normal operation
B3	IN2–	I	Amplifier Inverting Input 2
B4	IN2+	I	Amplifier Non-Inverting Input 2
C1	V_{BST}	—	Boost Converter Output
C2	SW/$\overline{\text{HW}}$	I	Mode Selection Control: SW/$\overline{\text{HW}}$ = 0 → Hardware Mode SW/$\overline{\text{HW}}$ = 1 → Software Mode
C3	SCL/GAIN	I	I^2C Serial Clock Input (Software Mode) Gain Select Input (Hardware Mode) see (Table 5)
C4	SDA/SEL	I/O	I^2C Serial Data Input (Software Mode) Amplifier Input Select (Hardware Mode) see (Table 5)
D1	SET	—	ALC Timing Input
D2	V_{DD}	—	Power Supply
D3	SW	—	Boost Converter Switching Node
D4	PGND	—	Boost Converter Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{DD}	Supply voltage[2]		6	V
SW	Voltage		25	V
V_{BST}	Voltage		21	V
	Input voltage	–0.3	V_{DD} 0.3	V
	Power dissipation[3]	Internally limited		
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, $θ_{JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} – T_A) / θ_{JA}$ or the given in *Absolute Maximum Ratings*, whichever is lower.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	
		Machine Model[3]	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Machine model, applicable std. JESD22-A115-A.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating free-air temperature	–40		85	°C
V_{DD}	Supply voltage	2.7		5.5	V

6.4 Electrical Characteristics V_{DD} = 3.6 V

The following specifications apply for R_L = 1.5 µF + 10 Ω, C_{BST} = 1 µF, C_{IN} = 0.47 µF, C_{SET} = 100 nF, A_V = 24 dB unless otherwise specified. Limits apply for T_A = 25 °C.(1)(2)

PARAMETER		TEST CONDITIONS		MIN (3)	TYP (4)	MAX (3)	UNIT
V_{DD}	Supply voltage			2.7		5.5	V
I_{DD}	Quiescent power supply current	V_{IN} = 0 V, R_L = ∞					
		ALC Enabled			4	6	mA
		ALC Disabled			3.6		mA
P_D	Power consumption	V_{OUT} = 25 V_{P-P}, f = 1 kHz			1		W
I_{SD}	Shutdown current	Software Mode			2.5	4.4	µA
		Hardware Mode			0.1	2	µA
T_{WU}	Wake-up time	From Shutdown			15		ms
V_{OS}	Differential output offset voltage	A_V = 24 V			10	90	mV
		A_V = 0 dB (Boost Disabled)			5	20	mV
A_V	Gain (Hardware Mode)	IN1	GAIN = 0	0.5	0	0.5	dB
			GAIN = 1	5.5	6	6.5	dB
		IN2	GAIN = 0	23.5	24	24.5	dB
			GAIN = 1	29.5	30	30.5	dB
	Gain (software mode)	Boost Disabled	GAIN1 = 0, GAIN0 = 0	–0.5	0	0.5	dB
			GAIN1 = 0, GAIN0 = 1	5.5	6	6.5	dB
			GAIN1 = 1, GAIN0 = 0	11.5	12	12.5	dB
			GAIN1 = 1, GAIN0 = 1	17.5	18	18.5	dB
		Boost Enabled	GAIN1 = 0, GAIN0 = 0	20.5	21	21.5	dB
			GAIN1 = 0, GAIN0 = 1	23.5	24	24.5	dB
			GAIN1 = 1, GAIN0 = 0	26.5	27	27.5	dB
			GAIN1 = 1, GAIN0 = 1	29.5	30	30.5	dB
R_{IN}	Gain step size (software mode)				3		dB
	Input resistance	A_V	0 dB	46	50	58	kΩ
			30 dB	46	50	58	kΩ
V_{OUT}	Output voltage	THD+N = 1%					V_{P-P}
		f	200 Hz	25	30		V_{P-P}
			1 kHz	25	30		V_{P-P}
THD+N	Total harmonic distortion + noise	V_{OUT} = 18 V_{P-P}, f = 1 kHz			0.08%		
PSRR	Power supply rejection ratio (Figure 22)	V_{DD} = 3.6 V + 200 mV_{P-P} sine, Inputs = AC GND					dB
		f_{RIPPLE} = 217 Hz		55	78		dB
		f_{RIPPLE} = 1 kHz			76		dB
CMRR	Common mode rejection ratio (Figure 23)	V_{CM} = 200 mV_{P-P} sine					
		f_{RIPPLE} = 217 Hz			68		dB
		f_{RIPPLE} = 1k Hz			78		dB
SNR	Signal-to-noise-ratio	Boost Disabled, A-weighted			107		dB
		Boost Enabled A-weighted			98		dB
ε_{OS}	Output noise	A-weighted					
		A_V	24 dB		134		μV_{RMS}
			0 dB (Boost Disabled)		16		μV_{RMS}

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(3) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.
(4) Typical values represent most likely parametric norms at T_A = 25 ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.

Electrical Characteristics V_{DD} = 3.6 V (continued)

The following specifications apply for R_L = 1.5 μF + 10 Ω, C_{BST} = 1 μF, C_{IN} = 0.47 μF, C_{SET} = 100 nF, A_V = 24 dB unless otherwise specified. Limits apply for T_A = 25 °C.(1)(2)

PARAMETER		TEST CONDITIONS	MIN (3)	TYP (4)	MAX (3)	UNIT
T_A	Attack time	ATK1:ATK0 = 00, C_{SET} = 100 nF		0.83		ms
T_R	Release time	RLT1:RLT0 = 00, C_{SET} = 100 nF		0.5		s
f_{SW}	Boost converter switching frequency			2		MHz
I_{LIMIT}	Boost converter current limit			1.5		A
V_{IH}	Logic high input threshold	$\overline{SHDN}$	1.4			V
V_{IL}	Logic low input threshold	$\overline{SHDN}$			0.5	V
I_{IN}	Input leakage current	$\overline{SHDN}$		0.1	0.2	μA

6.5 I²C Interface Characteristics

The following specifications apply for R_{PU} = 1 kΩ to V_{DD}, SW/$\overline{HW}$ = 1 (Software Mode) unless otherwise specified. Limits apply for T_A = 25 °C. (1)(2)

PARAMETER		TEST CONDITIONS	MIN (3)	TYP (4)	MAX (3)	UNIT
V_{IH}	Logic Input High Threshold	SDA, SCL	1.1			V
V_{IL}	Logic Input Low Threshold	SDA, SCL			0.5	V
	SCL Frequency				400	kHz
t_1	SCL Period		2.5			μs
t_2	SDA Setup Time		250			ns
t_3	SDA Stable Time		250			ns
t_4	Start Condition Time		250			ns
t_5	Stop Condition Time		250			ns

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(3) Typical values represent most likely parametric norms at T_A = 25 ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
(4) Charge device model, applicable std. JESD22-C101-C.

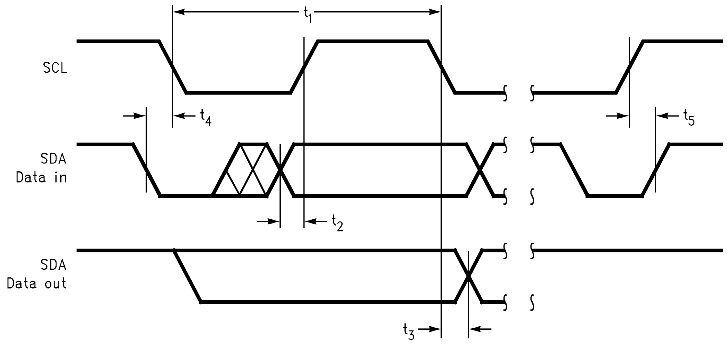


Figure 1. I²C Timing Diagram

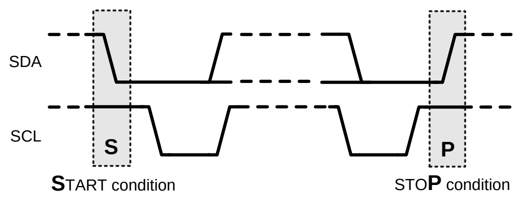


Figure 2. Start and Stop Diagram

6.6 Typical Characteristics

All typical performance curves are taken with conditions seen in *Typical Characteristics*, unless otherwise specified.

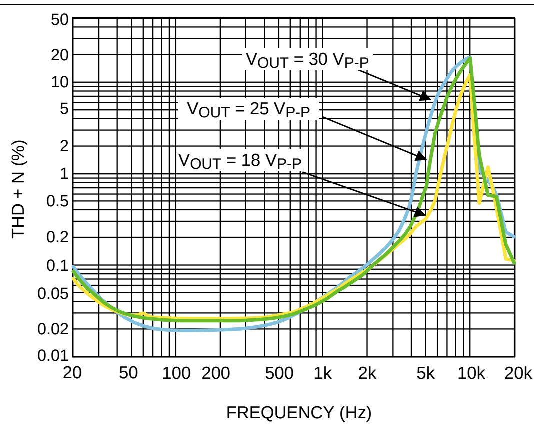


Figure 3. THD+N vs Frequency
C_L = 0.6 µF, V_{DD} = 3.6 V, Boosted, A_V = 24 dB

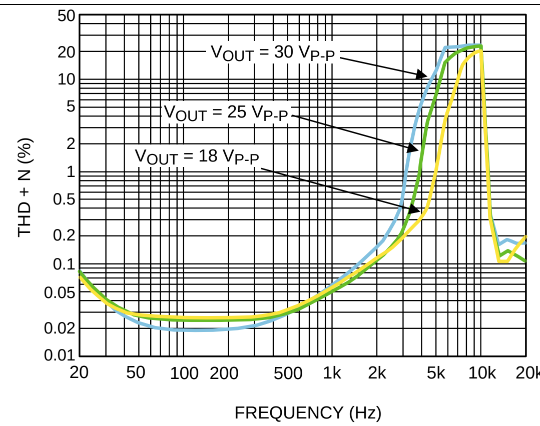


Figure 4. THD+N vs Frequency
C_L = 1 µF, V_{DD} = 3.6 V, Boosted, A_V = 24 dB

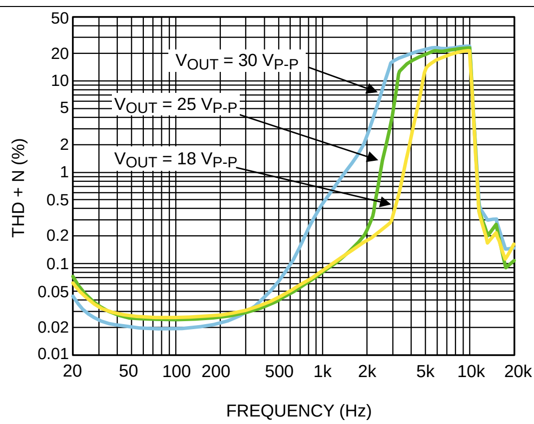


Figure 5. THD+N vs Frequency
C_L = 1.5 µF, V_{DD} = 3.6 V, Boosted, A_V = 24 dB

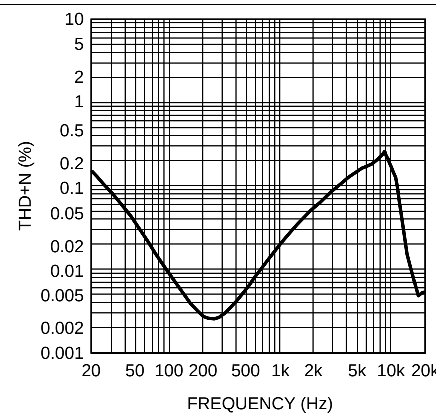


Figure 6. THD+N vs Frequency
V_{DD} = 3.6 V, C_L = 0.6 µF, V_{OUT} = 5 V_{P-P}
Unboosted, A_V = 0 dB

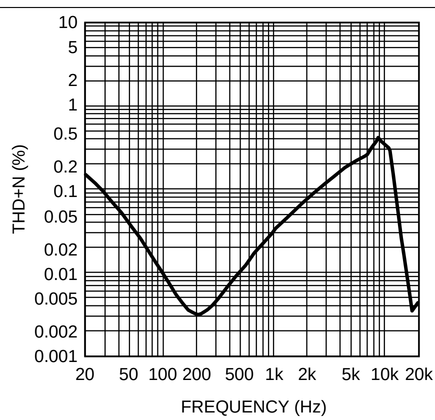


Figure 7. THD+N vs Frequency
V_{DD} = 3.6 V, C_L = 1 µF, V_{OUT} = 5 V_{P-P}
Unboosted , A_V = 0 dB

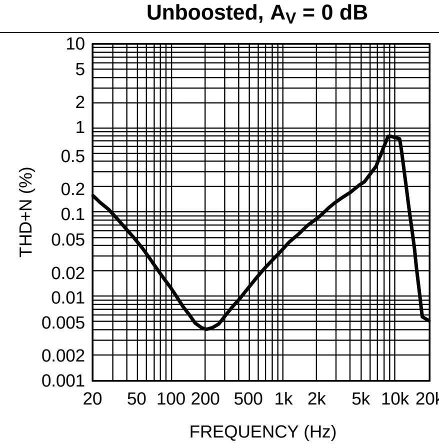


Figure 8. THD+N vs Frequency
V_{DD} = 3.6 V, C_L = 1.5 µF, V_{OUT} = 5 V_{P-P}
Unboosted, A_V = 0 dB

Typical Characteristics (continued)

All typical performance curves are taken with conditions seen in *Typical Characteristics*, unless otherwise specified.

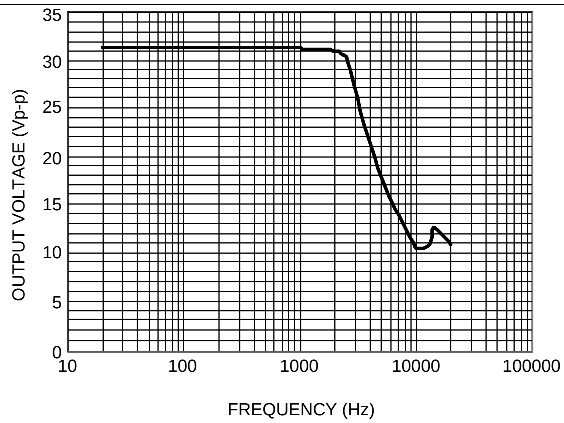


Figure 9. Output Voltage vs Frequency
C_L = 1.5 µF, THD+N ≤ 1%, Boosted

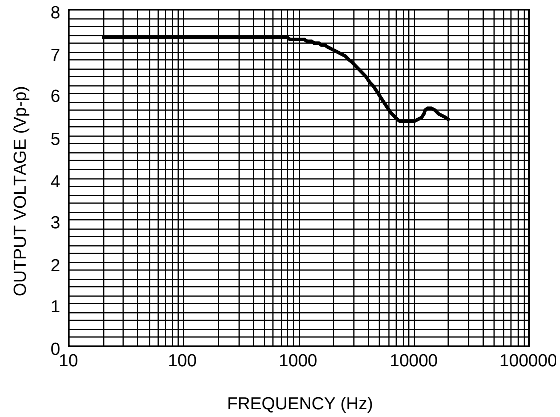


Figure 10. Output Voltage vs Frequency
C_L = 1.5 µF, THD+N ≤ 1%, Unboosted

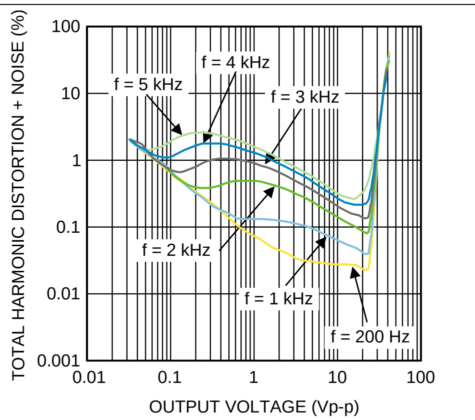


Figure 11. THD+N vs Output Voltage
C_L = 0.6 µF, V_{DD} = 3.6 V, Boosted, A_V = 24 dB

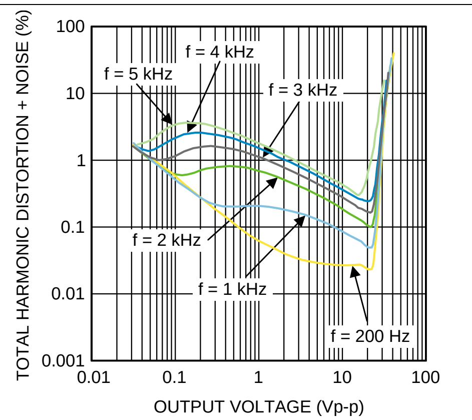


Figure 12. THD+N vs Output Voltage
C_L = 1 µF, V_{DD} = 3.6 V, Boosted, A_V = 24 dB

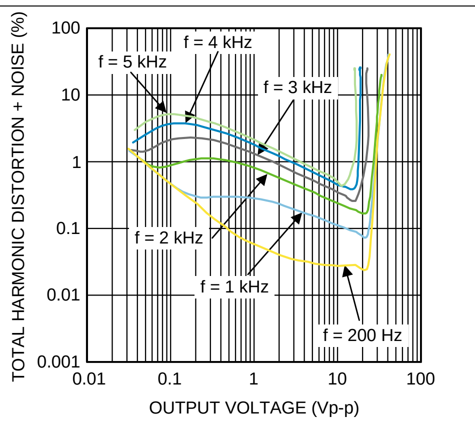


Figure 13. THD+N vs Output Voltage
C_L = 1.5 µF, V_{DD} = 3.6 V, Boosted, A_V = 24 dB

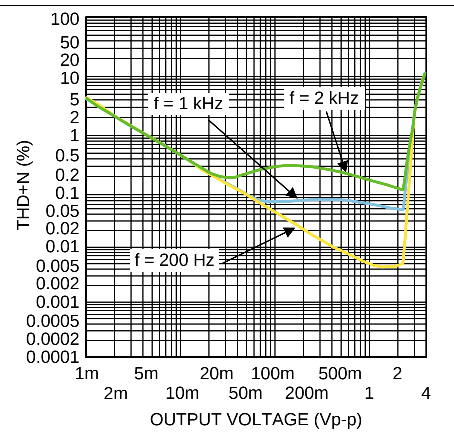


Figure 14. THD+N vs Output Voltage
C_L = 1.5 µF, V_{DD} = 3.6 V, Unboosted, A_V = 0 dB

Typical Characteristics (continued)

All typical performance curves are taken with conditions seen in *Typical Characteristics*, unless otherwise specified.

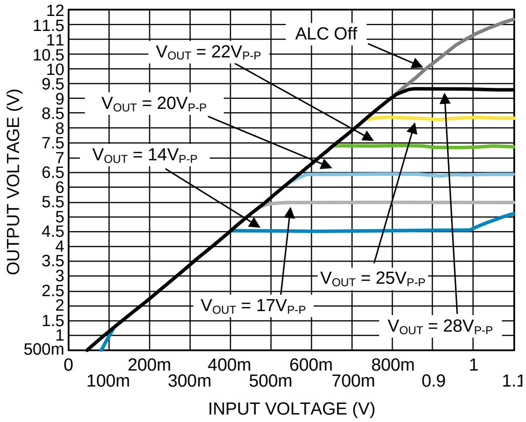


Figure 15. Input Voltage vs Output Voltage
ALC Enabled, A_V = 21 dB, V_{DD} = 3.6 V

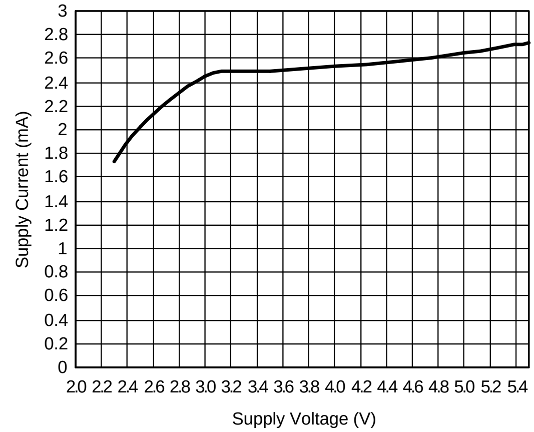


Figure 16. Supply Current vs Supply Voltage
$R_L = \infty$

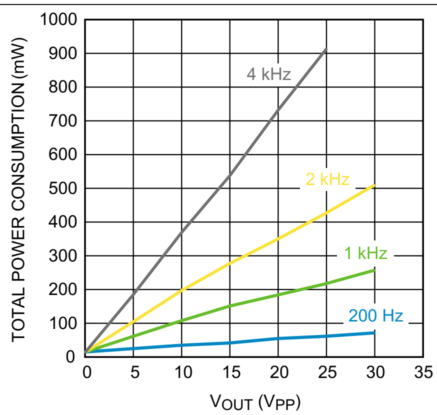


Figure 17. Total Power Consumption vs Output Voltage
V_{DD} = 3.6 V, C_L = 0.6 µF

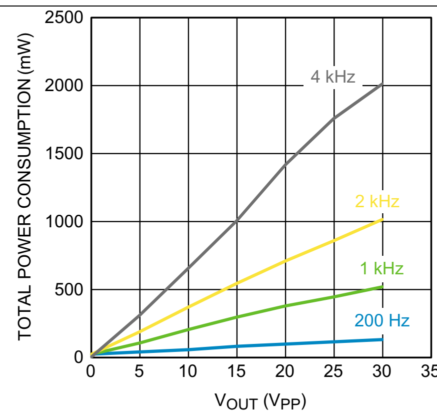


Figure 18. Total Power Consumption vs Output Voltage
V_{DD} = 3.6 V, C_L = 1 µF

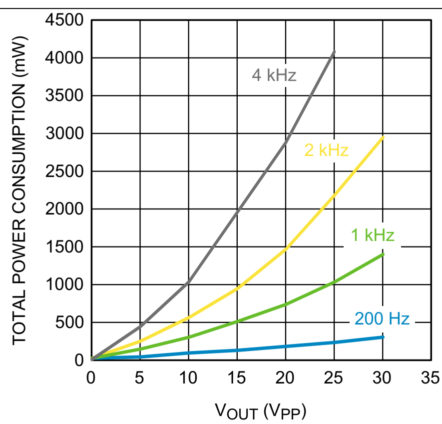


Figure 19. Total Power Consumption vs Output Voltage
V_{DD} = 3.6 V, C_L = 1.5 µF

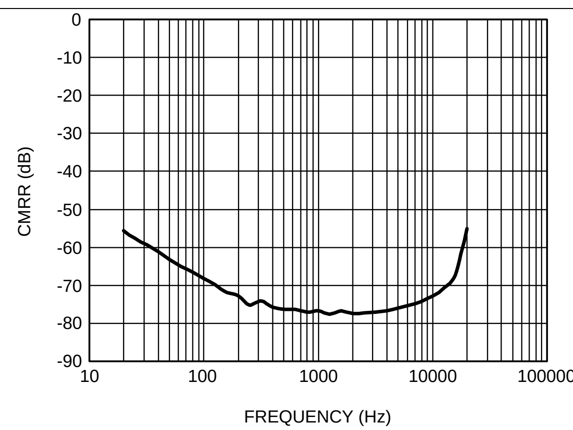


Figure 20. Common Mode Rejection Ratio vs Frequency
V_{CM}= 200 mV_{P-P}, C_{IN} = 10 µF, V_{DD} = 3.6 V, C_L = 1.5 µF

Typical Characteristics (continued)

All typical performance curves are taken with conditions seen in *Typical Characteristics*, unless otherwise specified.

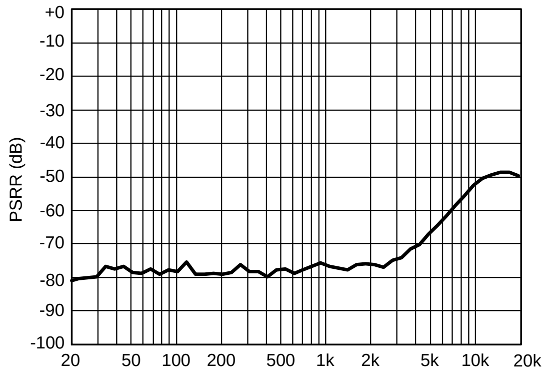


Figure 21. Power Supply Rejection Ratio vs Frequency
V_{RIPPLE} = 200 mV_{P-P}, V_{DD} = 3.6 V, C_L = 1.5 µF

7 Parameter Measurement Information

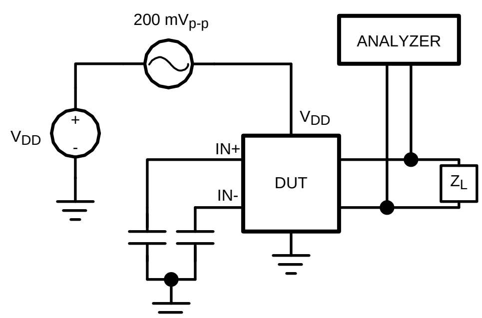


Figure 22. PSRR Test Circuit

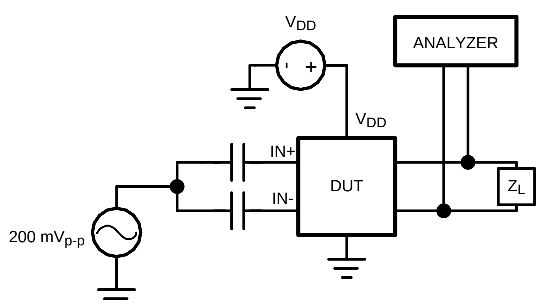


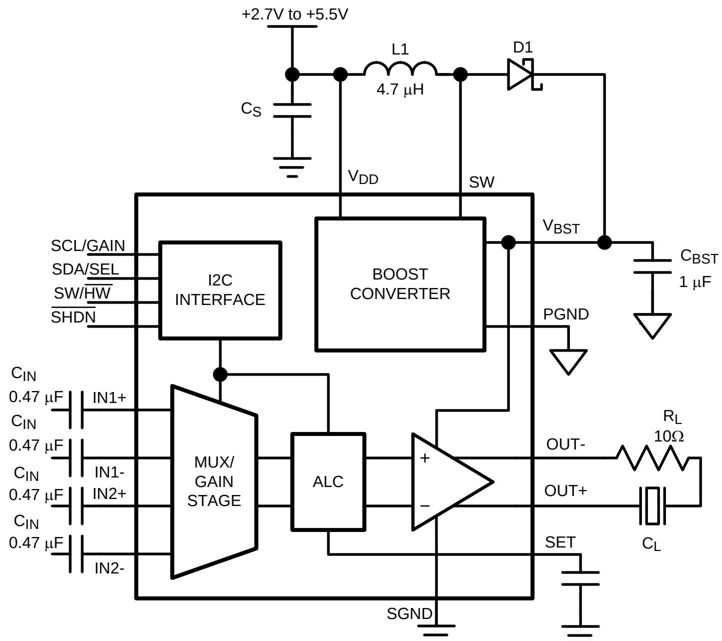
Figure 23. CMRR Test Circuit

8 Detailed Description

8.1 Overview

The LM48560 device is a fully differential Class H driver for ceramic speakers and piezo actuators. The integrated, high efficiency boost converter dynamically adjusts the amplifier's supply voltage based on the output signal to maintain sufficient headroom while improving efficiency. The LM48560 device's Class H architecture offers significant power savings compared to conventional Class AB drivers. The LM48560 features two fully differential inputs with separate gain settings, and a selectable control interface. In software control mode, the gain control and device modes are configured through the I^2C interface. In hardware control mode, the gain and input mux are configured through a pair of logic inputs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 General Amplifier Function

The LM48560 device is a fully differential, Class H piezo driver for ceramic speakers and haptic actuators. The integrated, high efficiency boost converter dynamically adjusts the amplifier's supply voltage based on the output signal, increasing headroom and improving efficiency compared to a conventional Class AB driver. The fully differential amplifier takes advantage of the increased headroom and bridge-tied load (BTL) architecture, delivering significantly more voltage than a single-ended amplifier.

8.3.2 Class H Operation

Class H is a modification of another amplifier class (typically Class B or Class AB) to increase efficiency and reduce power dissipation. To decrease power dissipation, Class H uses a tracking power supply that monitors the output signal and adjusts the supply accordingly. When the amplifier output is below $3V_{P-P}$, the nominal boost voltage is 6 V. As the amplifier output increases above 3 V_{P-P}, the boost voltage tracks the amplifier output as shown in Figure 24. When the amplifier output falls below 3 V_{P-P}, the boost converter returns to its nominal output voltage. Power dissipation is greatly reduced compared to conventional Class AB drivers.

Feature Description (continued)

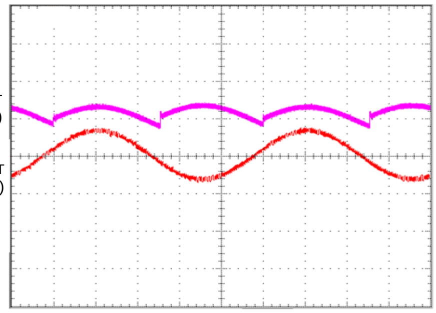


Figure 24. Class H Operation

8.3.3 Differential Amplifier Explanation

The LM48560 device features a fully differential amplifier. A differential amplifier amplifies the difference between the two input signals. A major benefit of the fully differential amplifier is the improved common mode rejection ratio (CMRR) over single ended input amplifiers. The increased CMRR of the differential amplifier reduces sensitivity to ground offset related noise injection, especially important in noisy systems.

8.3.4 Automatic Level Control (ALC)

The ALC is available in software mode only, and only in boosted mode. In hardware mode ALC is always disabled. The ALC limits the peak output voltage to the programmed value. Consequently, it limits the peak boost voltage, as this is derived from the output voltage. The ALC is continuous, in that it provides a continuous adjustment of the voltage gain to limit the output voltage to the programmed value. The available gain adjustment range is typically 8 dB. When the input amplitude is further increased beyond the ALC attenuation range, the output will again increase. This is illustrated in the Typical Performance Graphs, as seen on the 14 V_{PP} plot in the Input voltage vs Output Voltage curve. The attack and decay of the ALC is programmed by software and works in conjunction with the external capacitor C_{SET}. Typically C_{SET} is 0.1 µF, although it can be changed from 0.1 µF to 4.7 µF to select other ranges of attack and decay time.

8.3.5 Attack Time

Attack time ($t_{ATK)}$ is the time it takes for the gain to be reduced by 6 dB once the audio signal exceeds the ALC threshold. Fast attack times allow the ALC to react quickly and prevent transients such as symbol crashes from being distorted. However, fast attack times can lead to volume pumping, where the gain reduction and release becomes noticeable, as the ALC cycles quickly. Slower attack times cause the ALC to ignore the fast transients, and instead act upon longer, louder passages. Selecting an attack time that is too slow can lead to increased distortion in the case of the No Clip function, and possible output overload conditions in the case of the Voltage limiter. The attack time is set by a combination of the value of C_{SET} and the attack time coefficient as given by Equation 1:

$$t_{ATK} = 20\ k\Omega C_{SET} / \alpha_{ATK} \quad (1)$$

Where α_{ATK} is the attack time coefficient (Table 1) set by bits B4:B3 in the Voltage Limit Control Register. The attack time coefficient allows the user to set a nominal attack time. The internal 20 kΩ resistor is subject to temperature change, and it has tolerance between –11% to +20%.

Table 1. Attack Time Coefficient

B4	B3	α_{ATK}
0	0	2.4
0	1	1.7
1	0	1.3
1	1	0.9

8.3.6 Release Time

Release time (t_{RL}) is the time it takes for the gain to return from 6 dB to its normal level once the audio signal returns below the ALC threshold. A fast release time allows the ALC to react quickly to transients, preserving the original dynamics of the audio source. However, similar to a fast attack time, a fast release time contributes to volume pumping. A slow release time reduces the effect of volume pumping. The release time is set by a combination of the value of C_{SET} and release time coefficient as given by Equation 2:

$$t_{RL} = 20\ M\Omega C_{SET} / \alpha_{RL} \quad (s) \tag{2}$$

where α_{RL} is the release time coefficient (Table 2) set by bits B6:B5 in the No Clip Control Register. The release time coefficient allows the user to set a nominal release time. The internal 20 MΩ is subject to temperature change, and it has tolerance between -11% to +20%.

Table 2. Release Time Coefficient

B6	B5	α_{RL}
0	0	4
0	1	5.3
1	0	9.5
1	1	11.8

8.3.7 Boost Converter

The LM48560 device features an integrated boost converter with a dynamic output control. The device monitors the output signal of the amplifier, and adjusts the output voltage of the boost converter to maintain sufficient headroom while improving efficiency.

8.3.8 Gain Setting

The LM48560 device features four internally configured gain settings 0 db, 6 dB, and 30 dB. The device gain is selected through a single pin (GAIN). The gain settings are shown in Table 3.

Table 3. Gain Setting

GAIN	GAIN SETTING IN1	GAIN SETTING IN2
0	0 dB	24 dB
1	6 dB	30 dB

8.3.9 Shutdown Function

The LM48560 device features a low current shutdown mode. Set $\overline{SD}$ = GND to disable the amplifier and boost converter and reduce supply current to 0.01 µA.

8.4 Device Functional Modes

8.4.1 Software or Hardware Mode

Device operation in hardware or software mode is determined by the state of the SW/$\overline{HW}$ pin. Connect SW/$\overline{HW}$ to ground for hardware mode, and connect to V_{DD} for software mode.

SW/$\overline{HW}$	SDA/SEL	SCL/GAIN	MODE
0	0 (Boost Disabled)	0	IN1, Av = 0
		1	IN1, Av = 6
	1 (Boost Enabled)	0	IN2, Av = 24
		1	IN2, Av = 30
1	SDA	SCL	I^2C Mode

8.4.2 Single-Ended Input Configuration

The LM48560 device is compatible with single-ended sources. When configured for single-ended inputs, input capacitors must be used to block and DC component at the input of the device. Figure 25 shows the typical single-ended applications circuit.

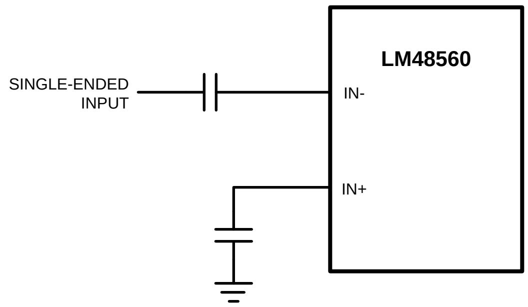


Figure 25. Single-Ended Input Configuration

8.5 Programming

8.5.1 Read/Write I²C Compatible Interface

The LM48560 device is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM48560 device and the master can communicate at clock rates up to 400 kHz. Figure 1 shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48560 device is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition Figure 2. Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse Figure 26. The LM48560 device address is 1101111.

8.5.2 Write Sequence

The example write sequence is shown in Figure 26. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/$\overline{W}$ bit (R/$\overline{W}$ = 0 indicating the master is writing to the LM48560 device). The data is latched in on the rising edge of the clock. Each address bit must be stable while SDA is HIGH. After the R/$\overline{W}$ bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48560 device receives the correct address, the device pulls the SDA line low, generating and acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register address word is sent, MSB first. Each data bit should be stable while SCL is HIGH. After the 8-bit register address is sent, the LM48560 device sends another ACK bit. Upon receipt of the acknowledge, the 8-bit register data is sent, MSB first. The register data word is followed by an ACK, upon receipt of which, the master issues a STOP bit, allowing SDA to go high while SDA is high.

Figure 26. Example I²C Write Cycle

8.5.3 Read Sequence

The example read sequence is shown in Figure 27. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

Programming (continued)

The 7-bit device address is written to the bus, followed by the R/$\overline{W}$ = 1 (R/$\overline{W}$ = 1 indicating the master wants to read data from the LM48560 device). After the R/$\overline{W}$ bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48560 device receives the correct address, the device pulls the SDA line low, generating and acknowledge bit (ACK). Once the master device registers the ACK bit, the 8-bit register address word is sent, MSB first, followed by an ACK and selected register data from the LM48560 device. The register data is sent MSB first. Following the acknowledgment of the register data word [7:0], the master issues a STOP bit, allowing SDA to go high while SDA is high.

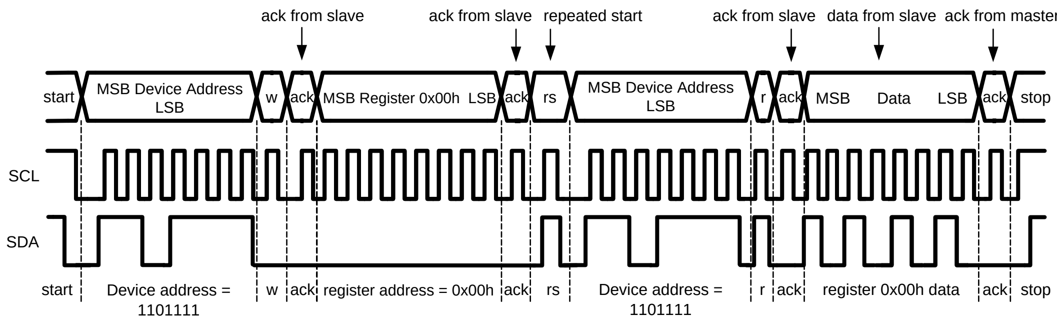


Figure 27. Example I^2C Read Cycle

Table 4. Device Address

	B7	B6	B5	B4	B3	B2	B1	B0 (R/$\overline{W}$)
Device Address	1	1	0	1	1	1	1	0

Table 5. Mode Selection

SW/HW	SDA/SEL	SCL/GAIN	MODE
0	0 (Boost Disabled)	0	IN1, A_V = 0
		1	IN1, A_V = 6
	1 (Boost Enabled)	0	IN2, A_V = 24
		1	IN2, A_V = 30
1	X	X	I^2C Mode

8.6 Register Maps

Table 6. I^2C Control Registers

REGISTER ADDRESS	Register Name	B7	B6	B5	B4	B3	B2	B1	B0
0x00h	SHUTDOWN CONTROL	X	X	X	X	TURN_ON	IN_SEL	BOOST_EN	$\overline{\text{SHDN}}$
0x01h	NO CLIP CONTROL	X	RLT1	RLT0	ATK1	ATK0	PLEV2	PLEV1	PLEV0
0x02h	GAIN CONTROL	X	X	X	X	X	X	GAIN1	GAIN0
0x03h	TEST MODE	X	X	X	X	X	X	X	X

Table 7. Shutdown Control Register

BIT	NAME	VALUE	DESCRIPTION
B7:B4	UNUSED	X	Unused, set to 0
B3	TURN_ON	0	Normal turn on time, t_{WU} = 15 ms
		1	Fast turn on time, t_{WU} = 5 ms

Table 7. Shutdown Control Register (continued)

BIT	NAME	VALUE	DESCRIPTION
B2	IN_SEL	0	Input 1 selected
		1	Input 2 selected
B1	BOOST_EN	0	Boost disabled
		1	Boost enabled
B0	$\overline{\text{SHDN}}$	0	Device shutdown
		1	Device enabled

Table 8. No Clip Control Register

BIT	NAME	VALUE			DESCRIPTION
B7	UNUSED	X			Unused, set to 0
B6:B5	RLT1 (B6) RLT0 (B5)	B6	B5		Sets Release Time based on C_{SET}. See *Release Time* section.
		0	0		T_R = 0.5 s
		0	1		T_R = 0.38 s
		1	0		T_R = 0.21 s
		1	1		T_R = 0.17 s
B4:B3	ATK1 (B4) ATK0 (B3)	B4	B3		Sets Attack Time based on C_{SET}. See *Attack Time* section.
		0	0		T_A = 0.83 ms
		0	1		T_A = 1.2 ms
		1	0		T_A = 1.5 ms
		1	1		T_A = 2.2 ms
B2:B0	PLEV2 (B2) PLEV1 (B1) PLEV0 (B0)	B2	B1	B0	Sets output voltage limit level.
		0	0	0	Voltage Limit disabled
		0	0	1	$V_{TH(VLIM)}$ = 14 V_{P-P}
		0	1	0	$V_{TH(VLIM)}$ = 17 V_{P-P}
		0	1	1	$V_{TH(VLIM)}$ = 20 V_{P-P}
		1	0	0	$V_{TH(VLIM)}$ = 22 V_{P-P}
		1	0	1	$V_{TH(VLIM)}$ = 25 V_{P-P}
		1	1	0	$V_{TH(VLIM)}$ = 28 V_{P-P}
		1	1	1	Voltage Limit disabled

Table 9. Gain Control Register

BIT	NAME	VALUE		DESCRIPTION
B7:B2	UNUSED	X		Unused, set to 0
B1:B0	GAIN1(B1) GAIN0 (B0)	B1	B0	Sets amplifier gain. Boost disabled (BOOST_EN = 0)
		0	0	0 dB
		0	1	6 dB
		1	0	12 dB
		1	1	18 dB
B1:B0	GAIN1(B1) GAIN0 (B0)	B1	B0	Sets amplifier gain. Boost enabled (BOOST_EN = 1)
		0	0	21 dB
		0	1	24 dB
		1	0	27 dB
		1	1	30 dB

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM48560 device is a high voltage, high efficiency Class H driver for ceramic speakers and piezo actuators. The integrated, high efficiency boost converter dynamically adjusts the amplifier's supply voltage based on the output signal to increase headroom and improve efficiency. The LM48560 device's Class H architecture offers significant power savings compared to traditional Class AB amplifiers. The device provides 30Vp-p output drive while consuming just 4 mA of quiescent current from a 3.6 V supply.

The LM48560 device features two fully differential inputs with separate gain settings, and a selectable control interface. In software control mode, the gain control and device modes are configured through the I2C interface. In hardware control mode, the gain and input mux are configured through a pair of logic inputs. The LM48560 device has a low current shutdown mode that disables the amplifier and boost converter and reduces quiescent current consumption to 0.1 µA.

9.2 Typical Application

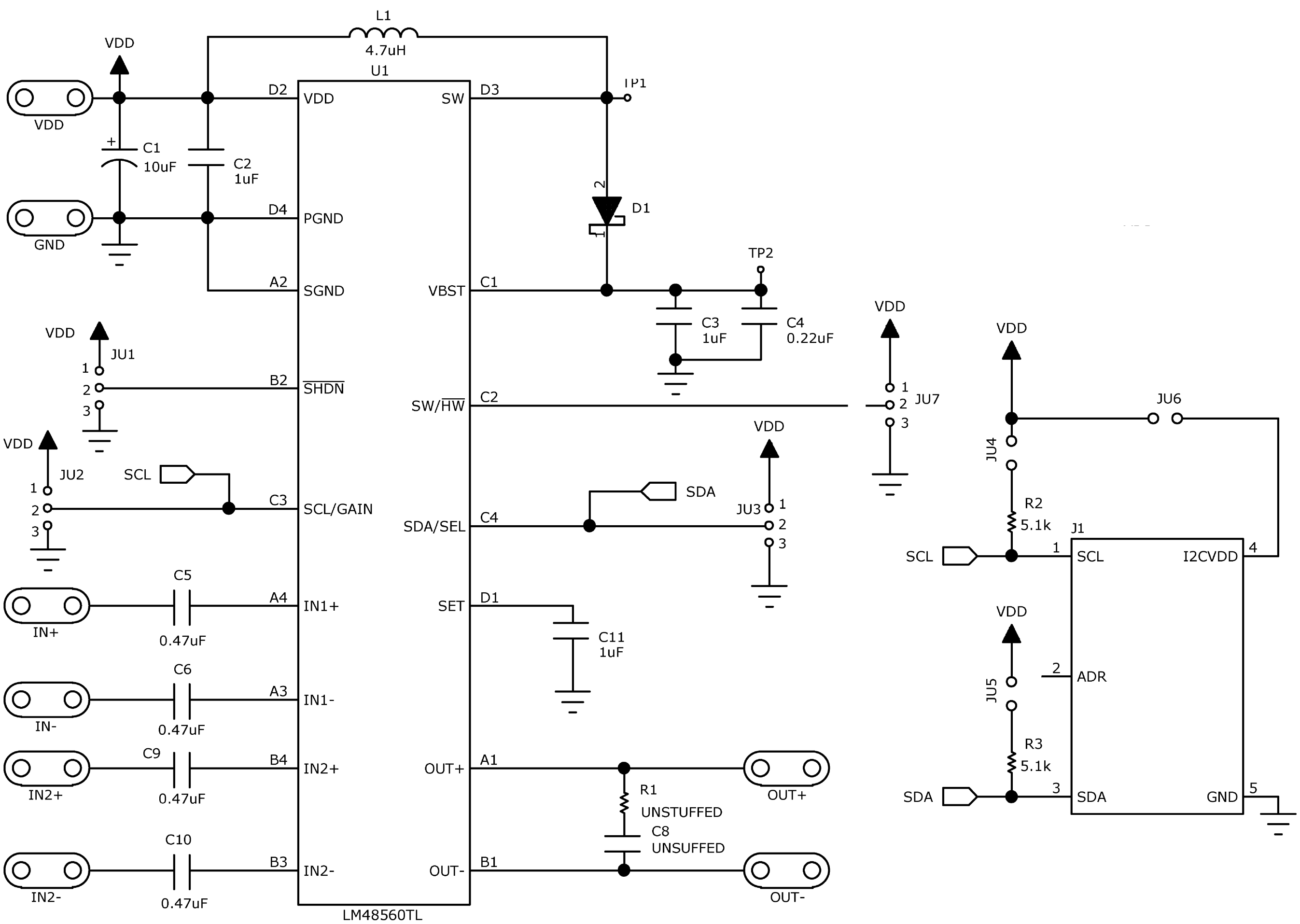


Figure 28. Demo Board Schematic

Typical Application (continued)

9.2.1 Design Requirements

Table 10 shows the design parameters for this design example.

Table 10. Design Parameters

PARAMETERS	VALUES
Supply voltage	2.7 V to 5.5 V
Temperature	–40 °C to 85 °C
Input voltage	–0.3 V to Vdd 0.3 V

9.2.2 Detailed Design Procedure

9.2.2.1 Proper Selection of External Components

9.2.2.1.1 ALC Timing (C_{SET}) Capacitor Selection

The recommended range value of C_{SET} is between 0.01 µF to 1 µF. Lowering the value below 0.01 µF can increase the attack time but LM48560 device ALC ability to regulate its output can be disrupted and approaches the hard limiter circuit. This in turn increases the THD+N and audio quality will be severely affected.

9.2.2.1.2 Power Selection of External Components

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1-µF ceramic capacitor from V_{DD} to GND. Additional bulk capacitance may be added as required.

9.2.2.1.3 Boost Converter Capacitor Selection

The LM48560 device boost converter requires three external capacitors for proper operation: a 1-µF supply bypass capacitor, and 1-µF + 100-pF output reservoir capacitors. Place the supply bypass capacitor as close to V_{DD} as possible. Place the reservoir capacitors as close to VBST and VAMP as possible. Low ESR surface-mount multi-layer ceramic capacitors with X7R or X5R temperature characteristics are recommended. Select output capacitors with voltage rating of 25 V or higher. Tantalum, OS-CON and aluminum electrolytic capacitors are not recommended.

9.2.2.1.4 Inductor Selection

The LM48560 device boost converter is designed for use with a 4.7-µH inductor. Choose an inductor with a saturation current rating greater than the maximum operating peak current of the LM48560 device (> 1A). This ensures that the inductor does not saturate, preventing excess efficiency loss, over heating and possible damage to the inductor. Additionally, choose an inductor with the lowest possible DCR (series resistance) to further minimize efficiency losses.

9.2.2.1.5 Diode Selection

Use a Schottkey diode as shown in Figure 28. A 20-V diode such as the NSR0520V2T1G from On Semiconductor is recommended. The NSR0520V2T1G is designed to handle a maximum average current of 500 mA.

9.2.3 Application Curve

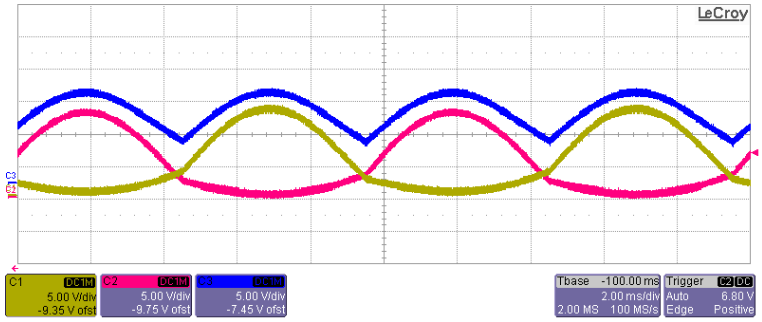


Figure 29. Out+, Out– and Vbst Waveforms for a 100 Hz Input Sine Wave

10 Power Supply Recommendations

The LM48560 device is designed be operate with a power supply between 2.7 V and 5.5 V. Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1-µF ceramic capacitor from VDD to GND. Additional bulk capacitance may be added as required.

11 Layout

11.1 Layout Guidelines

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM48560 device and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

11.2 Layout Example

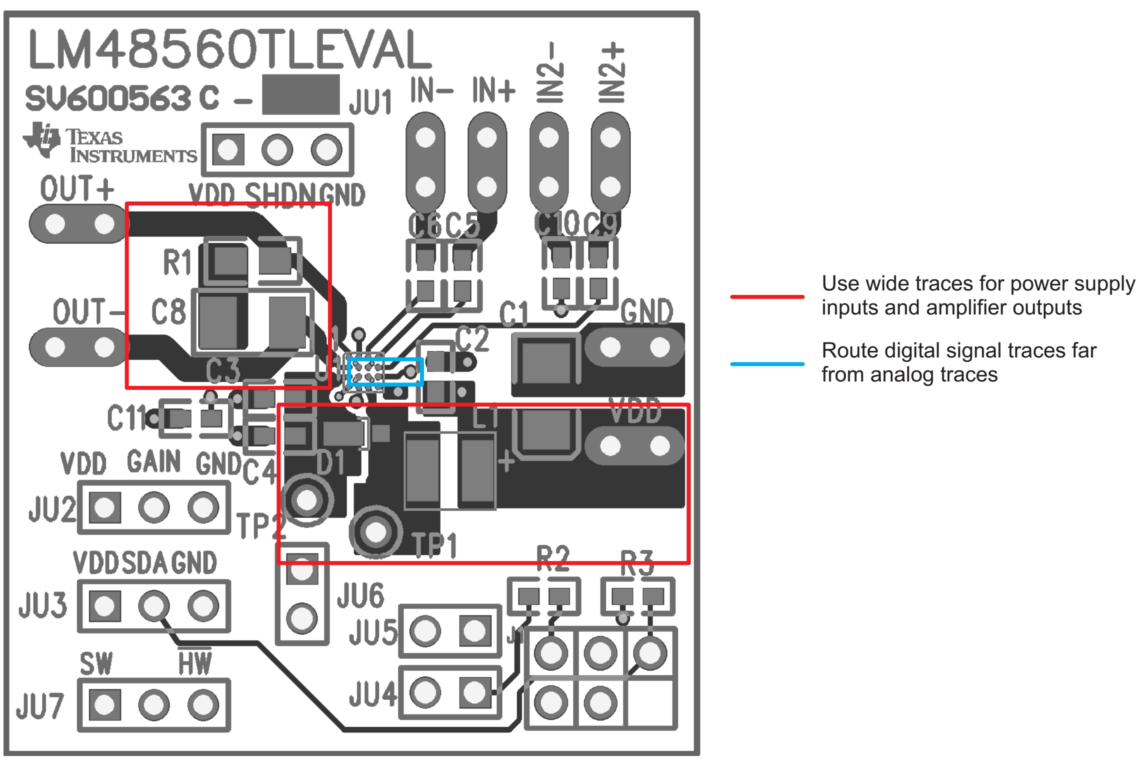


Figure 30. PCB Layout Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM48560TL/NOPB	ACTIVE	DSBGA	YZR	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GO5	Samples
LM48560TLX/NOPB	ACTIVE	DSBGA	YZR	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GO5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

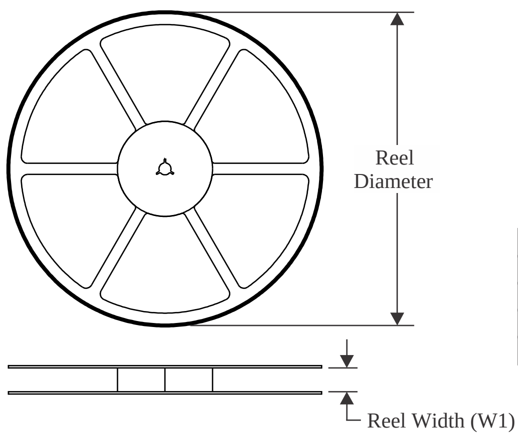
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

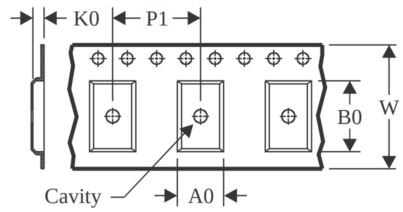
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

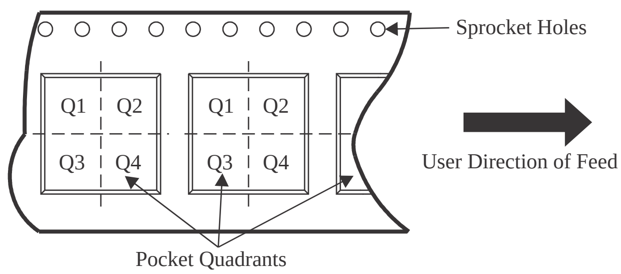


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

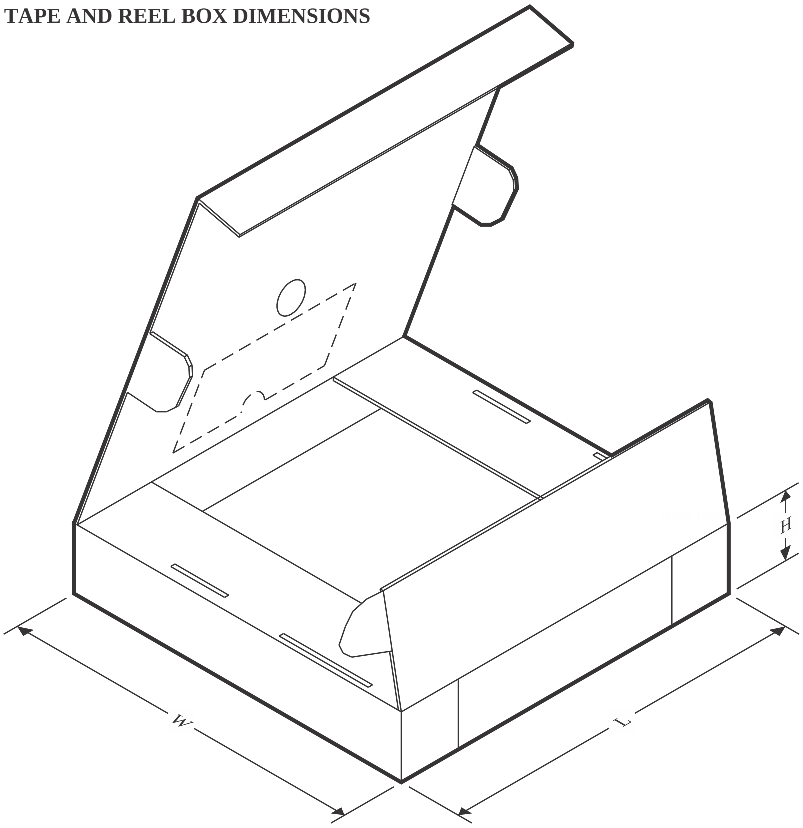
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM48560TL/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM48560TLX/NOPB	DSBGA	YZR	16	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

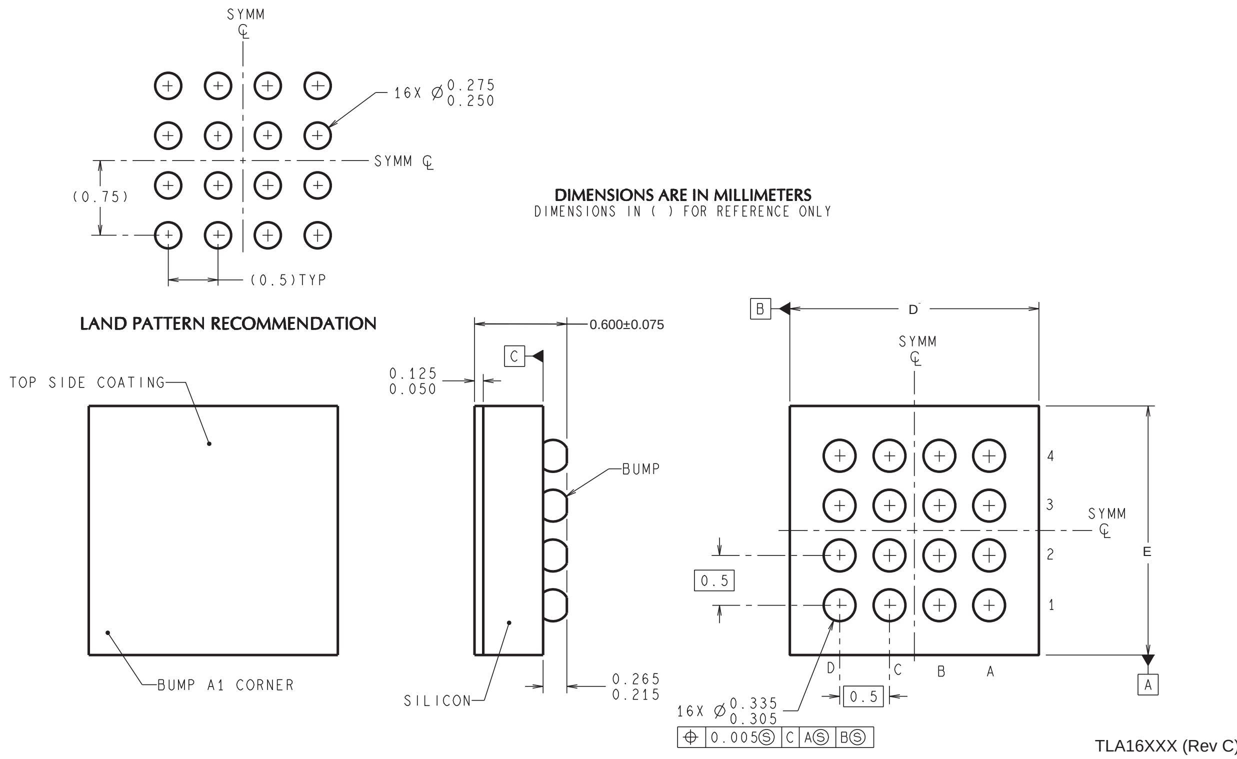
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM48560TL/NOPB	DSBGA	YZR	16	250	208.0	191.0	35.0
LM48560TLX/NOPB	DSBGA	YZR	16	3000	208.0	191.0	35.0

YZR0016



D: Max = 1.99 mm, Min = 1.93 mm	
E: Max = 1.99 mm, Min = 1.93 mm	

4215051/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.