SM72501 SolarMagic Precision, CMOS Input, RRIO, Wide Supply Range Amplifier

Check for Samples: SM72501

FEATURES
- Renewable Energy Grade
- Input Offset Voltage ±200 µV (max)
- Input Bias Current ±200 fA
- Input Voltage Noise 9 nV/√Hz
- CMRR 130 dB
- Open Loop Gain 130 dB
- Temperature Range –40°C to 125°C
- Unity Gain Bandwidth 2.5 MHz
- Supply Current (SM72501) 715 µA
- Supply Voltage Range 2.7V to 12V
- Rail-to-rail Input and Output

APPLICATIONS
- High Impedance Sensor Interface
- Battery Powered Instrumentation
- High Gain Amplifiers
- DAC Buffer
- Instrumentation Amplifier
- Active Filters

DESCRIPTION
The SM72501 is a low offset voltage, rail-to-rail input and output precision amplifier with a CMOS input stage and a wide supply voltage range. The SM72501 is ideal for sensor interface and other instrumentation applications.

The low offset voltage of less than ±200 µV along with the low input bias current of less than ±1 pA makes the SM72501 ideal for precision applications. The SM72501 is built utilizing VIP50 technology, which allows the combination of a CMOS input stage and a 12V common mode and supply voltage range. This makes the SM72501 a great choice in many applications where conventional CMOS parts cannot operate under the desired voltage conditions.

The SM72501 has a rail-to-rail input stage that significantly reduces the CMRR glitch commonly associated with rail-to-rail input amplifiers. This is achieved by trimming both sides of the complimentary input stage, thereby reducing the difference between the NMOS and PMOS offsets. The output of the SM72501 swings within 40 mV of either rail to maximize the signal dynamic range in applications requiring low supply voltage.

The SM72501 is offered in the space saving 5-Pin SOT-23. This small package is an ideal solution for area constrained PC boards and portable electronics.

Typical Application

![Figure 1. Precision Current Source](image)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>ESD Tolerance(3)</th>
<th>Human Body Model</th>
<th>2000V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Machine Model</td>
<td></td>
<td>200V</td>
</tr>
<tr>
<td>Charge-Device Model</td>
<td></td>
<td>1000V</td>
</tr>
<tr>
<td>Supply Voltage (V_S = V^+ – V^-)</td>
<td></td>
<td>±300 mV</td>
</tr>
<tr>
<td>Voltage at Input/Output Pins</td>
<td>V^+ + 0.3V, V^- – 0.3V</td>
<td></td>
</tr>
<tr>
<td>Input Current</td>
<td>10 mA</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>–65°C to +150°C</td>
<td></td>
</tr>
<tr>
<td>Junction Temperature(4)</td>
<td>+150°C</td>
<td></td>
</tr>
<tr>
<td>Soldering Information</td>
<td>Infrared or Convection (20 sec)</td>
<td>235°C</td>
</tr>
<tr>
<td></td>
<td>Wave Soldering Lead Temp. (10 sec)</td>
<td>260°C</td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional. For specifications and the test conditions, see the Electrical Characteristics Tables.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.


(4) The maximum power dissipation is a function of T_J(MAX), θ_JA. The maximum allowable power dissipation at any ambient temperature is P_D = (T_J(MAX) – T_A)/ θ_JA. All numbers apply for packages soldered directly onto a PC Board.

### Operating Ratings

<table>
<thead>
<tr>
<th>Temperature Range(2)</th>
<th>–40°C to +125°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V_S = V^+ – V^-)</td>
<td>2.7V to 12V</td>
</tr>
<tr>
<td>Package Thermal Resistance (θ_JA(2))</td>
<td>265°C/W</td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional. For specifications and the test conditions, see the Electrical Characteristics Tables.

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3V Electrical Characteristics

Unless otherwise specified, all limits are specified for $T_A = 25^\circ C$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V^+/2$, and $R_L > 10 \, k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min $^{(2)}$</th>
<th>Typ $^{(3)}$</th>
<th>Max $^{(2)}$</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td></td>
<td>$\pm 37$</td>
<td>$\pm 200$</td>
<td>$\pm 500$</td>
<td>$\mu V$</td>
</tr>
<tr>
<td>$TCV_{OS}$</td>
<td>Input Offset Voltage Temperature Drift</td>
<td>See $^{(4)}$</td>
<td>$\pm 1$</td>
<td>$\pm 5$</td>
<td></td>
<td>$\mu V/^\circ C$</td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input Bias Current</td>
<td>See $^{(4)}$ $-40^\circ C \leq T_A \leq 85^\circ C$</td>
<td>$\pm 0.2$</td>
<td>$\pm 1$</td>
<td>$\pm 50$</td>
<td>$pA$</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current</td>
<td></td>
<td>40</td>
<td></td>
<td></td>
<td>fA</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>$0V \leq V_{CM} \leq 3V$</td>
<td>86</td>
<td>130</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>$2.7V \leq V^+ \leq 12V$, $V_o = V^+/2$</td>
<td>86</td>
<td>98</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>CMVR</td>
<td>Common Mode Voltage Range</td>
<td>$CMRR \geq 80 , dB$, $CMRR \geq 77 , dB$</td>
<td>-0.2</td>
<td>3.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$A_{VOL}$</td>
<td>Open Loop Voltage Gain</td>
<td>$R_L = 2 , k\Omega$ $V_O = 0.3V$ to $2.7V$</td>
<td>100</td>
<td>114</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 10 , k\Omega$ $V_O = 0.2V$ to $2.9V$</td>
<td>100</td>
<td>124</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output Voltage Swing High</td>
<td>$R_L = 2 , k\Omega$ to $V^+/2$</td>
<td>40</td>
<td>80</td>
<td>120</td>
<td>mV from $V^+$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 10 , k\Omega$ to $V^+/2$</td>
<td>30</td>
<td>40</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Voltage Swing Low</td>
<td>$R_L = 2 , k\Omega$ to $V^+/2$</td>
<td>40</td>
<td>60</td>
<td>80</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 10 , k\Omega$ to $V^+/2$</td>
<td>20</td>
<td>40</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output Current $^{(6)}$$^{(7)}$</td>
<td>Sourcing $V_O = V^+/2$ $V_{IN} = 100 , mV$</td>
<td>25</td>
<td>42</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking $V_O = V^+/2$ $V_{IN} = -100 , mV$</td>
<td>25</td>
<td>42</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td></td>
<td>0.670</td>
<td>1.0</td>
<td>1.2</td>
<td>mA</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate $^{(8)}$</td>
<td>$A_V = +1$, $V_O = 2 , V_{PP}$ 10% to 90%</td>
<td>0.9</td>
<td></td>
<td></td>
<td>V/$\mu s$</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain Bandwidth</td>
<td></td>
<td>2.5</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>THD+N</td>
<td>Total Harmonic Distortion + Noise</td>
<td>$f = 1 , kHz$, $A_V = 1$, $R_L = 10 , k\Omega$</td>
<td>0.02</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$e_n$</td>
<td>Input Referred Voltage Noise Density</td>
<td>$f = 1 , kHz$</td>
<td>9</td>
<td></td>
<td></td>
<td>nV/$\sqrt{Hz}$</td>
</tr>
<tr>
<td>$I_n$</td>
<td>Input Referred Current Noise Density</td>
<td>$f = 100 , kHz$</td>
<td>1</td>
<td></td>
<td></td>
<td>fA/$\sqrt{Hz}$</td>
</tr>
</tbody>
</table>

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. Parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

(2) Limits are 100% production tested at $25^\circ C$. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested on shipped production material.

(4) This parameter is specified by design and/or characterization and is not tested in production.

(5) Positive current corresponds to current flowing into the device.

(6) The maximum power dissipation is a function of $T_{J(MAX)} - \theta_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

(7) The short circuit test is a momentary test.

(8) The number specified is the slower of positive and negative slew rates.
5V Electrical Characteristics

Unless otherwise specified, all limits are specified for \( T_A = 25^\circ C, V^+ = 5V, V^- = 0V, V_{CM} = V^+/2 \), and \( R_L > 10 \text{ k}\Omega \) to \( V^+/2 \). **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min (2)</th>
<th>Typ (3)</th>
<th>Max (2)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td>See (4)</td>
<td>±37</td>
<td>±200</td>
<td>±500</td>
<td>( \mu V )</td>
</tr>
<tr>
<td>( TCV_{OS} )</td>
<td>Input Offset Voltage Temperature Drift</td>
<td></td>
<td>±1</td>
<td>±5</td>
<td>( \mu V/^\circ C )</td>
<td></td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td>( -40^\circ C \leq T_A \leq 85^\circ C )</td>
<td>±0.2</td>
<td>±1</td>
<td>±50</td>
<td>( \text{pA} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( -40^\circ C \leq T_A \leq 125^\circ C )</td>
<td>±0.2</td>
<td>±1</td>
<td>±400</td>
<td>( \text{pA} )</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Input Offset Current</td>
<td></td>
<td>40</td>
<td>10</td>
<td>( fA )</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>( 0V \leq V_{CM} \leq 5V )</td>
<td>88</td>
<td>130</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>( 2.7V \leq V^+ \leq 12V, V_O = V^+/2 )</td>
<td>86</td>
<td>100</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>CMVR</td>
<td>Common Mode Voltage Range</td>
<td>CMRR ≥ 80 dB</td>
<td>–0.2</td>
<td>5.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CMRR ≥ 70 dB</td>
<td>–0.2</td>
<td>5.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( A_{VOL} )</td>
<td>Open Loop Voltage Gain</td>
<td>( R_L = 2 \text{ k}\Omega )</td>
<td>100</td>
<td>119</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_O = 0.3V \text{ to } 4.7V )</td>
<td>96</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 10 \text{ k}\Omega )</td>
<td>100</td>
<td>130</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_O = 0.2V \text{ to } 4.8V )</td>
<td>96</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Output Voltage Swing High</td>
<td>( R_L = 2 \text{ k}\Omega ) to ( V^+/2 )</td>
<td>60</td>
<td>110</td>
<td>130</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 10 \text{ k}\Omega ) to ( V^+/2 )</td>
<td>40</td>
<td>50</td>
<td>70</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output Voltage Swing Low</td>
<td>50</td>
<td>80</td>
<td>90</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 2 \text{ k}\Omega ) to ( V^+/2 )</td>
<td>30</td>
<td>40</td>
<td>50</td>
<td>mV</td>
</tr>
<tr>
<td>( I_{OUT} )</td>
<td>Output Current (6)(7)</td>
<td>Sourcing ( V_O = V^+/2 )</td>
<td>40</td>
<td>66</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_N = 100 \text{ mV} )</td>
<td>28</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking ( V_O = V^+/2 )</td>
<td>40</td>
<td>76</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_N = -100 \text{ mV} )</td>
<td>28</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td></td>
<td>0.715</td>
<td>1.0</td>
<td>1.2</td>
<td>mA</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate (8)</td>
<td>( A_V = +1, V_O = 4 \text{ V}_{PP} )</td>
<td>1.0</td>
<td></td>
<td></td>
<td>V/\mu s</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain Bandwidth</td>
<td></td>
<td>2.5</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>THD+N</td>
<td>Total Harmonic Distortion + Noise</td>
<td>( f = 1 \text{ kHz}, A_V = 1 )</td>
<td>0.02</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>( e_n )</td>
<td>Input Refereed Voltage Noise Density</td>
<td>( f = 1 \text{ kHz} )</td>
<td>9</td>
<td></td>
<td></td>
<td>nV/\sqrt{Hz}</td>
</tr>
<tr>
<td>( I_n )</td>
<td>Input Referred Current Noise Density</td>
<td>( f = 100 \text{ kHz} )</td>
<td>1</td>
<td></td>
<td></td>
<td>fA/\sqrt{Hz}</td>
</tr>
</tbody>
</table>

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(7) The short circuit test is a momentary test.

(8) The number specified is the slower of positive and negative slew rates.
±5V Electrical Characteristics (1)

Unless otherwise specified, all limits are specified for $T_A = 25^\circ C$, $V^+ = 5V$, $V^- = -5V$, $V_{CM} = 0V$, and $R_L > 10 \, k\Omega$ to 0V.

**Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min (2)</th>
<th>Typ (3)</th>
<th>Max (2)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td></td>
<td>$\pm 37$</td>
<td>$\pm 200$</td>
<td>$\pm 500$</td>
<td>$\mu V$</td>
</tr>
<tr>
<td>$TCV_{OS}$</td>
<td>Input Offset Voltage Temperature Drift</td>
<td>$-40^\circ C \leq T_A \leq 85^\circ C$</td>
<td>$\pm 0.2$</td>
<td>$1$</td>
<td>$\pm 50$</td>
<td>$\mu V/\circ C$</td>
</tr>
<tr>
<td>$TCV_{OS}$</td>
<td>Input Offset Voltage Temperature Drift</td>
<td>$-40^\circ C \leq T_A \leq 125^\circ C$</td>
<td>$\pm 0.2$</td>
<td>$1$</td>
<td>$\pm 400$</td>
<td>$\mu V/\circ C$</td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input Bias Current</td>
<td></td>
<td>$\pm 0.2$</td>
<td>$1 \mu A$</td>
<td>$-40 \leq T_A \leq 125^\circ C$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current</td>
<td>See (4)</td>
<td>$40$</td>
<td>$92$</td>
<td>$138$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$CMRR$</td>
<td>Common Mode Rejection Ratio</td>
<td>$-5V \leq V_{CM} \leq 5V$</td>
<td>$92$</td>
<td>$88$</td>
<td>$138$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$PSRR$</td>
<td>Power Supply Rejection Ratio</td>
<td>$2.7V \leq V^+ \leq 12V$, $V_O = 0V$</td>
<td>$86$</td>
<td>$98$</td>
<td>$98$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$CMVR$</td>
<td>Common Mode Voltage Range</td>
<td>$CMRR \geq 80 , dB$, $CMRR \geq 70 , dB$</td>
<td>$-5.2$</td>
<td>$5.2$</td>
<td>$5.2$</td>
<td>$V$</td>
</tr>
<tr>
<td>$A_{VOL}$</td>
<td>Open Loop Voltage Gain</td>
<td>$R_L = 2 , k\Omega$, $V_O = -4.7V$ to $4.7V$</td>
<td>$100$</td>
<td>$100$</td>
<td>$121$</td>
<td>$dB$</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output Voltage Swing High</td>
<td>$R_L = 2 , k\Omega$ to $0V$</td>
<td>$90$</td>
<td>$150$</td>
<td>$170$</td>
<td>$mV$ from $V^+$</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output Voltage Swing Low</td>
<td>$R_L = 10 , k\Omega$ to $0V$</td>
<td>$40$</td>
<td>$80$</td>
<td>$100$</td>
<td>$mV$ from $V^-$</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output Current (6)(7)</td>
<td>Sourcing $V_O = 0V$, $V_{IN} = 100 , mV$</td>
<td>$50$</td>
<td>$86$</td>
<td>$86$</td>
<td>$mA$</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output Current (6)(7)</td>
<td>Sinking $V_O = 0V$, $V_{IN} = -100 , mV$</td>
<td>$50$</td>
<td>$35$</td>
<td>$84$</td>
<td>$mA$</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td></td>
<td>$0.790$</td>
<td>$1.1$</td>
<td>$1.3$</td>
<td>$mA$</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate (8)</td>
<td>$A_V = +1, V_O = 9 , V_{PP}$, 10% to 90%</td>
<td>$1.1$</td>
<td>$1$</td>
<td></td>
<td>$V/\mu S$</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain Bandwidth</td>
<td></td>
<td>$2.5$</td>
<td>$1.1$</td>
<td></td>
<td>$MHz$</td>
</tr>
<tr>
<td>THD+N</td>
<td>Total Harmonic Distortion + Noise</td>
<td>$f = 1 , kHz$, $A_V = 1$, $R_L = 10 , k\Omega$</td>
<td>$0.02$</td>
<td>$2.5$</td>
<td></td>
<td>$%$</td>
</tr>
<tr>
<td>$e_n$</td>
<td>Input Referred Voltage Noise Density</td>
<td>$f = 1 , kHz$</td>
<td>$9$</td>
<td></td>
<td></td>
<td>$nV/\sqrt{Hz}$</td>
</tr>
<tr>
<td>$i_n$</td>
<td>Input Referred Current Noise Density</td>
<td>$f = 100 , kHz$</td>
<td>$1$</td>
<td></td>
<td></td>
<td>$fA/\sqrt{Hz}$</td>
</tr>
</tbody>
</table>

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. Parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

(2) Limits are 100% production tested at $25^\circ C$. Limits over the operating temperature range are specified through correlations using the Statistical Quality Control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested on shipped production material.

(4) This parameter is specified by design and/or characterization and is not tested in production.

(5) Positive current corresponds to current flowing into the device.

(6) The maximum power dissipation is a function of $T_J(MAX) - \theta_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(MAX) - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

(7) The short circuit test is a momentary test.

(8) The number specified is the slower of positive and negative slew rates.
Connection Diagram

Figure 2. 5-Pin SOT-23 - Top View
See DBV Package
Typical Performance Characteristics

Unless otherwise noted: $T_A = 25^\circ C$, $V_{CM} = V_S/2$, $R_L > 10 \, \Omega$.

Offset Voltage Distribution

TCVOS Distribution

Offset Voltage Distribution

TCVOS Distribution

Offset Voltage Distribution

TCVOS Distribution

Offset Voltage Distribution

TCVOS Distribution
Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{\text{CM}} = V_S/2$, $R_L > 10\ \Omega$.

**Offset Voltage vs. Temperature**

![Offset Voltage vs. Temperature graph](image)

**CMRR vs. Frequency**

![CMRR vs. Frequency graph](image)

**Offset Voltage vs. Supply Voltage**

![Offset Voltage vs. Supply Voltage graph](image)

**Offset Voltage vs. $V_{\text{CM}}$**

![Offset Voltage vs. $V_{\text{CM}}$ graph](image)
Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25 \degree C$, $V_{CM} = V_S/2$, $R_L > 10 \, k\Omega$.

**Input Bias Current vs. $V_{CM}$**

- **Figure 15.**
- **Figure 16.**
- **Figure 17.**
- **Figure 18.**
- **Figure 19.**
- **Figure 20.**
Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25^\circ C$, $V_{CM} = V_S/2$, $R_L > 10 \, k\Omega$.

**PSRR vs. Frequency**

**Supply Current vs. Supply Voltage (Per Channel)**

**Sinking Current vs. Supply Voltage**

**Sourcing Current vs. Supply Voltage**

**Output Voltage vs. Output Current**

**Slew Rate vs. Supply Voltage**

Figure 21.

Figure 22.

Figure 23.

Figure 24.

Figure 25.

Figure 26.
Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25^\circ C$, $V_{CM} = V_S/2$, $R_L > 10 \, k\Omega$.

Open Loop Frequency Response

![Graph showing Open Loop Frequency Response](image)

**Figure 27.**

Large Signal Step Response

![Graph showing Large Signal Step Response](image)

**Figure 29.**

Small Signal Step Response

![Graph showing Small Signal Step Response](image)

**Figure 30.**

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Product Folder Links: SM72501
Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25^\circ C$, $V_{CM} = V_S/2$, $R_L > 10 \, k\Omega$.

Input Voltage Noise vs. Frequency

Open Loop Gain vs. Output Voltage Swing

Output Swing High vs. Supply Voltage

Output Swing Low vs. Supply Voltage

Input Voltage Noise

Output Swing High

Output Swing Low

Output Swing High

Output Swing Low

Figure 33.

Figure 34.

Figure 35.

Figure 36.

Figure 37.

Figure 38.
Typical Performance Characteristics (continued)

Unless otherwise noted: $T_A = 25^\circ C$, $V_{CM} = V_S/2$, $R_L > 10 \, k\Omega$.

**THD+N vs. Frequency**

**Figure 39.**

**THD+N vs. Output Voltage**

**Figure 40.**
APPLICATION INFORMATION

SM72501

The SM72501 is a low offset voltage, rail-to-rail input and output precision amplifier with a CMOS input stage and wide supply voltage range of 2.7V to 12V. The SM72501 has a very low input bias current of only ±200 fA at room temperature.

The wide supply voltage range of 2.7V to 12V over the extensive temperature range of −40°C to 125°C makes the SM72501 an excellent choice for low voltage precision applications with extensive temperature requirements.

The SM72501 has only ±37 μV of typical input referred offset voltage and this offset is specified to be less than ±500 μV over temperature. This minimal offset voltage allows more accurate signal detection and amplification in precision applications.

The low input bias current of only ±200 fA along with the low input referred voltage noise of 9 nV/√Hz gives the SM72501 superiority for use in sensor applications. Lower levels of noise from the SM72501 means better signal fidelity and a higher signal-to-noise ratio.

Technical support and extensive characterization data is available for sensitive applications or applications with a constrained error budget.

The SM72501 is offered in the space saving 5-Pin SOT-23. This small package is an ideal solution for area constrained PC boards and portable electronics.

CAPACITIVE LOAD

The SM72501 can be connected as a non-inverting unity gain follower. This configuration is the most sensitive to capacitive loading.

The combination of a capacitive load placed on the output of an amplifier along with the amplifier's output impedance creates a phase lag which in turn reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be either underdamped or it will oscillate.

In order to drive heavier capacitive loads, an isolation resistor, \( R_{ISO} \), in Figure 41 should be used. By using this isolation resistor, the capacitive load is isolated from the amplifier's output, and hence, the pole caused by \( C_L \) is no longer in the feedback loop. The larger the value of \( R_{ISO} \), the more stable the output voltage will be. If values of \( R_{ISO} \) are sufficiently large, the feedback loop will be stable, independent of the value of \( C_L \). However, larger values of \( R_{ISO} \) result in reduced output swing and reduced output current drive.

![Figure 41. Isolating Capacitive Load](image)

INPUT CAPACITANCE

CMOS input stages inherently have low input bias current and higher input referred voltage noise. The SM72501 enhances this performance by having the low input bias current of only ±200 fA, as well as, a very low input referred voltage noise of 9 nV/√Hz. In order to achieve this a larger input stage has been used. This larger input stage increases the input capacitance of the SM72501. The typical value of this input capacitance, \( C_{IN} \), for the SM72501 is 25 pF. The input capacitance will interact with other impedances such as gain and feedback resistors, which are seen on the inputs of the amplifier, to form a pole. This pole will have little or no effect on the output of the amplifier at low frequencies and DC conditions, but will play a bigger role as the frequency increases. At higher frequencies, the presence of this pole will decrease phase margin and will also cause gain peaking. In order to compensate for the input capacitance, care must be taken in choosing the feedback resistors. In addition to being selective in picking values for the feedback resistor, a capacitor can be added to the feedback path to increase stability.

The DC gain of the circuit shown in Figure 42 is simply \(-R_2/R_1\).
For the time being, ignore $C_F$. The AC gain of the circuit in Figure 42 can be calculated as follows:

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{1 + \frac{s}{A_0 \frac{R_1}{R_1 + R_2}} + \frac{s^2}{A_0 \frac{C_{IN} R_2}{R_2}}}$$

(1)

This equation is rearranged to find the location of the two poles:

$$p_{1,2} = \frac{-1}{2C_{IN}} \left[ \frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left( \frac{1}{R_1} + \frac{1}{R_2} \right)^2 - \frac{4 A_0 C_{IN}}{R_2}} \right]$$

(2)

As shown in Equation 2, as values of $R_1$ and $R_2$ are increased, the magnitude of the poles is reduced, which in turn decreases the bandwidth of the amplifier. Whenever possible, it is best to choose smaller feedback resistors. Figure 43 shows the effect of the feedback resistor on the bandwidth of the SM72501.

Equation 2 has two poles. In most cases, it is the presence of pairs of poles that causes gain peaking. In order to eliminate this effect, the poles should be placed in Butterworth position, since poles in Butterworth position do not cause gain peaking. To achieve a Butterworth pair, the quantity under the square root in Equation 2 should be set to equal $-1$. Using this fact and the relation between $R_1$ and $R_2$, $R_2 = -A_V R_1$, the optimum value for $R_1$ can be found. This is shown in Equation 3. If $R_1$ is chosen to be larger than this optimum value, gain peaking will occur.

$$R_1 < \frac{(1 \cdot A_V)^2}{2A_0 A_V C_{IN}}$$

(3)

In Figure 42, $C_F$ is added to compensate for input capacitance and to increase stability. Additionally, $C_F$ reduces or eliminates the gain peaking that can be caused by having a larger feedback resistor. Figure 44 shows how $C_F$ reduces gain peaking.
**DIODES BETWEEN THE INPUTS**

The SM72501 has a set of anti-parallel diodes between the input pins, as shown in Figure 45. These diodes are present to protect the input stage of the amplifier. At the same time, they limit the amount of differential input voltage that is allowed on the input pins. A differential signal larger than one diode voltage drop might damage the diodes. The differential signal between the inputs needs to be limited to ±300 mV or the input current needs to be limited to ±10 mA.

**PRECISION CURRENT SOURCE**

The SM72501 can be used as a precision current source in many different applications. Figure 46 shows a typical precision current source. This circuit implements a precision voltage controlled current source. Amplifier A1 is a differential amplifier that uses the voltage drop across \( R_S \) as the feedback signal. Amplifier A2 is a buffer that eliminates the error current from the load side of the \( R_S \) resistor that would flow in the feedback resistor if it were connected to the load side of the \( R_S \) resistor. In general, the circuit is stable as long as the closed loop bandwidth of amplifier A2 is greater than the closed loop bandwidth of amplifier A1. Note that if A1 and A2 are the same type of amplifiers, then the feedback around A1 will reduce its bandwidth compared to A2.
The equation for output current can be derived as follows:

\[
\frac{V_2 R}{R + R} + \frac{(V_0 - IR_0) R}{R + R} = \frac{V_1 R}{R + R} + \frac{V_0 R}{R + R}
\]  

(4)

Solving for the current \( I \) results in the following equation:

\[
I = \frac{V_2 - V_1}{R_S}
\]

(5)

LOW INPUT VOLTAGE NOISE

The SM72501 has a very low input voltage noise of 9 nV/\( \sqrt{\text{Hz}} \). This input voltage noise can be further reduced by placing \( N \) amplifiers in parallel as shown in Figure 47. The total voltage noise on the output of this circuit is divided by the square root of the number of amplifiers used in this parallel combination. This is because each individual amplifier acts as an independent noise source, and the average noise of independent sources is the quadrature sum of the independent sources divided by the number of sources. For \( N \) identical amplifiers, this means:

\[
\text{REDUCED INPUT VOLTAGE NOISE} = \frac{1}{N} \sqrt{\frac{\varepsilon_{n1}^2 + \varepsilon_{n2}^2 + \cdots + \varepsilon_{nN}^2}{N}}
\]

\[
= \frac{1}{\sqrt{N}} \sqrt{N \varepsilon_n^2} = \sqrt{\frac{N}{N}} \varepsilon_n
\]

\[
= \frac{1}{\sqrt{N}} \varepsilon_n
\]

(6)

Figure 47 shows a schematic of this input voltage noise reduction circuit. Typical resistor values are:

\( R_G = 10 \Omega, \ R_F = 1 \, \text{k}\Omega, \ \text{and} \ R_O = 1 \, \text{k}\Omega. \)
TOTAL NOISE CONTRIBUTION

The SM72501 has very low input bias current, very low input current noise, and very low input voltage noise. As a result, these amplifiers are ideal choices for circuits with high impedance sensor applications.

Figure 48 shows the typical input noise of the SM72501 as a function of source resistance where:

- $e_n$ denotes the input referred voltage noise
- $e_i$ is the voltage drop across source resistance due to input referred current noise or $e_i = R_S \cdot i_n$
- $e_t$ shows the thermal noise of the source resistance
- $e_{ni}$ shows the total noise on the input.

Where:

$$e_{ni} = \sqrt{e_n^2 + e_i^2 + e_t^2}$$  \hspace{1cm} (7)

The input current noise of the SM72501 is so low that it will not become the dominant factor in the total noise unless source resistance exceeds 300 MΩ, which is an unrealistically high value.

As is evident in Figure 48, at lower $R_S$ values, total noise is dominated by the amplifier's input voltage noise. Once $R_S$ is larger than a few kilo-Ohms, then the dominant noise factor becomes the thermal noise of $R_S$. As mentioned before, the current noise will not be the dominant noise factor for any practical application.
HIGH IMPEDANCE SENSOR INTERFACE

Many sensors have high source impedances that may range up to 10 MΩ. The output signal of sensors often needs to be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor’s output and cause a voltage drop across the source resistance as shown in Figure 49, where $V_{IN}^+ = V_S - I_{BIAS}R_S$.

The last term, $I_{BIAS}R_S$, shows the voltage drop across $R_S$. To prevent errors introduced to the system due to this voltage, an op amp with very low input bias current must be used with high impedance sensors. This is to keep the error contribution by $I_{BIAS}R_S$ less than the input voltage noise of the amplifier, so that it will not become the dominant noise factor.

pH electrodes are very high impedance sensors. As their name indicates, they are used to measure the pH of a solution. They usually do this by generating an output voltage which is proportional to the pH of the solution. pH electrodes are calibrated so that they have zero output for a neutral solution, pH = 7, and positive and negative voltages for acidic or alkaline solutions. This means that the output of a pH electrode is bipolar and has to be level shifted to be used in a single supply system. The rate of change of this voltage is usually shown in mV/pH and is different for different pH sensors. Temperature is also an important factor in a pH electrode reading. The output voltage of the sensor will change with temperature.

Figure 50 shows a typical output voltage spectrum of a pH electrode. Note that the exact values of output voltage will be different for different sensors. In this example, the pH electrode has an output voltage of 59.15 mV/pH at 25°C.

The temperature dependence of a typical pH electrode is shown in Figure 51. As is evident, the output voltage changes with changes in temperature.
The schematic shown in Figure 52 is a typical circuit which can be used for pH measurement. The LM35 is a precision integrated circuit temperature sensor. This sensor is differentiated from similar products because it has an output voltage linearly proportional to Celsius measurement, without the need to convert the temperature to Kelvin. The LM35 is used to measure the temperature of the solution and feeds this reading to the Analog to Digital Converter, ADC. This information is used by the ADC to calculate the temperature effects on the pH readings. The LM35 needs to have a resistor, R_T in Figure 52, to –V^+ in order to be able to read temperatures below 0°C. R_T is not needed if temperatures are not expected to go below zero.

The output of pH electrodes is usually large enough that it does not require much amplification; however, due to the very high impedance, the output of a pH electrode needs to be buffered before it can go to an ADC. Since most ADCs are operated on single supply, the output of the pH electrode also needs to be level shifted. Amplifier A1 buffers the output of the pH electrode with a moderate gain of +2, while A2 provides the level shifting. V_{OUT} at the output of A2 is given by: V_{OUT} = -2V_{pH} + 1.024V.

The LM4140A is a precision, low noise, voltage reference used to provide the level shift needed. The ADC used in this application is the ADC12032 which is a 12-bit, 2 channel converter with multiplexers on the inputs and a serial output. The 12-bit ADC enables users to measure pH with an accuracy of 0.003 of a pH unit. Adequate power supply bypassing and grounding is extremely important for ADCs. Recommended bypass capacitors are shown in Figure 52. It is common to share power supplies between different components in a circuit. To minimize the effects of power supply ripples caused by other components, the op amps need to have bypass capacitors on the supply pins. Using the same value capacitors as those used with the ADC are ideal. The combination of these three values of capacitors ensures that AC noise present on the power supply line is grounded and does not interfere with the amplifiers’ signal.
Figure 52. pH Measurement Circuit
## REVISION HISTORY

**Changes from Revision B (April 2013) to Revision C**

<table>
<thead>
<tr>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
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### PACKAGING INFORMATION

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<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
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<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>S501</td>
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<td>-40 to 125</td>
<td>S501</td>
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</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

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<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
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<td>A0</td>
<td>Dimension designed to accommodate the component width</td>
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<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
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<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
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<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
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#### REEL DIMENSIONS

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal*

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<td>8.4</td>
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**TAPE AND REEL BOX DIMENSIONS**

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<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
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*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.
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