# DS99R124Q 5 - 43 MHz 18-bit Color FPD-Link II to FPD-Link Converter

**Check for Samples: DS99R124Q**

## FEATURES

- **5 – 43 MHz Support (140 Mbps to 1.2 Gbps Serial Link)**
- **4-Channel (3 data + 1 Clock) FPD-Link LVDS Outputs**
- **3 Low-Speed Over-Sampled LVCMOS Outputs**
- **AC Coupled STP Interconnect up to 10 Meters in Length**
- **Integrated Input Termination**
- **@ Speed Link BIST Mode and Reporting Pin**
- **Optional I2C Compatible Serial Control Bus**
- **RGB666 + VS, HS, DE Converted from 1 Pair**
- **Power Down Mode Minimizes Power Dissipation**
- **FAST Random Data Lock; no Reference Clock Required**
- **Adjustable Input Receive Equalization**
- **LOCK (Real Time Link Status) Reporting Pin**
- **Low EMI FPD-Link Output**
- **SSCG Option for Lower EMI**
- **1.8V or 3.3V Compatible I/O Interface**
- **Automotive Grade Product: AEC-Q100 Grade 2 Qualified**
- **>8 kV HBM and ISO 10605 ESD Rating**

## APPLICATIONS

- **Automotive Display for Navigation**
- **Automotive Display for Entertainment**

## DESCRIPTION

The DS99R124Q converts FPD-Link II to FPD-Link. It translates a high-speed serialized interface with an embedded clock over a single pair (FPD-Link II) to three LVDS data/control streams and one LVDS clock pair (FPD-Link). This serial bus scheme greatly eases system design by eliminating skew problems between clock and data, reduces the number of connector pins, reduces the interconnect size, weight, and cost, and overall eases PCB layout. In addition, internal DC balanced decoding is used to support AC-coupled interconnects.

The DS99R124Q converter recovers the data (RGB) and control signals and extracts the clock from a serial stream (FPD-Link II). It is able to lock to the incoming data stream without the use of a training sequence or special SYNC patterns and does not require a reference clock. A link status (LOCK) output signal is provided.

Adjustable input equalization of the serial input stream provides compensation for transmission medium losses of the cable and reduces the medium-induced deterministic jitter. EMI is minimized by the use of low voltage differential signaling, output state select feature, and additional output spread spectrum generation.

With fewer wires to the physical interface of the display, FPD-Link output with LVDS technology is ideal for high speed, low power and low EMI data transfer.

The DS99R124Q is offered in a 48-pin WQFN package and is specified over the automotive AEC-Q100 Grade 2 temperature range of -40˚C to +105˚C.

## Applications Diagram

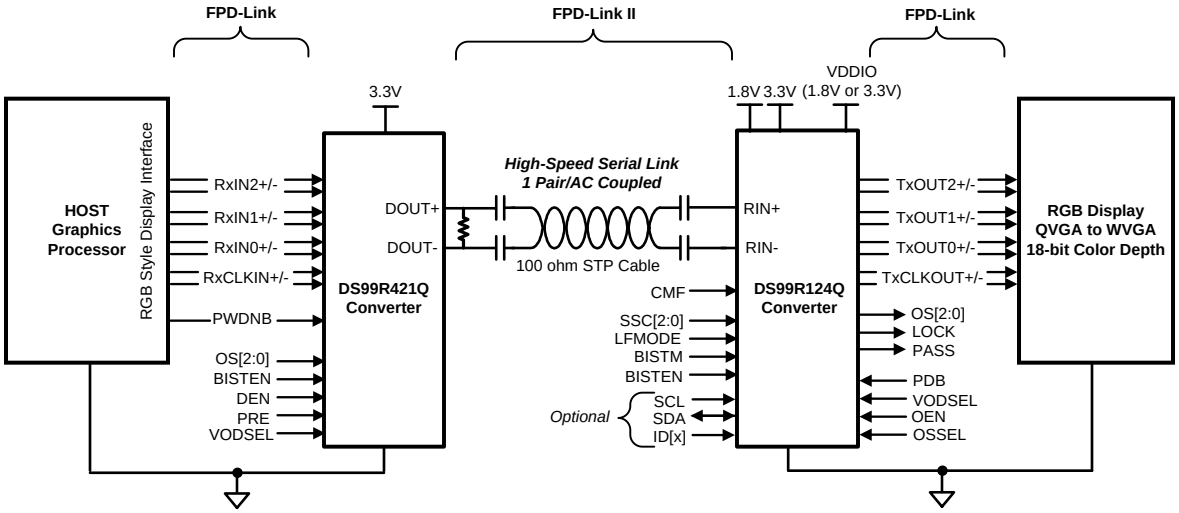



**Figure 1.**

## DS99R124Q Pin Diagram

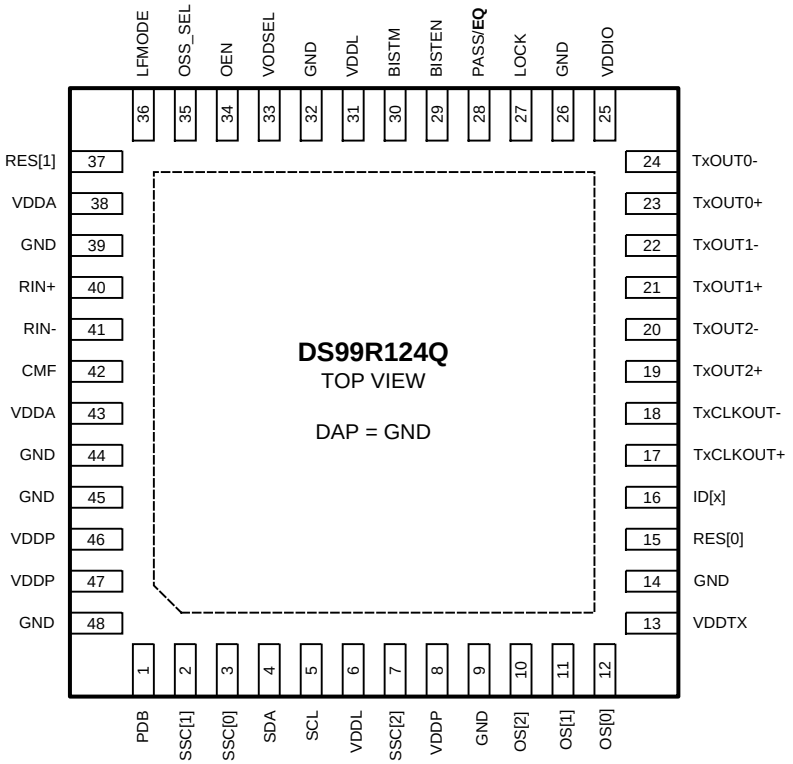



**Figure 2. FPD-Link II to FPD-Link Convertor - DS99R124Q**
**48 Pin WQFN Package**
**See Package Number RHS0048A**

## PIN DESCRIPTIONS

| Pin Name | Pin # | I/O, Type | Description |
|---|---|---|---|
| **FPD-Link II Input Interface** | | | |
| RIN+ | 40 | I, LVDS | True input<br>The input must be AC coupled with a 100 nF capacitor. Internal termination. |
| RIN- | 41 | I, LVDS | Inverting input<br>The input must be AC coupled with a 100 nF capacitor. Internal termination. |
| CMF | 42 | I, Analog | Common-Mode Filter<br>VCM center-tap is a virtual ground which maybe ac-coupled to ground to increase receiver common mode noise immunity. Recommended value is 4.7 µF or higher. |
| **FPD-Link Output Interface** | | | |
| TxOUT[2:0]+ | 19, 21, 23 | O, LVDS | True LVDS Data Output<br>This pair should have a 100 Ω termination for standard LVDS levels. |
| TxOUT[2:0]- | 20, 22, 24 | O, LVDS | Inverting LVDS Data Output<br>This pair should have a 100 Ω termination for standard LVDS levels. |
| TxCLKOUT+ | 17 | O, LVDS | True LVDS Clock Output<br>This pair should have a 100 Ω termination for standard LVDS levels. |
| TxCLKOUT- | 18 | O, LVDS | Inverting LVDS Clock Output<br>This pair should have a 100 Ω termination for standard LVDS levels. |
| **LVCMOS Outputs** | | | |
| OS[2:0] | 10, 11, 12 | O, LVMOS | Over-Sampled Low Frequency Outputs<br>These bits map to the DS99R421's OS[2:0] over-sampled low-frequency inputs. Signals must be slower the TxCLK/5. On the DS90UR241 these map to the DIN[23:21] inputs. OS0 = DIN21, OS1 = DIN22, OS2 = DIN23. |
| LOCK | 27 | O, LVMOS | LOCK Status Output<br>LOCK = 1, PLL is locked, outputs are active.<br>LOCK = 0, PLL is unlocked, output states determined by OSS_SEL.<br>Maybe used as a Link Status or to flag when the Video Data is active (ON/OFF). |
| **Control and Configuration** | | | |
| PDB | 1 | I, LVCMOS w/ pull-down | Power Down Mode Input<br>PDB = 1, Device is enabled (normal operation)<br>PDB = 0, Device is in power-down, the output are controlled by the settings. Control registers are **RESET**. |
| VODSEL | 33 | I, LVCMOS w/ pull-down | Differential Driver Output Voltage Select<br>VODSEL = 1, LVDS VOD is ±400 mV, 800 mVp-p (typ) — Long Cable / De-E Applications<br>VODSEL = 0, LVDS VOD is ±250 mV, 500 mVp-p (typ)<br>See Table 2 |
| OEN | 34 | I, LVCMOS w/ pull-down | Output Enable Input<br>OEN = 1, FPD-Link outputs are enabled (active).<br>OEN = 0, FPD-Link outputs are TRI-STATE. |
| OSS_SEL | 35 | I, LVCMOS w/ pull-down | Output Sleep State Select Input<br>See Table 1 |
| LFMODE | 36 | I, LVCMOS w/ pull-down | Low Frequency Mode — Pin or Register Control<br>LF_MODE = 1, low frequency mode (TxCLKOUT = 5-20 MHz)<br>LF_MODE = 0, high frequency mode (TxCLKOUT = 20-43 MHz) |
| SSC[2:0] | 7, 2, 3 | I, LVCMOS w/ pull-down | Spread Spectrum Clock Generation (SSCG) Range Select<br>See Table 3 and Table 4 |
| RES[1:0] | 37, 15 | I, LVCMOS w/ pull-down | ***Reserved***<br>Tie Low |
| **Control and Configuration — STRAP PIN**<br>For a High State, use a 10 kΩ pull up to VDDIO; for a Low State, the IO includes an internal pull down. The STRAP pin is read upon power-up and set device configuration. Pin number listed along with shared LVCMOS Output name in square bracket. | | | |
| EQ | 28 [PASS] | STRAP<br>I, LVCMOS w/ pull-down | EQ Gain Control of FPD-Link II Input<br>EQ = 1, EQ gain is enabled (~13 dB)<br>EQ = 0, EQ gain is disabled (~1.625 dB) |
| **Optional BIST Mode** | | | |
| BISTEN | 29 | I, LVCMOS w/ pull-down | BIST Enable Input – Optional<br>BISTEN = 1, BIST Mode is enabled.<br>BISTEN = 0, normal mode. |

## PIN DESCRIPTIONS (continued)

| Pin Name | Pin # | I/O, Type | Description |
|---|---|---|---|
| BISTM | 30 | I, LVCMOS w/ pull-down | BIST Mode Input – Optional<br>BISTM = 1, selects Payload Error Mode<br>BISTM = 0, selects Pass / Fail Result-Only Mode |
| PASS | 28 | O, LVCMOS | PASS Output (BIST Mode) – Optional<br>PASS = 1, no errors detected<br>PASS = 0, errors detected<br>Leave open if unused. Route to a test point (pad) recommended. |
| **Optional Serial Bus Control Interface** | | | |
| SCL | 5 | I, LVCMOS | Serial Control Bus Clock Input - Optional<br>SCL requires an external pull-up resistor to $V_{DDIO}$. |
| SDA | 4 | I/O, LVCMOS Open Drain | Serial Control Bus Data Input / Output - Optional<br>SDA requires an external pull-up resistor to $V_{DDIO}$. |
| ID[x] | 16 | I, Analog | Serial Control Bus Device ID Address Select — Optional<br>Resistor to Ground and 10 kΩ pull-up to 1.8V rail. See Table 5. |
| **Power and Ground** | | | |
| VDDL | 6, 31 | Power | Logic Power, 1.8 V ±5% |
| VDDA | 38, 43 | Power | Analog Power, 1.8 V ±5% |
| VDDP | 8, 46, 47 | Power | SSC Generator Power, 1.8 V ±5% |
| VDDTX | 13 | Power | FPD-Link Power, 3.3 V ±10% |
| VDDIO | 25 | Power | LVCMOS I/O Power, 1.8 V ±5% OR 3.3 V ±10% |
| GND | 9, 14, 26, 32, 39, 44, 45, 48 | Ground | Ground |
| DAP | DAP | Ground | DAP is the large metal contact at the bottom side, located at the center of the WQFN package. **Connected to the ground plane** (GND) with at least 9 vias. |

## Block Diagram

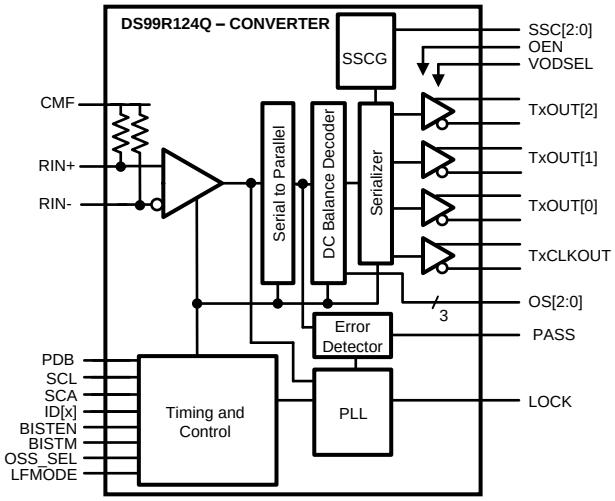



**Figure 3. FPD-Link II to FPD-Link Convertor**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings[1][2]

| | | |
|---|---|---|
| Supply Voltage – $V_{DDn}$ (1.8V) | | −0.3V to +2.5V |
| Supply Voltage – $V_{DDTX}$ (3.3V) | | −0.3V to +4.0V |
| Supply Voltage – $V_{DDIO}$ | | −0.3V to +4.0V |
| LVCMOS I/O Voltage | | −0.3V to +(VDDIO + 0.3V) |
| Receiver Input Voltage | | −0.3V to (VDD + 0.3V) |
| LVDS Output Voltage | | −0.3V to (VDDTX + 0.3V) |
| Junction Temperature | | +150°C |
| Storage Temperature | | −65°C to +150°C |
| Lead Temperature (Soldering, 4s) | | +260°C |
| 48L RHS Package | | |
| Maximum Power Dissipation Capacity at 25°C | Derate above 25°C | 1/ $\theta_{JA}$°C/W |
| | $\theta_{JA}$ | 27.7 °C/W |
| | $\theta_{JC}$ | 3.0 °C/W |
| ESD Rating (IEC, powered-up only), $R_D$ = 330Ω, $C_S$ = 150pF | Air Discharge ($R_{IN+}$, $R_{IN-}$) | ≥±30 kV |
| | Contact Discharge ($R_{IN+}$, $R_{IN-}$) | ≥±6 kV |
| ESD Rating (ISO10605), $R_D$ = 330Ω, $C_S$ = 150 & 330pF | Air Discharge ($R_{IN+}$, $R_{IN-}$) | ≥±15 kV |
| | Contact Discharge ($R_{IN+}$, $R_{IN-}$) | ≥±8 kV |
| ESD Rating (ISO10605), $R_D$ = 2kΩ, $C_S$ = 150 & 330pF | Air Discharge ($R_{IN+}$, $R_{IN-}$) | ≥±15 kV |
| | Contact Discharge ($R_{IN+}$, $R_{IN-}$) | ≥±8 kV |
| ESD Rating (HBM) | | ≥±8 kV |
| ESD Rating (CDM) | | ≥±1.25 kV |
| ESD Rating (MM) | | ≥±250 V |

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

## Recommended Operating Conditions

| | Min | Nom | Max | Units |
|---|---|---|---|---|
| Supply Voltage ($V_{DDn}$) | 1.71 | 1.8 | 1.89 | V |
| LVCMOS Supply Voltage ($V_{DDIO}$) | 1.71 | 1.8 | 1.89 | V |
| LVCMOS Supply Voltage ($V_{DDIO}$) | 3.0 | 3.3 | 3.6 | V |
| Operating Free Air Temperature ($T_A$) | −40 | +25 | +105 | °C |
| TxCLK Clock Frequency | 5 | | 43 | MHz |
| Supply Noise[1] | | | 100 | $mV_{P-P}$ |

(1) Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the $V_{DDn}$ (1.8V) supply with amplitude = 100 mVp-p measured at the device $V_{DDn}$ pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 750 kHz. The Des on the other hand shows no error when the noise frequency is less than 400 kHz.

## DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1)(2)(3)

| Symbol | Parameter | Conditions | | Pin/Freq. | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| **FPD-Link LVDS Output** | | | | | | | | |
| $\|V_{OD}\|$ | Differential Output Voltage | $R_L$ = 100Ω | VODSEL = L | TxCLKOUT+, TxCLKOUT-, TxOUT[2:0]+, TxOUT[2:0]- | 100 | 250 | 400 | mV |
| | | | VODSEL = H | | 200 | 400 | 600 | mV |
| $V_{ODp-p}$ | Differential Output Voltage A-B | | VODSEL = L | | | 500 | | mVp-p |
| | | | VODSEL = H | | | 800 | | mVp-p |
| $\Delta V_{OD}$ | Output Voltage Unbalance | | | | | 1 | 50 | mV |
| $V_{OS}$ | Offset Voltage | | VODSEL = L | | 1.0 | 1.2 | 1.5 | V |
| | | | VODSEL = H | | | 1.2 | | V |
| $\Delta V_{OS}$ | Offset Voltage Unbalance | | | | | 1 | 50 | mV |
| $I_{OS}$ | Output Short Circuit Current | Vout = GND | | | | -5 | | mA |
| $I_{OZ}$ | Output TRI-STATE Current | OEN = GND, Vout = $V_{DDTX}$, or GND | | | -10 | | +10 | µA |
| **3.3 V I/O LVCMOS DC SPECIFICATIONS – $V_{DDIO}$ = 3.0 to 3.6V** | | | | | | | | |
| $V_{IH}$ | High Level Input Voltage | | | PDB, VODSEL, OEN, OSS_SEL, LFMODE, SSC[2:0], BISTEN, BISTM | 2.2 | | $V_{DDIO}$ | V |
| $V_{IL}$ | Low Level Input Voltage | | | | GND | | 0.8 | V |
| $I_{IN}$ | Input Current | $V_{IN}$ = 0V or $V_{DDIO}$ | | | −15 | ±1 | +15 | µA |
| $V_{OH}$ | High Level Output Voltage | $I_{OH}$ = −0.5 mA | | LOCK, PASS, OS[2:0] | $V_{DDIO}$- 0.2 | $V_{DDIO}$ | | V |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL}$ = +0.5 mA | | | | GND | 0.2 | V |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT}$ = 0V | | | | -10 | | mA |
| $I_{OZ}$ | TRI-STATE Output Current | PDB = 0V, OSS_SEL = 0V, $V_{OUT}$ = 0V or $V_{DDIO}$ | | | −10 | | +10 | µA |
| **1.8 V I/O LVCMOS DC SPECIFICATIONS – $V_{DDIO}$ = 1.71 to 1.89V** | | | | | | | | |
| $V_{IH}$ | High Level Input Voltage | | | PDB, VODSEL, OEN, OSS_SEL, LFMODE, SSC[2:0], BISTEN, BISTM | 0.7 $V_{DDIO}$ | | $V_{DDIO}$ | V |
| $V_{IL}$ | Low Level Input Voltage | | | | GND | | 0.35* $V_{DDIO}$ | V |
| $I_{IN}$ | Input Current | $V_{IN}$ = 0V or $V_{DDIO}$ | | | −10 | ±1 | +10 | µA |

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

(2) Typical values represent most likely parametric norms at $V_{DDn}$ = 1.8V, $V_{DDTX}$ = 3.3V, $V_{DDIO}$ = 1.8V or 3.3V, Ta = +25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

## DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)

| Symbol | Parameter | Conditions | | Pin/Freq. | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High Level Output Voltage | $I_{OH}$ = −0.1 mA | | LOCK, PASS, OS[2:0] | $V_{DDIO}$ - 0.2 | $V_{DDIO}$ | | V |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL}$ = +0.1 mA | | | GND | | 0.2 | V |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT}$ = 0V | | | | -3 | | mA |
| $I_{OZ}$ | TRI-STATE Output Current | $V_{OUT}$ = 0V or $V_{DDIO}$ | | | -15 | | +15 | µA |
| **FPD-Link II LVDS RECEIVER DC SPECIFICATIONS** | | | | | | | | |
| $V_{TH}$ | Differential Input Threshold High Voltage | $V_{CM}$ = +1.2V (Internal $V_{BIAS}$) | | RIN+, RIN- | | | +50 | mV |
| $V_{TL}$ | Differential Input Threshold Low Voltage | | | | −50 | | | mV |
| $V_{CM}$ | Common Mode Voltage, Internal $V_{BIAS}$ | | | | | 1.2 | | V |
| $R_T$ | Input Termination | | | | 75 | 80 | 92 | Ω |
| **SUPPLY CURRENT** | | | | | | | | |
| $I_{DD1}$ | Supply Current (includes load current) 43 MHz Clock | Checker Board Pattern, VODSEL = H, SSCG = On Figure 4 | $V_{DDn}$= 1.89V | All $V_{DD(1.8)}$ pins | | 70 | 80 | mA |
| $I_{DDTX1}$ | | | $V_{DDTX}$ = 3.6V | $V_{DDTX}$ | | 30 | 40 | mA |
| $I_{DDIO1}$ | | | $V_{DDIO}$=1.89V | $V_{DDIO}$ | | 0.35 | 1 | mA |
| | | | $V_{DDIO}$ = 3.6V | | | 1 | 1.5 | mA |
| $I_{DDZ}$ | Supply Current Power Down | PDB = 0V, All other LVCMOS Inputs = 0V | $V_{DD}$= 1.89V | All $V_{DD(1.8)}$ pins | | 0.15 | 4 | mA |
| $I_{DDTXZ}$ | | | $V_{DDTX}$ = 3.6V | $V_{DDTX}$ | | 0.01 | 0.05 | mA |
| $I_{DDIOZ}$ | | | $V_{DDIO}$=1.89V | $V_{DDIO}$ | | 0.1 | 0.4 | mA |
| | | | $V_{DDIO}$ = 3.6V | | | 0.4 | 0.8 | mA |

## Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)

| Symbol | Parameter | Conditions | Pin/Freq. | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **FPD-Link II** | | | | | | | |
| $t_{DDLT}$ | Lock Time(3) | SSCG = Off | 5 MHz | | 6 | | ms |
| | | SSCG = On | 5 MHz | | 14 | | ms |
| | | SSCG = Off | 43 MHz | | 5 | | ms |
| | | SSCG = On | 43 MHz | | 8 | | ms |
| $t_{DJIT}$ | Input Jitter Tolerance | EQ = Off Jitter Frequency > 10 MHz Figure 14 | | | >0.45 | | UI |
| **FPD-Link Output** | | | | | | | |

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at $V_{DDn}$ = 1.8V, $V_{DDTX}$ = 3.3V, $V_{DDIO}$ = 1.8V or 3.3V, Ta = +25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(3) $t_{DDLT}$ is the time required by the deserializer to obtain lock when exiting power-down state with an active PCLK.

## Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)

| Symbol | Parameter | Conditions | Pin/Freq. | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{TLHT}$ | Low to High Transition Time | $R_L$ = 100Ω | TxCLKOUT±, TxOUT[2:0]± | | 0.3 | 0.6 | ns |
| $t_{THLT}$ | High to Low Transition Time | | | | 0.3 | 0.6 | ns |
| $t_{DCCJ}$ | Cycle-to-Cycle Output Jitter(4)(5) | TxCLKOUT = 5 MHz | TxCLKOUT± | | 900 | 2100 | ps |
| | | TxCLKOUT = 43 MHz | | | 75 | 125 | ps |
| $t_{TTP1}$ | Transmitter Pulse Position for bit 1 | | TxOUT[2:0]± | | 0 | | UI |
| $t_{TTP0}$ | Transmitter Pulse Position for bit 0 | | | | 1 | | UI |
| $t_{TPP6}$ | Transmitter Pulse Position for bit 6 | | | | 2 | | UI |
| $t_{TTP5}$ | Transmitter Pulse Position for bit 5 | | | | 3 | | UI |
| $t_{TTP4}$ | Transmitter Pulse Position for bit 4 | | | | 4 | | UI |
| $t_{TTP3}$ | Transmitter Pulse Position for bit 3 | | | | 5 | | UI |
| $t_{TTP2}$ | Transmitter Pulse Position for bit 2 | | | | 6 | | UI |
| $t_{TPDD}$ | Power Down Delay active to OFF Figure 6 | TxCLKOUT = 43 MHz | | | 6 | 10 | ns |
| $t_{TXZR}$ | Enable Delay OFF to active Figure 7 | TxCLKOUT = 43 MHz | | | 40 | 55 | ns |
| **LVCMOS Outputs** | | | | | | | |
| $t_{CLH}$ | Low to High Transition Time | $C_L$ = 8 pF Figure 5 | LOCK, PASS, OS[2:0] | | 10 | 15 | ns |
| $t_{CHL}$ | High to Low Transition Time | | | | 10 | 15 | ns |
| $t_{PASS}$ | BIST PASS Valid Time, BISTEN = 1, Figure 12 | TxCLKOUT = 5 MHz | PASS | | 560 | 570 | ns |
| | | TxCLKOUT = 43 MHz | | | 70 | 75 | ns |
| **SSCG Mode** | | | | | | | |
| $f_{DEV}$ | Spread Spectrum Clocking Deviation Frequency | See(6) | TxCLKOUT = 5 to 43 MHz, SSC[3:0] = ON | ±0.5 | | ±2 | % |
| $f_{MOD}$ | Spread Spectrum Clocking Modulation Frequency | See(6) | TxCLKOUT = 5 to 43 MHz, SSC[3:0] = ON | 8 | | 100 | kHz |

(4) $t_{DCCJ}$ is the maximum amount of jitter between adjacent clock cycles.
(5) Specification is ensured by characterization and is not tested in production.
(6) Specification is ensured by design and is not tested in production.

## Recommended Timing for the Serial Control Bus

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL Clock Frequency | Standard Mode | 0 | | 100 | kHz |
| | | Fast Mode | 0 | | 400 | kHz |
| $t_{LOW}$ | SCL Low Period | Standard Mode | 4.7 | | | us |
| | | Fast Mode | 1.3 | | | us |
| $t_{HIGH}$ | SCL High Period | Standard Mode | 4.0 | | | us |
| | | Fast Mode | 0.6 | | | us |
| $t_{HD;STA}$ | Hold time for a start or a repeated start condition, Figure 13 | Standard Mode | 4.0 | | | us |
| | | Fast Mode | 0.6 | | | us |

## Recommended Timing for the Serial Control Bus (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{SU:STA}$ | Set Up time for a start or a repeated start condition, Figure 13 | Standard Mode | 4.7 | | | us |
| | | Fast Mode | 0.6 | | | us |
| $t_{HD;DAT}$ | Data Hold Time, Figure 13 | Standard Mode | 0 | | 3.45 | us |
| | | Fast Mode | 0 | | 0.9 | us |
| $t_{SU;DAT}$ | Data Set Up Time, Figure 13 | Standard Mode | 250 | | | ns |
| | | Fast Mode | 100 | | | ns |
| $t_{SU;STO}$ | Set Up Time for STOP Condition, Figure 13 | Standard Mode | 4.0 | | | us |
| | | Fast Mode | 0.6 | | | us |
| $t_{BUF}$ | Bus Free Time Between STOP and START, Figure 13 | Standard Mode | 4.7 | | | us |
| | | Fast Mode | 1.3 | | | us |
| $t_r$ | SCL & SDA Rise Time, Figure 13 | Standard Mode | | | 1000 | ns |
| | | Fast Mode | | | 300 | ns |
| $t_f$ | SCL & SDA Fall Time, Figure 13 | Standard Mode | | | 300 | ns |
| | | Fast mode | | | 300 | ns |

## DC and AC Serial Control Bus Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Level | SDA and SCL | 0.7* $V_{DDIO}$ | | $V_{DDIO}$ | V |
| $V_{IL}$ | Input Low Level Voltage | SDA and SCL | GND | | 0.3* $V_{DDIO}$ | V |
| $V_{HY}$ | Input Hysteresis | | | >50 | | mV |
| $V_{OL}$ | | SDA, $I_{OL}$ = +0.5 mA | 0 | | 0.36 | V |
| $I_{in}$ | | SDA or SCL, Vin = $V_{DDIO}$ or GND | -10 | | +10 | µA |
| $t_R$ | SDA RiseTime – READ | SDA, RPU = X, Cb ≤ 400pF | | | 850 | ns |
| $t_F$ | SDA Fall Time – READ | | | | 120 | ns |
| $t_{SU;DAT}$ | Set Up Time — READ | | 500 | | | ns |
| $t_{HD;DAT}$ | Hold Up Time — READ | | 580 | | | ns |
| $t_{SP}$ | Input Filter | | | 50 | | ns |
| $C_{in}$ | Input Capacitance | SDA or SCL | | <5 | | pF |

## AC Timing Diagrams and Test Circuits

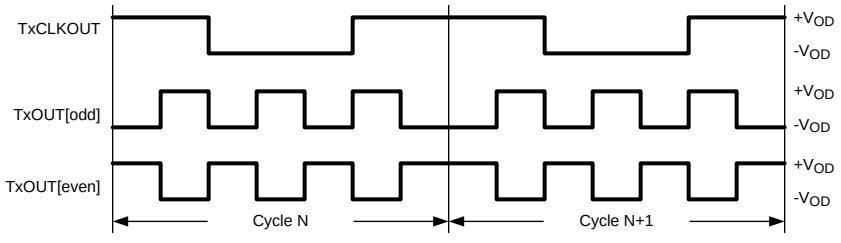



**Figure 4. Checkerboard Data Pattern**

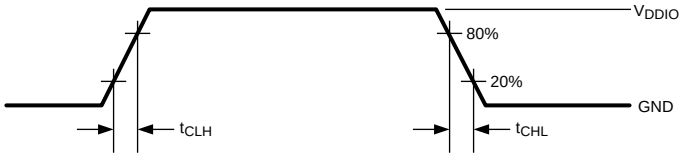



**Figure 5. LVCMOS Transition Times**

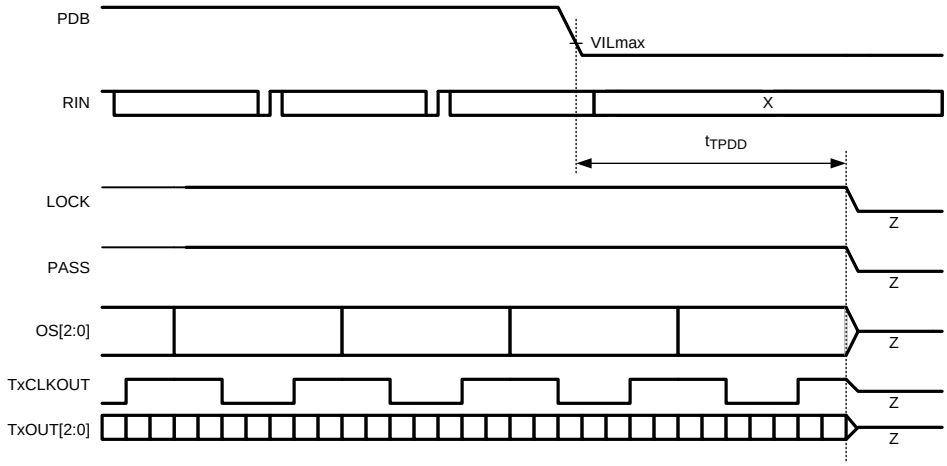



**Figure 6. FPD-Link & LVCMOS Powerdown Delay**

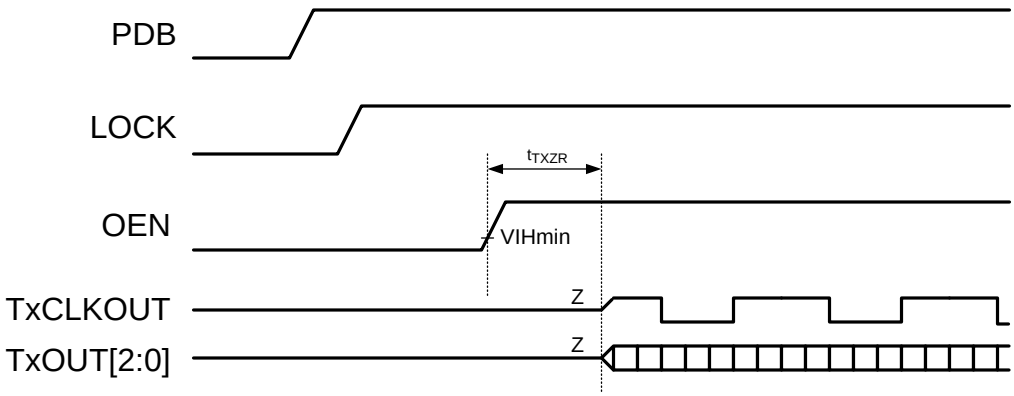



**Figure 7. FPD-Link Outputs Enable Delay**

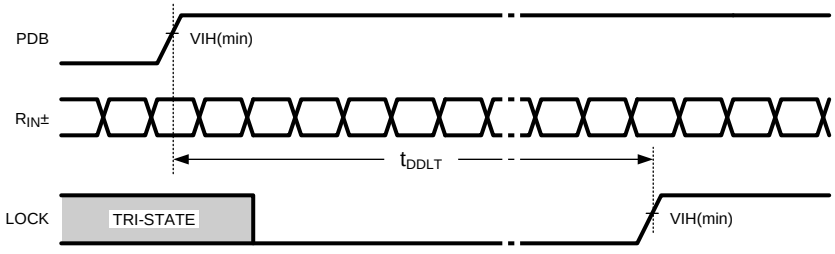



**Figure 8. Deserializer PLL Lock Times**

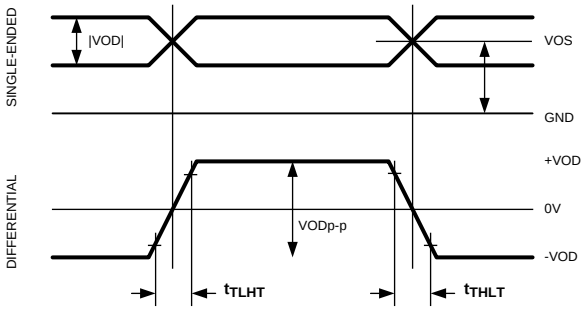



**Figure 9. FPD-Link (LVDS) Single-ended and Differential Waveforms**

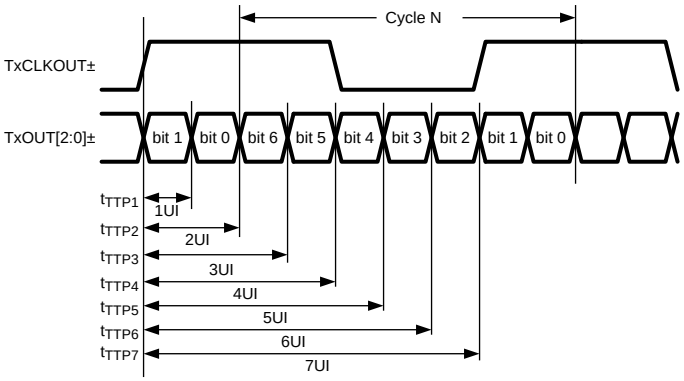



**Figure 10. FPD-Link Transmitter Pulse Positions**

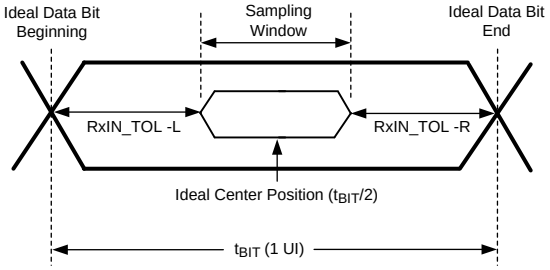



**Figure 11. Receiver Input Jitter Tolerance**

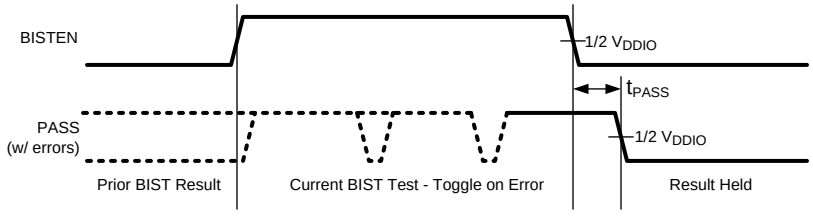



**Figure 12. BIST PASS Waveform**

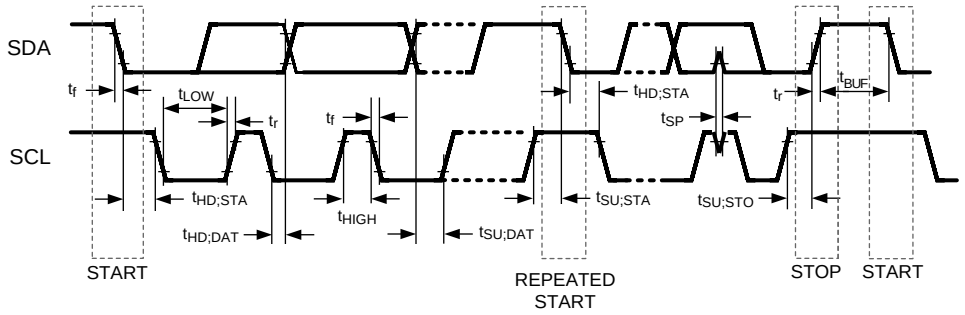



**Figure 13. Serial Control Bus Timing Diagram**

## Typical Performance Characteristics

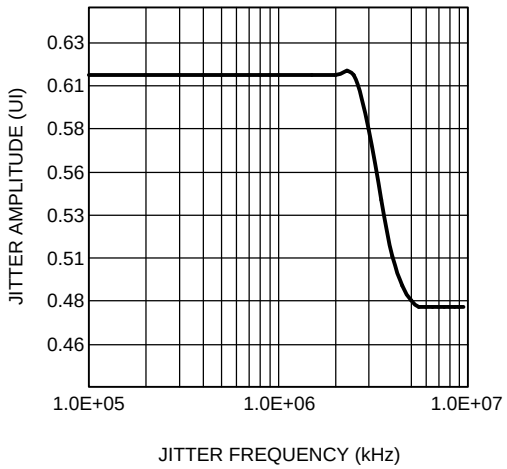



**Figure 14. Typical Input Jitter Tolerance Curve at 43 MHz**

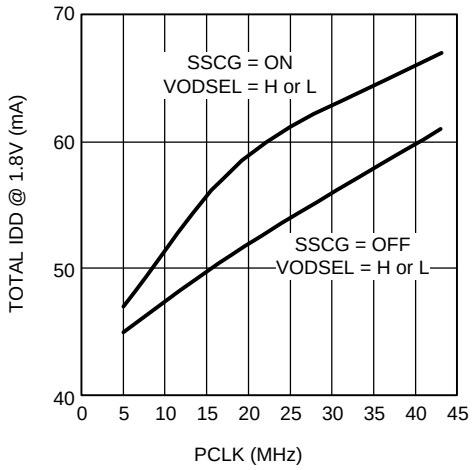



**Figure 15. Typical Total IDD Current (1.8V Supply) as a Function of PCLK**

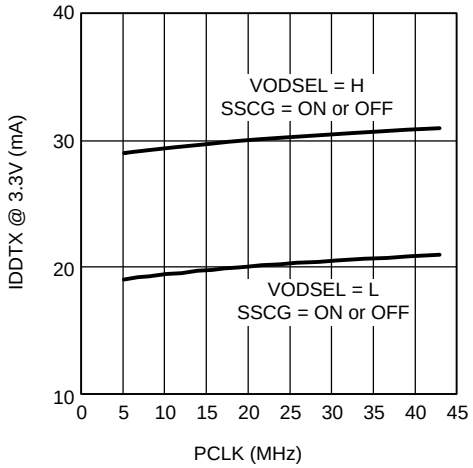



**Figure 16. Typical IDDTX Current (3.3V Supply) as a Function of PCLK**

## FUNCTIONAL DESCRIPTION

The DS99R124Q receives 24-bits of data over a single serial FPD-Link II pair operating at 140Mbps to 1.2Gbps. The serial stream also contains an embedded clock, and the DC-balance information which enhances signal quality and supports AC coupling. The receiver copnverts the serial stream into a 4-channel (3 data and 1 clock) FPD-Link LVDS Interface. The device is intended to be used with the DS90UR241or the DS99R421 FPD-Link II serializers.

The Des converts a single input serial data stream to a FPD-Link output bus, and also provides a signal check for the chipset Built In Self Test (BIST) mode. The device can be configured via external pins or through the optional serial control bus. The Des features enhance signal quality on the link by supporting the FPD-Link II data coding that provides randomization, scrambling, and DC balancing of the data. The Des includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the data, FPD-Link LVDS Output interface, and also the output spread spectrum clock generation (SSCG) support. The Des' power saving features include a power down mode, and optional LVCMOS (1.8 V) interface compatibility.

The Des can attain lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The Des also synchronizes to the Ser regardless of the data pattern, delivering true automatic “plug and lock” performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The Des recovers the clock and data by extracting the embedded clock information, validating and then deserializing the incoming data stream.

The DS99R421Q / DS99R124Q chipset supports 18-bit color depth, HS, VS and DE video control signals and up to three over-sampled low-speed (general purpose) data bits.

### DATA TRANSFER

The DS99R124 will receive a pixel of data in the following format: C1 and C0 represent the embedded clock in the serial stream. C1 is always HIGH and C0 is always LOW. b[23:0] contain the scrambled data. DCB is the DC-Balanced control bit. DCB is used to minimize the short and long-term DC bias on the signal lines. This bit determines if the data is unmodified or inverted. DCA is used to validate data integrity in the embedded data stream. Both DCA and DCB coding schemes are generated by the Ser and decoded by the Des automatically. Figure 17 illustrates the serial stream per PCLK cycle.

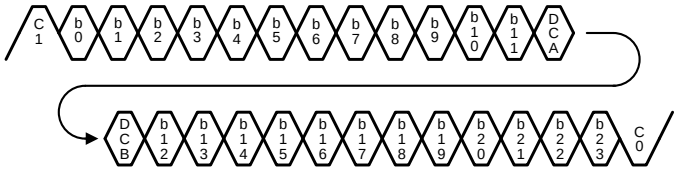



**Figure 17. FPD-Link II Serial Stream (DS99R421/DS99R124)**

The device supports clocks in the range of 5 MHz to 43 MHz. With every clock cycle 24 bits of payload are received along with the four overhead bits. Thus, the line rate is 1.2 Gbps maximum (140 Mbps minimum) with an effective data rate of 1.03 Gbps maximum. The link is extremely efficient at 86% (24/28).

The FPD-Link output will pass along the data to the Display in the format shown in Figure 18.

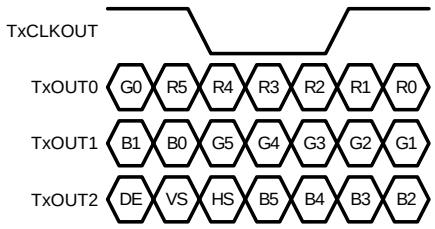



**Figure 18. FPD-Link Output Format**

## FPD-LINK II INPUT

### *Common Mode Filter Pin (CMF) — Optional*

The Des provides access to the center tap of the internal termination. A capacitor may be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high noise environments for additional noise rejection capability. A 4.7 µF capacitor may be connected to this pin to Ground.

## OUTPUT INTERFACES (LVCMOS & FPD-LINK)

### *OS[2:0] LVCMOS Outputs*

Additional signals maybe received across the serial link per PCLK. The over-sampled bits are restricted to be low speed signals and should be less than 1/5 of the frequency of the PCLK. Signals should convey level information only, as pulse width distrotion will occur by the over sampling technique and location of the sampling clock. The three over sampled bits are exactly mapped to DS99R421's; and to DS90UR421 bits are: OS0 = DIN21, OS1 = DIN22, and OS2 = DIN23.

### *CLOCK-DATA RECOVERY STATUS FLAG (LOCK) and OUTPUT STATE SELECT (OSS_SEL)*

When PDB is driven HIGH, the CDR PLL begins locking to the serial input, LOCK is Low and the FPD-Link interface state is determined by the state of the OSS_SEL pin.

After the DS99R124Q completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the FPD-Link outputs. The TxCLK output is held at its current state at the change from OSC_CLK (if this is enabled via OSC_SEL) to the recovered clock (or vice versa). Note that the FPD-Link outputs may be held in an inactive state (TRI-STATE) through the use of the Output Enable pin (OEN).

If there is a loss of clock from the input serial stream, LOCK is driven Low and the state of the outputs are based on the OSS_SEL setting (configuration pin or register).

**Table 1. Output State Table**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| **PDB** | **OEN** | **OSS_SEL** | **LOCK** | **OTHER OUTPUTS** |
| L | X | L | Z | TxCLKOUT is TRI-STATE<br>TxOUT[2:0] areTRI-STATE<br>OS[2:0] are TRI-STATE<br>PASS is TRI-STATE |
| L | X | H | L | TxCLKOUT is TRI-STATE<br>TxOUT[2:0] areTRI-STATE<br>OS[2:0] are LOW<br>PASS is TRI-STATE |
| H | L | L | L | TxCLKOUT is TRI-STATE<br>TxOUT[2:0] areTRI-STATE<br>OS[2:0] are LOW<br>PASS is HIGH |
| H | L | H | L | TxCLKOUT is TRI-STATE<br>TxOUT[2:0] areTRI-STATE<br>OS[2:0] are LOW<br>PASS is LOW |
| H | H | L | L | TxCLKOUT is TRI-STATE<br>TxOUT[2:0] areTRI-STATE<br>OS[2:0] are TRI-STATE<br>PASS is HIGH |
| H | H | H | L | TxCLKOUT is TRI-STATE<br>TxOUT[2:0] areLOW<br>OS[2:0] are LOW<br>PASS is LOW |

**Table 1. Output State Table (continued)**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| **PDB** | **OEN** | **OSS_SEL** | **LOCK** | **OTHER OUTPUTS** |
| H | L | X | H | TxCLKOUT is TRI-STATE<br>TxOUT[2:0] areTRI-STATE<br>OS[2:0] are Active<br>PASS is Active<br>*(This setting allows the system to run BIST or use the OS[2:0] bits while the panel is off)* |
| H | H | X | H | TxCLKOUT is Active<br>TxOUT[2:0] are Active<br>OS[2:0] are Active<br>PASS is Active<br>*(Normal operating mode)* |

### *LVCMOS 1.8V / 3.3V VDDIO Operation*

The LVCMOS inputs and outputs can operate with 1.8 V or 3.3 V levels ($V_{DDIO}$) for target (Display) compatibility. The 1.8 V levels will offer a lower noise (EMI) and also a system power savings.

### *FPD-LINK OUTPUT*

#### VODSEL

The differential output voltage of the FPD-Link interface is controlled by the VODSEL input.

**Table 2. VODSEL Configuration Table**

| VODSEL | Result |
|---|---|
| L | VOD is 250mV TYP (500mVp-p) |
| H | VOD is 400mV TYP (800mVp-p) |

### SSCG Generation — Optional

The Des provides an internally generated spread spectrum clock (SSCG) to modulate its outputs. Both clock and data outputs are modulated. This will aid to lower system EMI. Output SSCG deviations to ±2.0% (4% total) at up to 35kHz modulations nominally are available. See Table 3 and Table 4. This feature may be controlled by pins or by register. The LFMODE should be set appropriately if the SSCG is being used. Set LFMODE High if the clock frequency is between 5 MHz and 20 MHz, set LFMODE Low if the clock frequency is between 20 MHz and 43 MHz.

**Table 3. SSCG Configuration (LFMODE = L) — Des Output**

| SSC[2:0] Inputs LFMODE = L (20 - 43 MHz) | | | Result | |
|---|---|---|---|---|
| **SSC2** | **SSC1** | **SSC0** | **fdev (%)** | **fmod (kHz)** |
| L | L | L | OFF | OFF |
| L | L | H | ±0.9 | CLK/2168 |
| L | H | L | ±1.2 | |
| L | H | H | ±1.9 | |
| H | L | L | ±2.3 | |
| H | L | H | ±0.7 | CLK/1300 |
| H | H | L | ±1.3 | |
| H | H | H | ±1.7 | |

**Table 4. SSCG Configuration (LFMODE = H) — Des Output**

| SSC[2:0] Inputs LFMODE = H (5 - 20 MHz) | | | Result | |
|---|---|---|---|---|
| SSC2 | SSC1 | SSC0 | fdev (%) | fmod (kHz) |
| L | L | L | OFF | OFF |
| L | L | H | ±0.7 | CLK/625 |
| L | H | L | ±1.3 | |
| L | H | H | ±1.8 | |
| H | L | L | ±2.2 | |
| H | L | H | ±0.7 | CLK/385 |
| H | H | L | ±1.2 | |
| H | H | H | ±1.7 | |

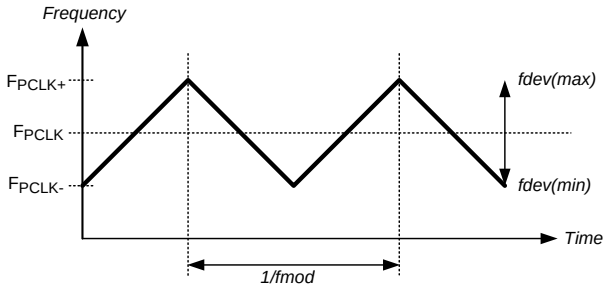



**Figure 19. SSCG Waveform**

## POWER SAVING FEATURES

### *PowerDown Feature (PDB)*

The Des has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the system to save power, disabling the Des when the display is not needed. An auto detect mode is also available. In this mode, the PDB pin is tied High and the Des will enter POWER DOWN when the serial stream stops. When the serial stream starts up again, the Des will lock to the input stream and assert the LOCK pin and output valid data. In POWER DOWN mode, the Data and PCLK output states are determined by the OSS_SEL status. Note – in POWER DOWN, the optional Serial Bus Control Registers are **RESET**.

### *Stop Stream SLEEP Feature*

The Des will enter a low power SLEEP state when the input serial stream is stopped. A STOP condition is detected when the embedded clock bits are not present. When the serial stream starts again, the Des will then lock to the incoming signal and recover the data. Note – in STOP STREAM SLEEP, the optional Serial Bus Control Registers values are **RETAINED**.

## Built In Self Test (BIST) — Optional

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high-speed serial link. This is useful in the prototype stage, equipment production, in-system test and also for system diagnostics. In the BIST mode only an input clock is required along with control to the Ser and Des BISTEN input pins. The Ser outputs a test pattern (PRBS7) and drives the link at speed. The Des detects the PRBS7 pattern and monitors it for errors. The PASS output pin toggles to flag any payloads that are received with 1 to 24 bit errors. The BISTM pin selects the operational mode of the PASS pin. If BISTM = L, the PASS pins reports the final result only. If BISTM = H, the PASS pins counts payload errors and also results the result. The result of the test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the Des BISTEN pin.

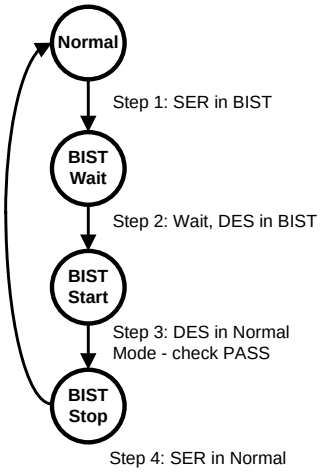



**Figure 20. BIST Mode Flow Diagram**

### Sample BIST Sequence

See Figure 20 for the BIST mode flow diagram.

1. For the DS99R421 FPD-Link II Ser BIST Mode is enabled via the BISTEN pin. For the DS90UR241 Ser, BIST mode is enetered by setting all the input data of the device to Low state. A PCLK is required for all the Ser options. When the Des detects the BIST mode pattern and command (DCA and DCB code) the RGB and control signal outputs are shut off.
2. Place the DS99R124Q Des in BIST mode by setting the BISTEN = H. The Des is now in the BIST mode. If BISTM = H, the Des will check the incoming serial payloads for errors. If an error in the payload (1 to 24) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.
3. To Stop the BIST mode, the Des BISTEN pin is set Low. The Des stops checking the data. The final test result is held on the PASS pin. If the test ran error free, the PASS output will be High. If there was one or more errors detected, the PASS output will be Low. The PASS output state is held until a new BIST is run, the device is RESET, or Powered Down. The BIST duration is user controlled by the duration of the BISTEN signal.
4. To return the link to normal operation, the Ser BISTEN input is set Low. The Link returns to normal operation.

Figure 21 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, reducing signal condition enhancements (De-Emphasis, VODSEL, or Rx Equalization).

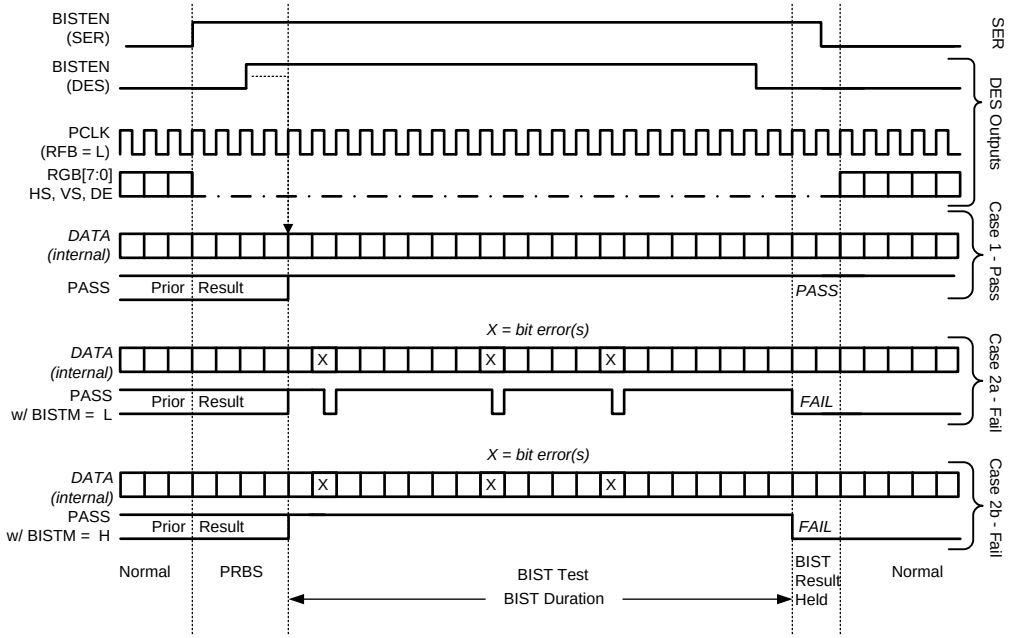



**Figure 21. BIST Waveforms**

## Serial Bus Control — Optional

The DS99R124 may also be configured by the use of a serial control bus that is I2C protocol compatible. By default, the I2C reg_0x00'h is set to 00'h and all configuration is set by control/strap pins. A write of 01'h to reg_0x00'h will enable/allow configuration by registers; this will override the control/strap pins. Multiple devices may share the serial control bus since multiple addresses are supported. See Figure 22.

The serial bus is comprised of three pins. The SCL is a Serial Bus Clock Input. The SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull up resistor to $V_{DDIO}$. For most applications a 4.7 k pull up resistor to $V_{DDIO}$ may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

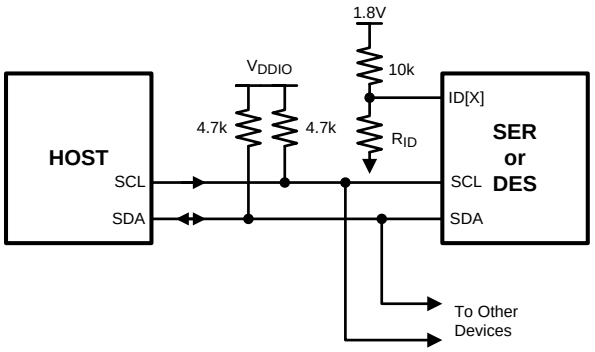



**Figure 22. Serial Control Bus Connection**

The third pin is the ID[X] pin. This pin sets one of four possible device addresses. Two different connections are possible. The pin may be pulled to $V_{DD}$ (**1.8V, NOT $V_{DDIO}$**)) with a 10 kΩ resistor. Or a 10 kΩ pull up resistor (to $V_{DD}$**1.8V, NOT $V_{DDIO}$**)) and a pull down resistor of the recommended value to set other three possible addresses may be used. See Table 5 for the Des.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transition High while SCL is also HIGH. See Figure 23

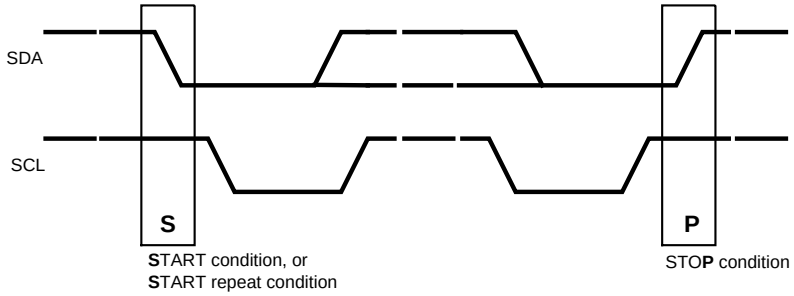



**Figure 23. START and STOP Conditions**

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 24 and a WRITE is shown in Figure 25.

If the Serial Bus is not required, the three pins may be left open (NC).

**Table 5. ID[x] Resistor Value – DS99R124Q Des**

| Resistor RID kΩ (5%tol) | Address 7'b | Address 8'b 0 appended (WRITE) |
|---|---|---|
| 0.47 | 7b' 111 0001 (h'71) | 8b' 1110 0010 (h'E2) |
| 2.7 | 7b' 111 0010 (h'72) | 8b' 1110 0100 (h'E4) |
| 8.2 | 7b' 111 0011 (h'73) | 8b' 1110 0110 (h'E6) |
| Open | 7b' 111 0110 (h'76) | 8b' 1110 1100 (h'EC) |

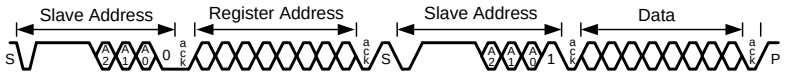



**Figure 24. Serial Control Bus — READ**

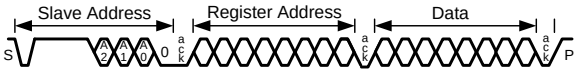



**Figure 25. Serial Control Bus — WRITE**

**Table 6. DS99R124Q — Serial Bus Control Registers**

| ADD (dec) | ADD (hex) | Register Name | Bit(s) | R/W | Default (bin) | Function | Description |
|---|---|---|---|---|---|---|---|
| 0 | 0 | Des Config 1 | 7 | R/W | 0 | LFMODE | SSCG Mode – low frequency support<br>0: 20 to 43 MHz Operation<br>1: 5 to 20 MHz Operation |
| | | | 6 | R/W | 0 | OSS_SEL | Output Sleep State Select<br>TBD |
| | | | 5 | R/W | 0 | ***Reserved*** | ***Reserved*** |
| | | | 4 | R/W | 0 | ***Reserved*** | ***Reserved*** |
| | | | 3:2 | R/W | 00 | ***Reserved*** | ***Reserved*** |
| | | | 1 | R/W | 0 | SLEEP | Note – not the same function as $\overline{\text{PowerDown}}$ (PDB)<br>0: normal mode<br>1: Sleep Mode – **Register settings retained.** |
| | | | 0 | R/W | 0 | REG Control | 0: Configurations set from control pins<br>1: Configurations set from registers (except I2C_ID) |
| 1 | 1 | Slave ID | 7 | R/W | 0 | ADD_SEL | 0: Address from ID[X] Pin<br>1: Address from Register |
| | | | 6:0 | R/W | 1110000 | ID[X] | Serial Bus Device ID, Four IDs are:<br>7b '1110 001 (h'71); 8b ' 1110 0010 (h'E2)<br>7b '1110 010 (h'72); 8b ' 1110 0100 (h'E4)<br>7b '1110 011 (h'73); 8b ' 1110 0110 (h'E6)<br>7b '1110 110 (h'76); 8b ' 1110 1100 (h'EC)<br>All other addresses are ***Reserved***. |
| 2 | 2 | Des Features 1 | 7 | R/W | 0 | OEN | Output Enable Input<br>0: FPD-Link output are TRI-STATE<br>1: FPD-Link outputs are enabled (active) |
| | | | 6 | R/W | 0 | ***Reserved*** | ***Reserved*** |
| | | | 5:4 | R/W | 00 | ***Reserved*** | ***Reserved*** |
| | | | 3 | R/W | 0 | VODSEL | Differential Driver Output Voltage Select<br>0: LVDS VOD is ±250 mV, 500 mVp-p (typ)<br>1: LVDS VOD is ±400 mV, 800 mVp-p (typ) |
| | | | 2:0 | R/W | 00 | OSC_SEL | 000: OFF<br>001: ***Reserved***<br>010: 25 MHz ±40%<br>011: 16.7 MHz ±40%<br>100: 12.5 MHz ±40%<br>101: 10 MHz ±40%<br>110: 8.3 MHz ±40%<br>111: 6.3 MHz ±40% |

**Table 6. DS99R124Q — Serial Bus Control Registers (continued)**

| ADD (dec) | ADD (hex) | Register Name | Bit(s) | R/W | Default (bin) | Function | Description |
|---|---|---|---|---|---|---|---|
| 3 | 3 | Des Features 2 | 7:5 | R/W | 000 | EQ Gain | 000: ~1.625 dB<br>001: ~3.25 dB<br>010: ~4.87 dB<br>011: ~6.5 dB<br>100: ~8.125 dB<br>101: ~9.75 dB<br>110: ~11.375 dB<br>111: ~13 dB |
| | | | 4 | R/W | 0 | EQ Enable | 0: EQ = disabled<br>1: EQ = enabled |
| | | | 3 | R/W | 0 | ***Reserved*** | ***Reserved*** |
| | | | 2:0 | R/W | 000 | SSC | **IF LFMODE = 0, then**:<br>000: SSCG OFF<br>001: fdev = ±0.9%, fmod = CLK/2168<br>010: fdev = ±1.2%, fmod = CLK/2168<br>011: fdev = ±1.9%, fmod = CLK/2168<br>100: fdev = ±2.3%, fmod = CLK/2168<br>101: fdev = ±0.7%, fmod = CLK/1300<br>110: fdev = ±1.3%, fmod = CLK/1300<br>111: fdev = ±1.57%, fmod = CLK/1300<br>**IF LFMODE = 1, then**:<br>000: SSCG OFF<br>001: fdev = ±0.7%, fmod = CLK/625<br>010: fdev = ±1.3%, fmod = CLK/625<br>011: fdev = ±1.8%, fmod = CLK/625<br>100: fdev = ±2.2%, fmod = CLK/625<br>101: fdev = ±0.7%, fmod = CLK/385<br>110: fdev = ±1.2%, fmod = CLK/385<br>111: fdev = ±1.7%, fmod = CLK/385 |

# APPLICATIONS INFORMATION

## DISPLAY APPLICATION

The DS99R124Q, in conjunction with the DS99R421Q or DS90UR241Q, is intended for interfacing between a host (graphics processor) and a Display. It supports an 18-bit color depth (RGB666) and up to WVGA display formats. In a RGB666 application, 18 color bits (R[5:0], G[5:0], B[5:0]), Pixel Clock (PCLK) and three control bits (VS, HS and DE) are supported across the serial link with PCLK rates from 5 to 43MHz.

## TYPICAL APPLICATION CONNECTION

Figure 26 shows a typical application of the DS99R124QQ Des in pin mode for a 43 MHz WVGA Display Application. The LVDS inputs utilize 100 nF coupling capacitors to the line and the Receiver provides internal termination. Bypass capacitors are placed near the power supply pins. Ferrite beads are placed on the power lines for effective noise suppression.

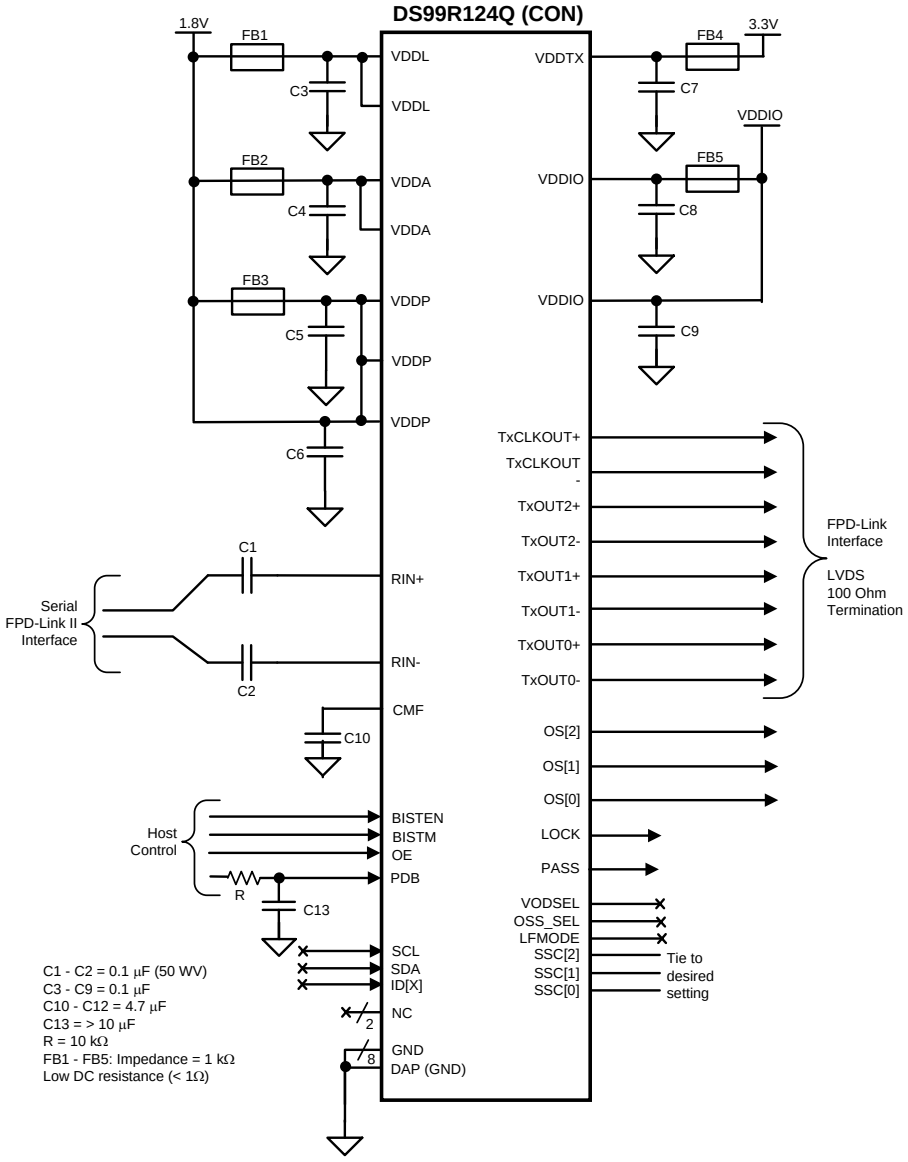



**Figure 26. DS99R124Q Typical Connection Diagram — Pin Control**

## POWER UP REQUIREMENTS AND PDB PIN

The VDD ($V_{DDn}$), $V_{DDTX}$ and $V_{DDIO}$ supply ramps should be faster than 1.5 ms with a monotonic rise. Supplies may power up in any order, however device operation should be initiated only after all supplies are in their valid operating ranges. The optional serial bus address selection is done upon power up also. Thus, if using this optional feature, the PDB signal must be delayed to allow time for the ID setting to occur. The delay maybe done by simply holding the PDB pin at a Low, or with an external RC delay based off the $V_{DDIO}$ rail which would then need to lag the others in time. If the PDB pin is pulled to $V_{DDIO}$, it is recommended to use a 10 kΩ pull-up and a 10 uF cap to GND to delay the PDB input signal.

## TRANSMISSION MEDIA

The Ser/Des chipset is intended to be used in a point-to-point configuration, through a PCB trace, or through twisted pair cable. The Ser and Des provide internal terminations providing a clean signaling environment. The interconnect for LVDS should present a differential impedance of 100 Ohms. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Shielded or un-shielded cables may be used depending upon the noise environment and application requirements.

## LIVE LINK INSERTION

The Ser and Des devices support live pluggable applications. The automatic receiver lock to random data “plug & go” hot insertion capability allows the DS99R124Q to attain lock to the active data stream during a live insertion event.

## PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the LVDS Ser/Des devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the WQFN style package is provided in Texas Instruments Note: AN-1187 (SNOA401).

## LVDS INTERCONNECT GUIDELINES

See AN-1108 (SNLA008) and AN-905 (SNLA035) for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the TI web site at: http://www.ti.com/ww/en/analog/interface/lvds.shtml

## REVISION HISTORY

| Changes from Revision C (April 2013) to Revision D | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 25 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DS99R124QSQ/NOPB | ACTIVE | WQFN | RHS | 48 | 1000 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 105 | DS99R124Q | Samples |
| DS99R124QSQE/NOPB | ACTIVE | WQFN | RHS | 48 | 250 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 105 | DS99R124Q | Samples |
| DS99R124QSQX/NOPB | ACTIVE | WQFN | RHS | 48 | 2500 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 105 | DS99R124Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

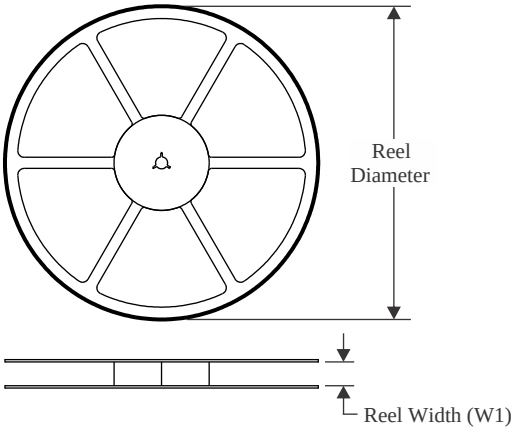
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

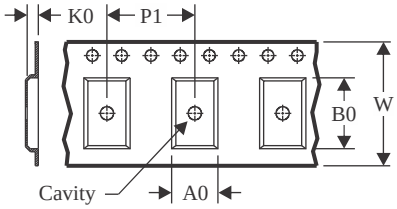
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

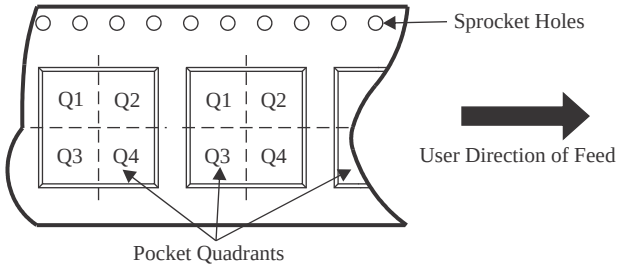



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

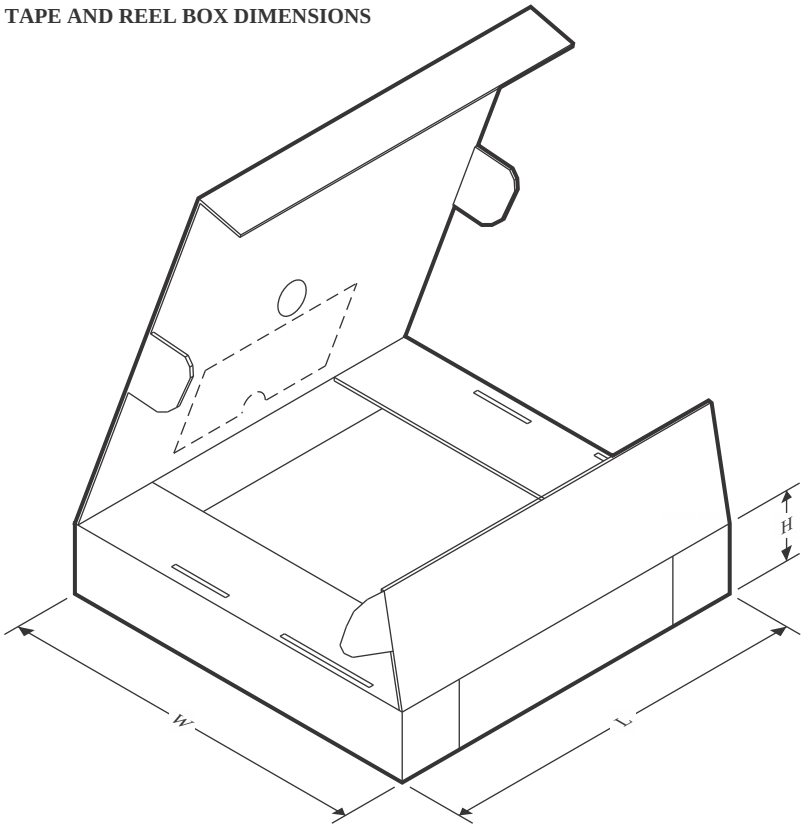
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DS99R124QSQ/NOPB | WQFN | RHS | 48 | 1000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| DS99R124QSQE/NOPB | WQFN | RHS | 48 | 250 | 178.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| DS99R124QSQX/NOPB | WQFN | RHS | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

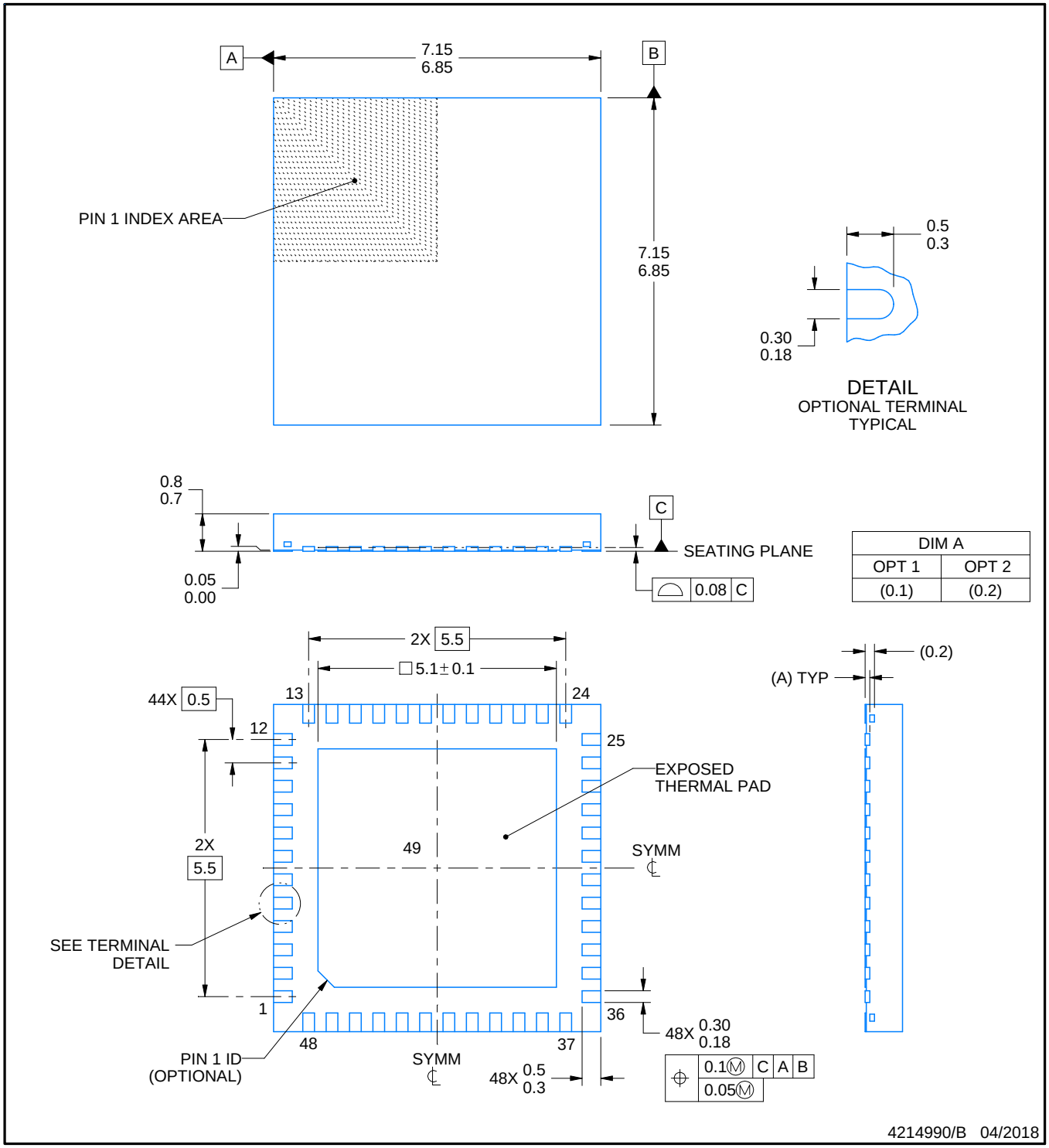
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DS99R124QSQ/NOPB | WQFN | RHS | 48 | 1000 | 356.0 | 356.0 | 35.0 |
| DS99R124QSQE/NOPB | WQFN | RHS | 48 | 250 | 208.0 | 191.0 | 35.0 |
| DS99R124QSQX/NOPB | WQFN | RHS | 48 | 2500 | 356.0 | 356.0 | 35.0 |

# PACKAGE OUTLINE

## RHS0048A

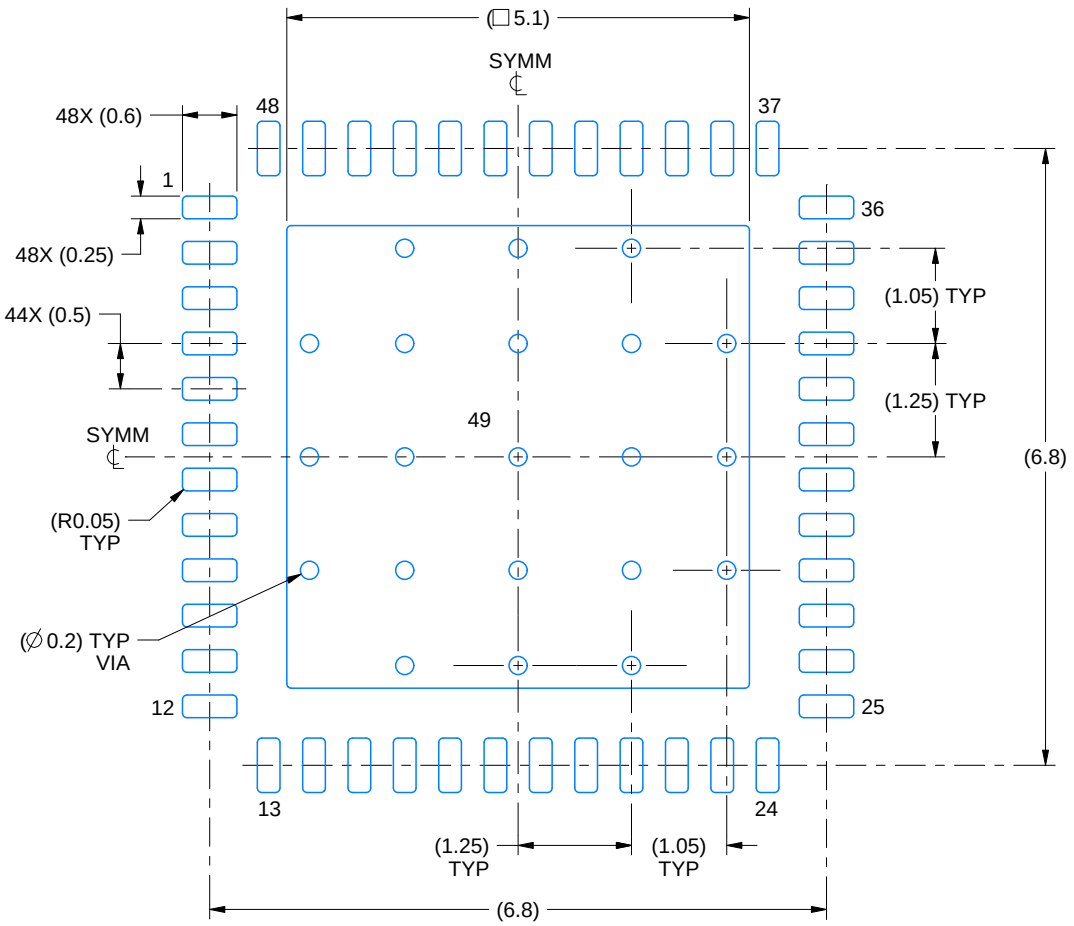
## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

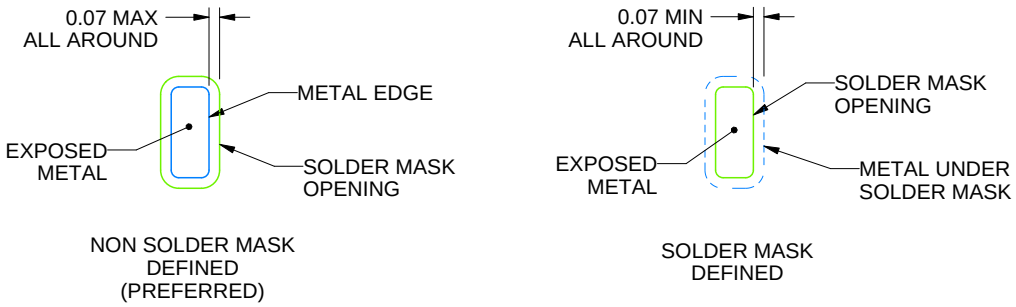



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

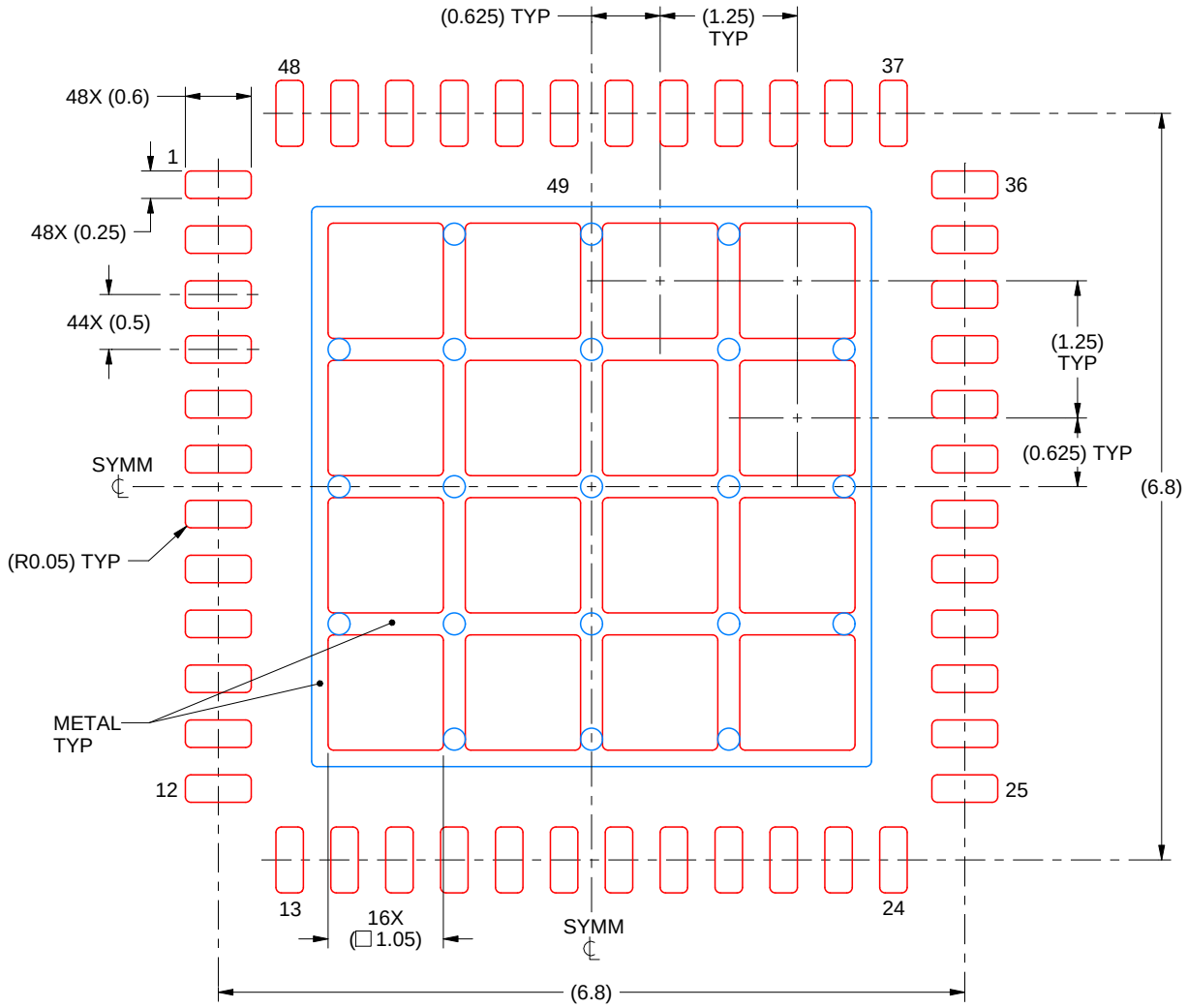



SOLDER MASK DETAILS

4214990/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4214990/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265