LMV33x-N / LMV393-N General-Purpose, Low-Voltage, Tiny Pack Comparators

1 Features

- (For 5-V Supply, Typical Unless Otherwise Noted)
- Ensured 2.7-V and 5-V Performance
- Industrial Temperature Range −40°C to 85°C
- Low Supply Current 60 µA/Channel
- Input Common Mode Voltage Range Includes Ground
- Low Output Saturation Voltage 200 mV
- Propagation Delay 200 ns
- Space-Saving 5-Pin SC70 and 5-Pin SOT23 Packages

2 Applications

- Mobile Communications
- Notebooks and PDAs
- Battery-Powered Electronics
- General-Purpose Portable Devices
- General-Purpose, Low-Voltage Applications

3 Description

The LMV393-N and LMV339-N are low-voltage (2.7 to 5 V) versions of the dual and quad comparators, LM393/339, which are specified at 5 to 30 V. The LMV331-N is the single version, which is available in space-saving, 5-pin SC70 and 5-pin SOT23 packages. The 5-pin SC70 is approximately half the size of the 5-pin SOT23.

The LMV393-N is available in 8-pin SOIC and VSSOP packages. The LMV339-N is available in 14-pin SOIC and TSSOP packages.

The LMV331-N/393-N/339-N is the most cost-effective solution where space, low voltage, low power, and price are the primary specification in circuit design for portable consumer products. They offer specifications that meet or exceed the familiar LM393/339 at a fraction of the supply current.

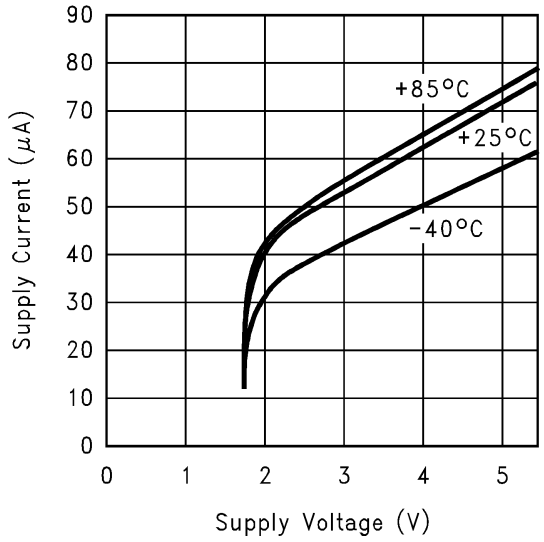
The chips are built with TI's advanced Submicron Silicon-Gate BiCMOS process. The LMV331-N/393-N/339-N have bipolar input and output stages for improved noise performance.

Table 1. Device Information(1)

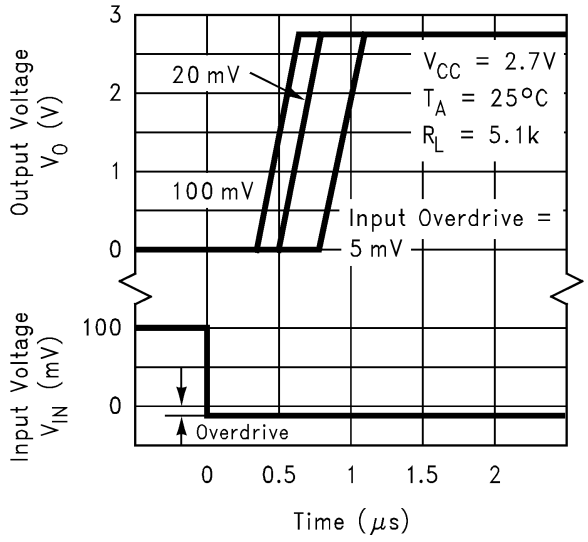
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV331-N	SC70 (5)	2.00 mm × 1.25 mm
	SOT-23 (5)	2.90 mm × 1.6 mm
LMV339-N	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm
LMV393-N	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Low Supply Current



Fast Response Time



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (Feburary 2013) to Revision H	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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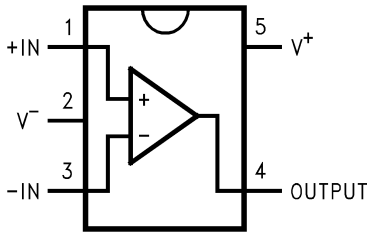
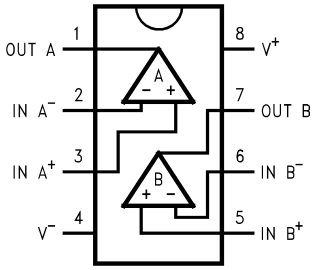
5 Pin Configuration and Functions

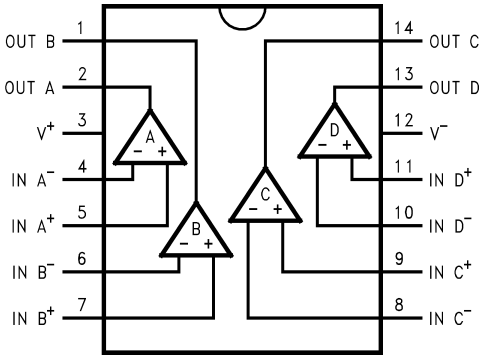
DCK and DBV Package
5-Pin SC70 / SOT23
Top View



D and DGK Package
8-Pin SOIC / VSSOP
Top View



D and PW Package
14-Pin SOIC / TSSOP
Top View



Pin Functions

PIN				TYPE	DESCRIPTION
NAME	LMV331-N DVB,DCK	LMV393-N D,DGK	LMV339-N PW		
+IN	1	-	-	I	Noninverting input
+IN A	-	3	5	I	Noninverting input, channel A
+IN B	-	5	7	I	Noninverting input, channel B
+IN C	-	-	9	I	Noninverting input, channel C
+IN D	-	-	11	I	Noninverting input, channel D
-IN	3	-	-	I	Inverting input
-IN A	-	2	4	I	Inverting input, channel A
-IN B	-	6	6	I	Inverting input, channel B
-IN C	-	-	8	I	Inverting input, channel C
-IN D	-	-	10	I	Inverting input, channel D
OUT	4	-	-	O	Output
OUT A	-	1	2	O	Output, channel A
OUT B	-	7	1	O	Output, channel B
OUT C	-	-	14	O	Output, channel C
OUT D	-	-	13	O	Output, channel D
V+	5	8	3	P	Positive (highest) power supply
V-	2	4	12	P	Negative (lowest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

	MIN	MAX	UNIT
Differential Input Voltage		±Supply Voltage	
Voltage on any pin (referred to V^- pin)		5.5	V
Soldering Information			
Infrared or Convection (20 sec)		235	°C
Junction Temperature [3]		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±800	V
	Machine model	±120	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply Voltage	2.7	5	V
Temperature Range [2]	−40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

6.4 Thermal Information

THERMAL METRIC[1]	LMV331-N		LMV339-N		LMV393-N		UNIT
	DCK	DBV	D	PW	D	DGK	
	5 PINS	5 PINS	14 PINS	14 PINS	8 PINS	8 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	478	265	145	155	190	23	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 2.7-V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^- = 0V.

PARAMETER	TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
V_{OS} Input Offset Voltage			1.7	7	mV
TCV_{OS} Input Offset Voltage Average Drift	At the temperature extremes		5		µV/°C

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

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2.7-V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7V, V^- = 0V.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
I_B	Input Bias Current			10	250	nA
		At the temperature extremes			400	
I_{OS}	Input Offset Current			5	50	nA
		At the temperature extremes			150	
V_{CM}	Input Voltage Range			−0.1		V
				2.0		V
V_{SAT}	Saturation Voltage	I_{SINK} ≤ 1 mA		120		mV
I_O	Output Sink Current	V_O ≤ 1.5V	5	23		mA
I_S	Supply Current	LMV331-N		40	100	µA
		LMV393-N Both Comparators		70	140	µA
		LMV339-N All four Comparators		140	200	µA
	Output Leakage Current			.003		µA
		At the temperature extremes			1	

6.6 2.7-V AC Electrical Characteristics

T_J = 25°C, V^+ = 2.7 V, R_L = 5.1 kΩ, V^- = 0 V.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 10 mV		1000		ns
		Input Overdrive = 100 mV		350		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 10 mV		500		ns
		Input Overdrive = 100 mV		400		ns

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

6.7 5-V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5 V, V^- = 0 V.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
V_{OS}	Input Offset Voltage			1.7	7	mV
		At the temperature extremes			9	
TCV_{OS}	Input Offset Voltage Average Drift			5		µV/°C
I_B	Input Bias Current			25	250	nA
		At the temperature extremes			400	
I_{OS}	Input Offset Current			2	50	nA
		At the temperature extremes			150	
V_{CM}	Input Voltage Range			−0.1		V
				4.2		V
A_V	Voltage Gain		20	50		V/mV

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

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5-V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5 V, V^- = 0 V.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
V_{sat}	Saturation Voltage	I_{SINK} ≤ 4 mA		200	400	mV
		At the temperature extremes			700	
I_O	Output Sink Current	V_O ≤ 1.5V		84	10	mA
I_S	Supply Current	LMV331-N		60	120	µA
		At the temperature extremes			150	
		LMV393-N Both Comparators		100	200	µA
		At the temperature extremes			250	
		LMV339-N All four Comparators		170	300	µA
		At the temperature extremes			350	
	Output Leakage Current			.003		µA
		At the temperature extremes			1	

6.8 5-V AC Electrical Characteristics

T_J = 25°C, V^+ = 5 V, R_L = 5.1 kΩ, V^- = 0 V.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 10 mV		600		ns
		Input Overdrive = 100 mV		200		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 10 mV		450		ns
		Input Overdrive = 100 mV		300		ns

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

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6.9 Typical Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C

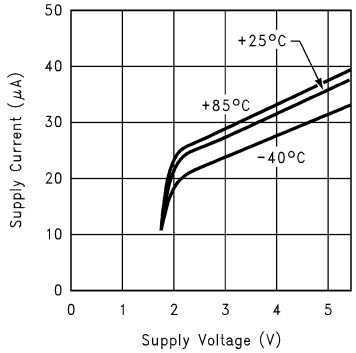

Figure 1. Supply Current vs. Supply Voltage Output High (LMV331-N)

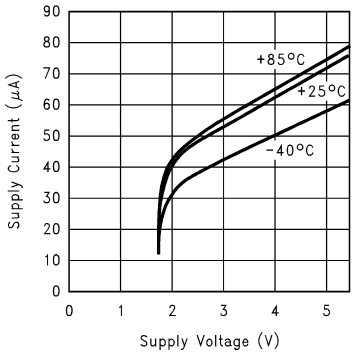

Figure 2. Supply Current vs. Supply Voltage Output Low (LMV331-N)

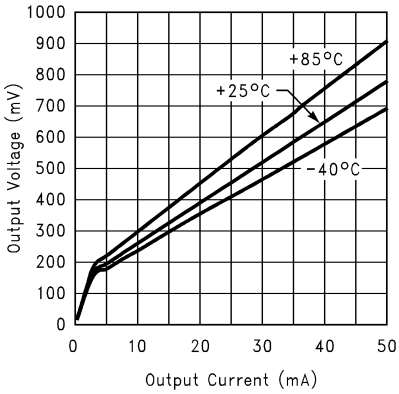

Figure 3. Output Voltage vs. Output Current at 5-V Supply

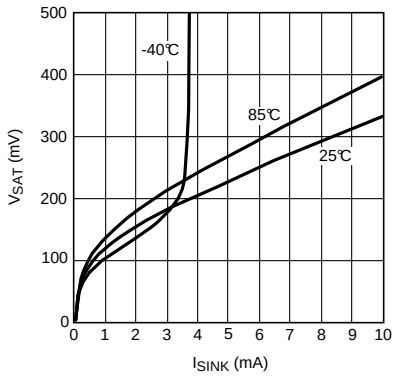

Figure 4. Output Voltage vs. Output Current at 2.7-V Supply

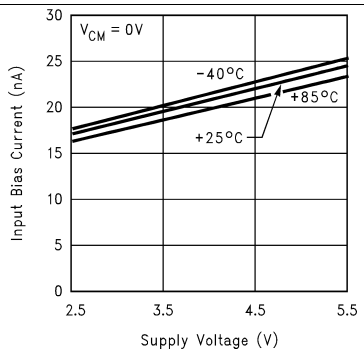

Figure 5. Input Bias Current vs. Supply Voltage

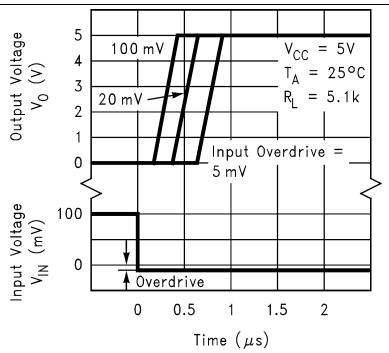

Figure 6. Response Time vs. Input Overdrive Negative Transition

Typical Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C

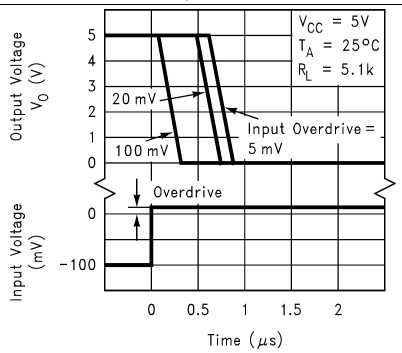

Figure 7. Response Time for Input Overdrive Positive Transition

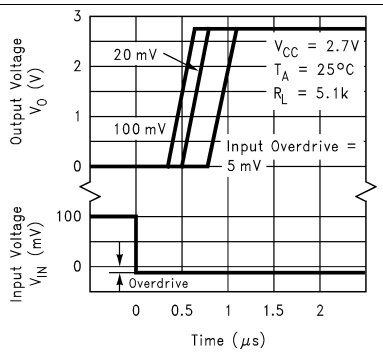

Figure 8. Response Time vs. Input Overdrive Negative Transition

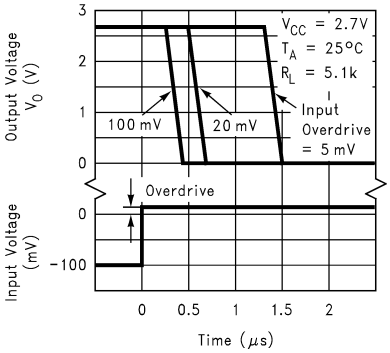

Figure 9. Response Time for Input Overdrive Positive Transition

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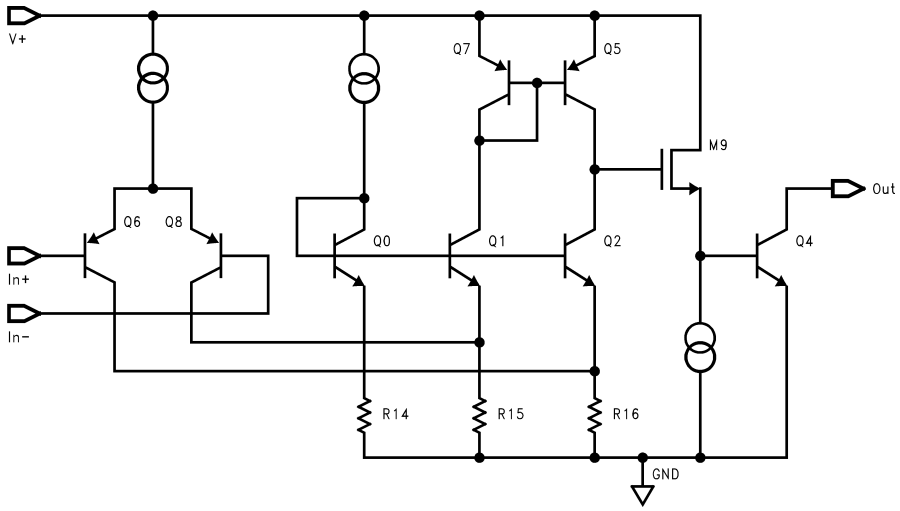
7 Detailed Description

7.1 Overview

The LMV331-N/393-N/339-N comparators features a supply voltage range of 2.7 V to 5 V with a low supply current of 55 µA/channel with propagation delays as low as 200ns. They are avaialble in small, space-saving packages, which makes these comparators versatile for use in a wide range of applications, from portable to industrial. The open collector output configuration allows the device to be used in wired-OR configurations, such as a window comparators.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Open Collector Output

The output of the LMV331-N/393-N/339-N series is the uncommitted collector of a grounded-emitter NPN output transistor, which requires a pull-up resistor to a positive supply voltage for the output to switch properly. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted V+ supply voltage range. The output pull-up resistor should be chosen high enough so as to avoid excessive power dissipation yet low enough to supply enough drive to switch whatever load circuitry is used on the comparator output. On the LMV331-N/393-N/339-N the pull-up resistor should range between 1 k to 10 kΩ.

7.3.2 Ground Sensing Input

The LMV331-N/393-N/339-N has a typical input common mode voltage range of −0.1V below the ground to 0.8V below Vcc.

7.4 Device Functional Modes

A basic comparator circuit is used for converting analog signals to a digital output.

The output is HIGH when the voltage on the non-inverting (+IN) input is greater than the inverting (-IN) input.

The output is LOW when the voltage on the non-inverting (+IN) input is less than the inverting (-IN) input.

The inverting input (-IN) is also commonly referred to as the "reference" or "V_{REF}" input.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Basic Comparator

The comparator compares the input voltage (V_{IN}) at the non-inverting pin to the reference voltage (V_{REF}) at the inverting pin. If V_{IN} is less than V_{REF}, the output voltage (V_O) is at the saturation voltage. On the other hand, if V_{IN} is greater than V_{REF}, the output voltage (V_O) is at V_{CC}.

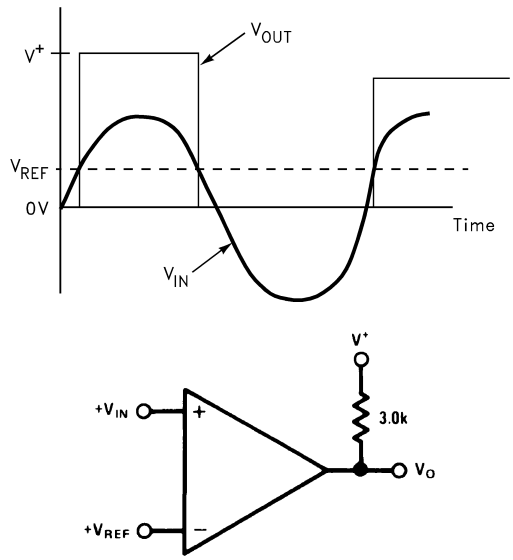


Figure 10. Basic Comparator

8.1.2 Comparator With Hysteresis

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by the addition of hysteresis or positive feedback.

8.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three resistor network that are referenced to the supply voltage V_{CC} of the comparator. When V_{in} at the inverting input is less than V_a, the voltage at the non-inverting node of the comparator ($V_{in} < V_a$), the output voltage is high (for simplicity assume V_O switches as high as V_{CC}). The three network resistors can be represented as $R_1//R_3$ in series with R_2. The lower input trip voltage V_{a1} is defined as:

$$V_{a_1} = \frac{V_{CC}\ R_2}{(R_1 \| R_3) + R_2} \tag{1}$$

When V_{in} is greater than V_a ($V_{in} > V_a$), the output voltage is low very close to ground. In this case the three network resistors can be presented as $R_2//R_3$ in series with R_1. The upper trip voltage V_{a2} is defined as:

$$V_{a2} = \frac{V_{CC}(R_2 // R_3)}{R_1 + (R_2 // R_3)} \tag{2}$$

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Application Information (continued)

The total hysteresis provided by the network is defined as:

$$\Delta V_a = V_{a1} - V_{a2} \quad (3)$$

To assure that the comparator will always switch fully to V_{CC} and not be pulled down by the load the resistors values should be chosen as follow:

$$R_{PULL\text{-}UP} << R_{LOAD} \quad (4)$$

$$\text{and } R_1 > R_{PULL\text{-}UP}. \quad (5)$$

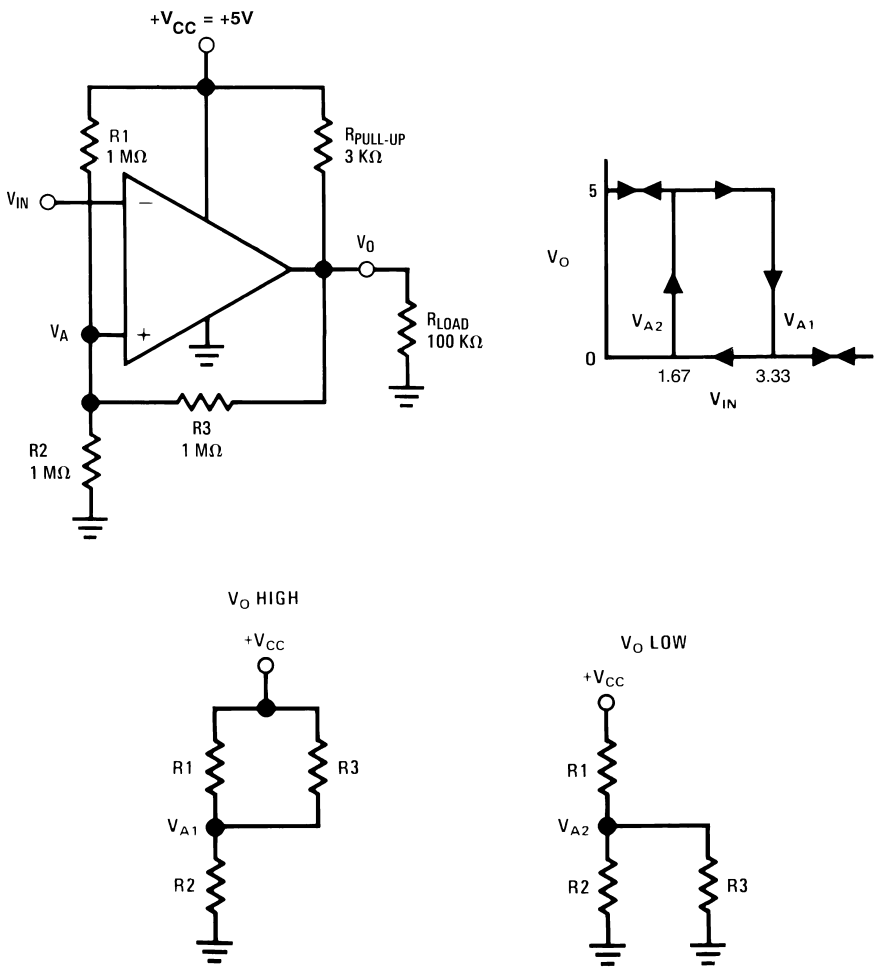

Figure 11. Inverting Comparator With Hysteresis

8.1.2.1.1 Non-inverting Comparator With Hysteresis

Non-inverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{ref}) at the inverting input. When V_{in} is low, the output is also low. For the output to switch from low to high, V_{in} must rise up to V_{in1} where V_{in1} is calculated by:

$$V_{in1} = \frac{V_{ref}(R_1 + R_2)}{R_2} \quad (6)$$

When V_{in} is high, the output is also high. To make the comparator switch back to its low state, V_{in} must equal V_{ref} before V_A will again equal V_{ref}. V_{in} can be calculated by:

$$V_{in2} = \frac{V_{ref}(R_1 + R_2) - V_{CC} R_1}{R_2} \quad (7)$$

The hysteresis of this circuit is the difference between V_{in1} and V_{in2}.

Application Information (continued)

$$\Delta V_{in} = V_{CC}R_1/R_2 \quad (8)$$

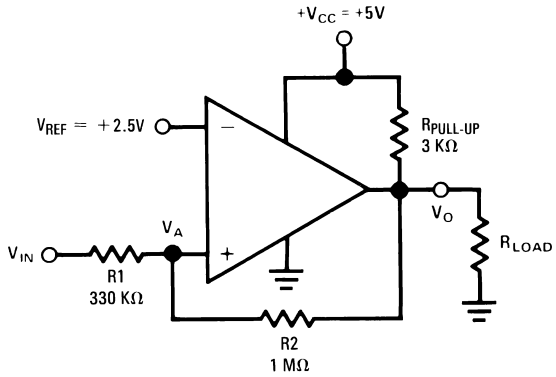

Figure 12. Noninverting Comparator With Hystersis

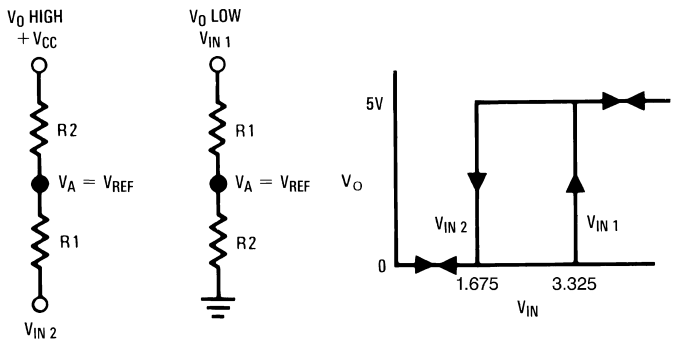

Figure 13. Hysteresis Threshold Points

8.1.3 ORing the Output

By the inherit nature of an open-collector comparator, the outputs of several comparators can be tied together with a shared pull-up resistor to V_{CC}. If one or more of the comparators outputs goes low, the output V_O will go low.

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Application Information (continued)

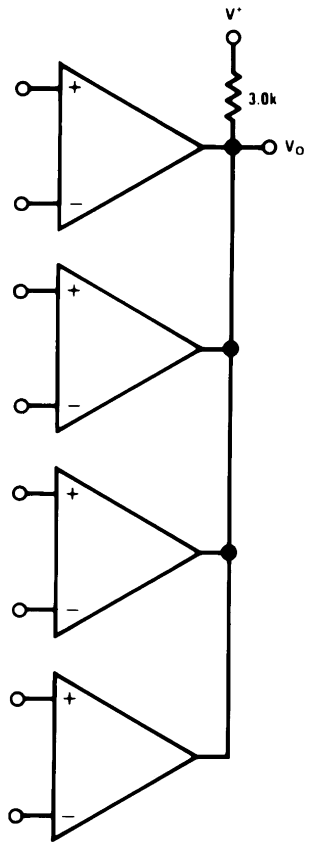

Figure 14. ORing the Outputs

8.1.4 Driving CMOS and TTL

The output of the comparator is capable of driving CMOS and TTL Logic circuits. The pull-up resistor may be pulled-up to any voltage equal to, or less than the supply voltage on V+. However, it must not be pulled-up to a voltage higher than V+.

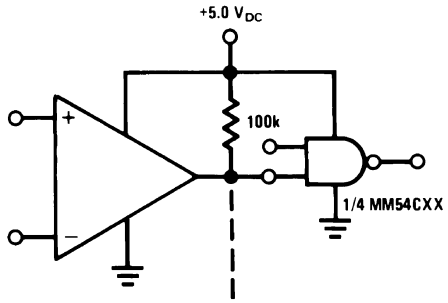

Figure 15. Driving CMOS

Application Information (continued)

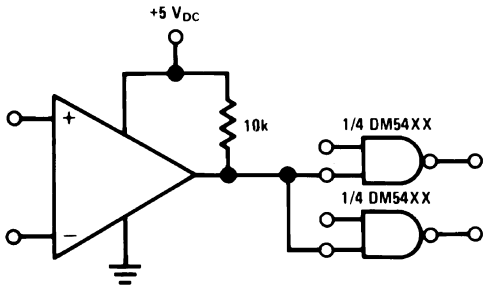

Figure 16. Driving TTL

8.1.5 AND Gates

The comparator can be used as three input AND gate. The operation of the gate is as follows:

The resistor divider at the inverting input establishes a reference voltage at that node. The non-inverting input is the sum of the voltages at the inputs divided by the voltage dividers. The output will go high only when all three inputs are high, casing the voltage at the non-inverting input to go above that at inverting input. The circuit values shown work for a 0 equal to ground and a 1 equal to 5 V.

The resistor values can be altered if different logic levels are desired. If more inputs are required, diodes are recommended to improve the voltage margin when all but one of the inputs are high.

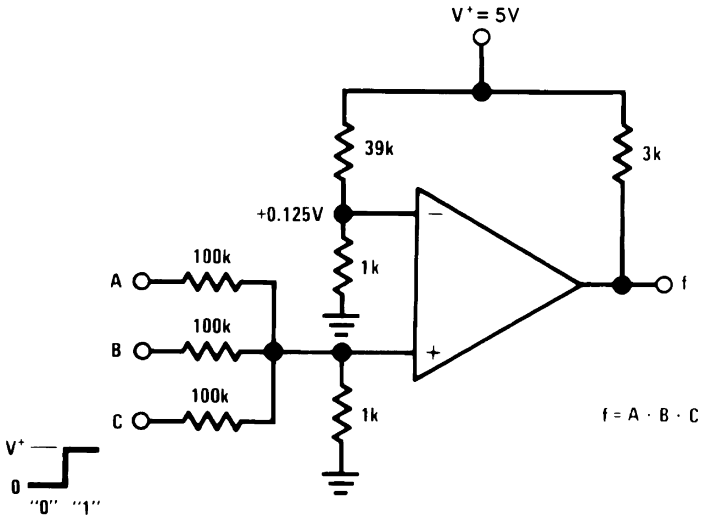

Figure 17. AND Gate

8.1.6 OR Gates

A three input OR gate is achieved from the basic AND gate simply by increasing the resistor value connected from the inverting input to V_{CC}, thereby reducing the reference voltage.

A logic 1 at any of the inputs will produce a logic 1 at the output.

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Application Information (continued)

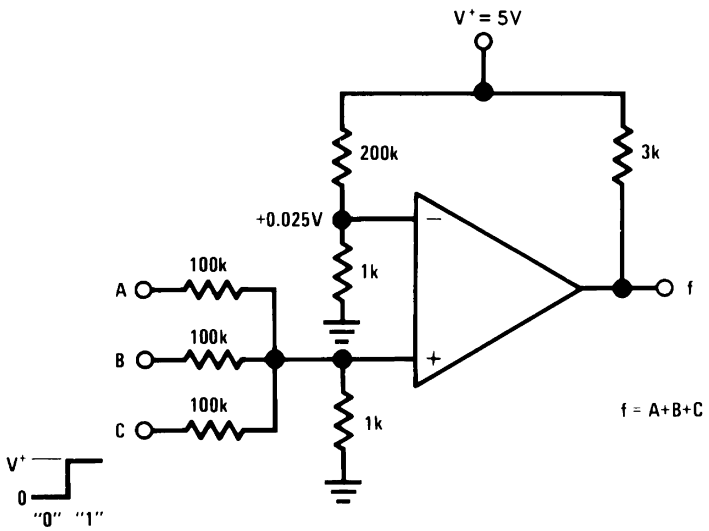

Figure 18. OR Gate

8.1.7 Large Fan-In Gate

Extra logic inputs may be added by ORing the input with multiple diodes.

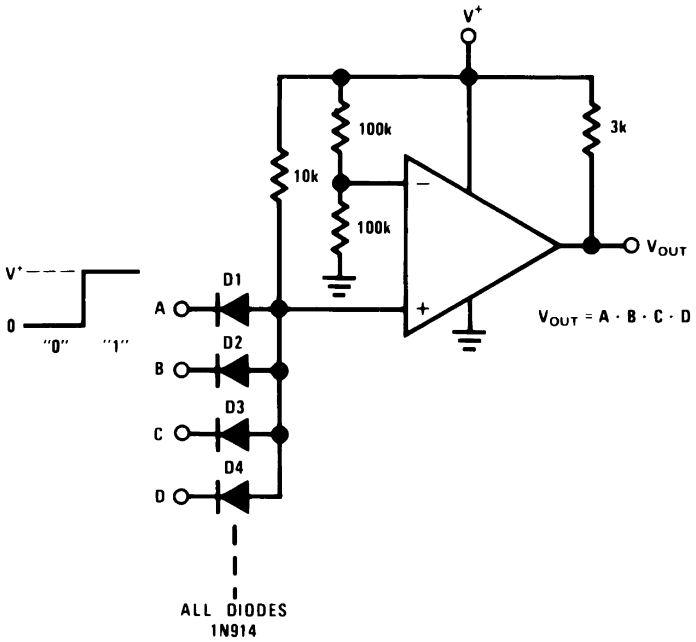

Figure 19. Large Fan-In and Gate

8.2 Typical Applications

8.2.1 Squarewave Oscillator

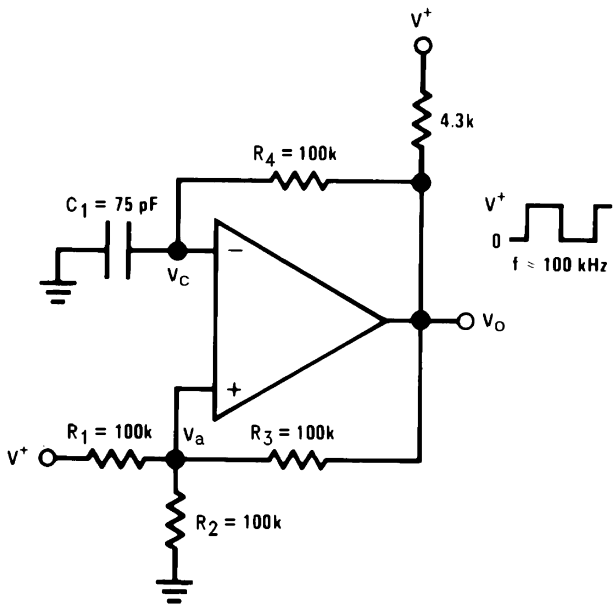

Figure 20. Squarewave Oscillator

8.2.1.1 Design Requirements

Comparators are ideal for oscillator applications. This square wave generator uses the minimum number of components. The output frequency is set by the RC time constant of the capacitor C_1 and the resistor in the negative feedback R_4. The maximum frequency is limited only by the large signal propagation delay of the comparator in addition to any capacitive loading at the output, which would degrade the output slew rate.

8.2.1.2 Detailed Design Procedure

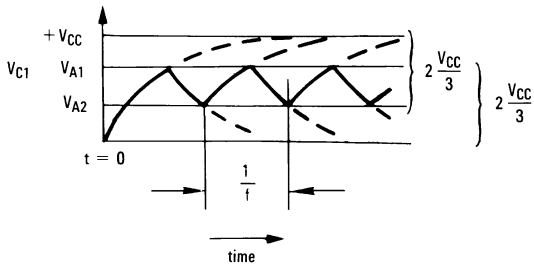

Figure 21. Squarewave Oscillator Timing Thresholds

To analyze the circuit, assume that the output is initially high. For this to be true, the voltage at the inverting input V_c has to be less than the voltage at the non-inverting input V_a. For V_c to be low, the capacitor C_1 has to be discharged and will charge up through the negative feedback resistor R_4. When it has charged up to value equal to the voltage at the positive input V_{a1}, the comparator output will switch.

V_{a1} will be given by:

$$V_{a1} = \frac{V_{CC} R_2}{R_2 + (R_1 // R_2)} \tag{9}$$

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Typical Applications (continued)

If:

$$R_1 = R_2 = R_3 \tag{10}$$

Then:

$$V_{a1} = 2V_{CC}/3 \tag{11}$$

When the output switches to ground, the value of V_a is reduced by the hysteresis network to a value given by:

$$V_{a2} = V_{CC}/3 \tag{12}$$

Capacitor C_1 must now discharge through R_4 towards ground. The output will return to its high state when the voltage across the capacitor has discharged to a value equal to V_{a2}.

For the circuit shown, the period for one cycle of oscillation will be twice the time it takes for a single RC circuit to charge up to one half of its final value. The time to charge the capacitor can be calculated from:

$$V_C = V_{max} \; e^{\frac{-t}{RC}} \tag{13}$$

Where V_{max} is the max applied potential across the capacitor = $(2V_{CC}/3)$

and $V_C = Vmax/2 = V_{CC}/3$

One period will be given by:

$$1/freq = 2t \tag{14}$$

or calculating the exponential gives:

$$1/freq = 2(0.694)\, R_4\, C_1 \tag{15}$$

Resistors R_3 and R_4 must be at least two times larger than R_5 to ensure that V_O will go all the way up to V_{CC} in the high state. The frequency stability of this circuit should strictly be a function of the external components.

8.2.1.3 Application Curve

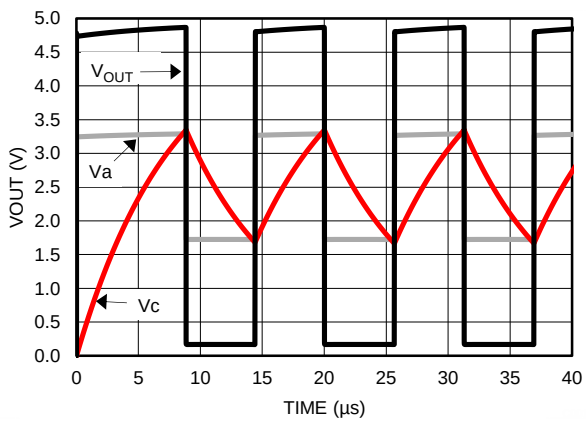

Figure 22. Waveforms for Circuit in *Typical Applications*

Typical Applications (continued)

8.2.2 Crystal Controlled Oscillator

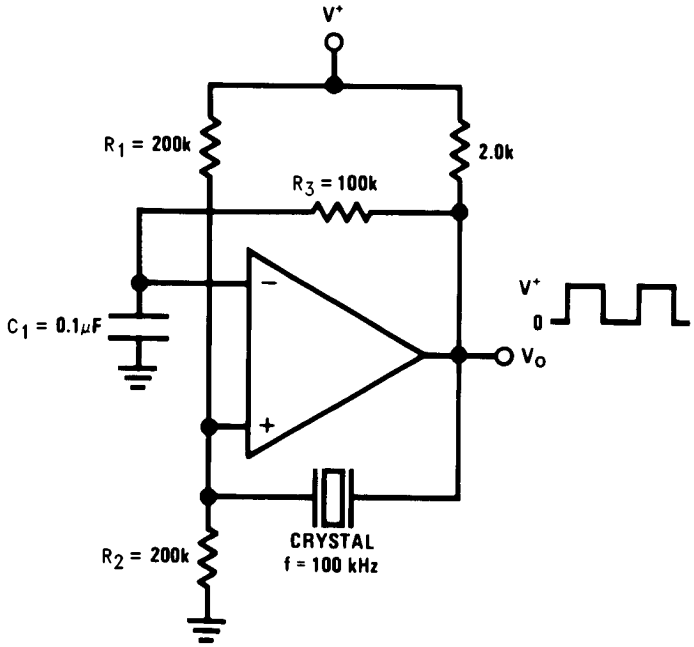

Figure 23. Crystal Controlled Oscillator

A simple yet very stable oscillator that generates a clock for slower digital systems can be obtained by using a resonator as the feedback element. It is similar to the squarewave oscillator, except that the positive feedback is obtained through a quartz crystal. The circuit oscillates when the transmission through the crystal is at a maximum, so the crystal in its series-resonant mode.

The value of R_1 and R_2 are equal so that the comparator will switch symmetrically about $+V_{CC}/2$. The RC constant of R_3 and C_1 is set to be several times greater than the period of the oscillating frequency, insuring a 50% duty cycle by maintaining a DC voltage at the inverting input equal to the absolute average of the output waveform.

When specifying the crystal, be sure to order series resonant with the desired temperature coefficient.

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Typical Applications (continued)

8.2.3 Pulse Generator With Variable Duty Cycle

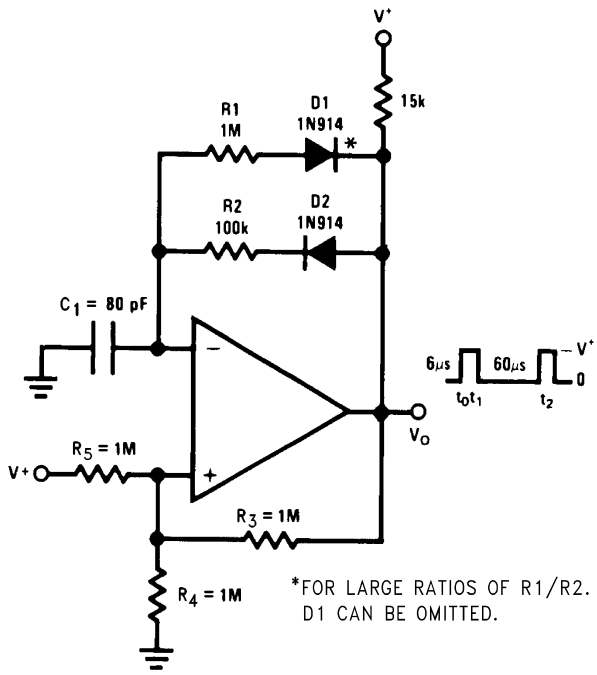

Figure 24. Pulse Generator With Variable Duty Cycle

The pulse generator with variable duty cycle is just a minor modification of the basic square wave generator. Providing a separate charge and discharge path for capacitor C_1generates a variable duty cycle. One path, through R_2 and D_2 will charge the capacitor and set the pulse width (t_1). The other path, R_1 and D_1 will discharge the capacitor and set the time between pulses (t_2).

By varying resistor R_1, the time between pulses of the generator can be changed without changing the pulse width. Similarly, by varying R_2, the pulse width will be altered without affecting the time between pulses. Both controls will change the frequency of the generator. The pulse width and time between pulses can be found from:

$$V_1 = V_{max}\left(1 - e^{-t_1/R_4C_1}\right) \quad \text{rise time}$$

$$V_1 = V_{max} \quad e^{-t_2/R_5C_1} \quad \text{fall time}$$

Where

$$V_{max} = \frac{2\,V_{CC}}{3}$$

and

$$V_1 = \frac{V_{max}}{3} = \frac{V_{CC}}{3}$$

Which gives

$$\frac{1}{2} = e^{-t_1/R_4C_1}$$

t_2 is then given by:

$$\frac{1}{2} = e^{-t_2/R_5C_1} \tag{16}$$

Typical Applications (continued)

Solving these equations for t_1 and t_2

$$t_1 = R_4C_1\ln 2 \tag{17}$$

$$t_2 = R_5C_1\ln 2 \tag{18}$$

These terms will have a slight error due to the fact that V_{max} is not exactly equal to 2/3 V_{CC} but is actually reduced by the diode drop to:

$$V_{max} = \frac{2}{3}(V_{CC} - V_{BE}) \tag{19}$$

$$\frac{1}{2(1 - V_{BE})} = e^{-t_1/R_4C_1} \tag{20}$$

$$\frac{1}{2(1 - V_{BE})} = e^{-t_2/R_5C_1} \tag{21}$$

8.2.4 Positive Peak Detector

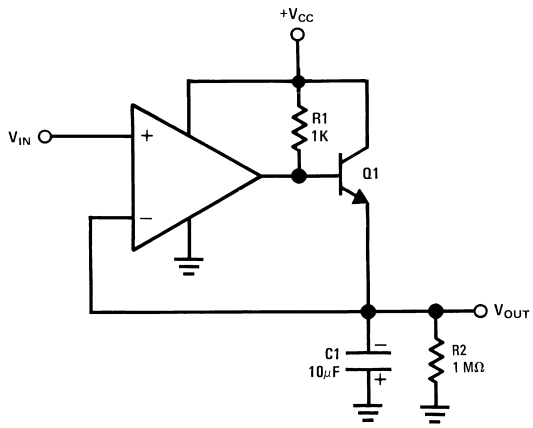

Figure 25. Positive Peak Detector

Positive peak detector is basically the comparator operated as a unit gain follower with a large holding capacitor from the output to ground. Additional transistor is added to the output to provide a low impedance current source. When the output of the comparator goes high, current is passed through the transistor to charge up the capacitor. The only discharge path will be the 1-MΩ resistor shunting C1 and any load that is connected to the output. The decay time can be altered simply by changing the 1-MΩ resistor. The output should be used through a high impedance follower to a avoid loading the output of the peak detector.

8.2.5 Negative Peak Detector

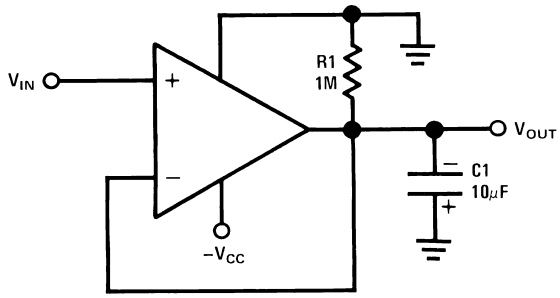

Figure 26. Negative Peak Detector

For the negative detector, the output transistor of the comparator acts as a low impedance current sink. The only discharge path will be the 1-MΩ resistor and any load impedance used. Decay time is changed by varying the 1-MΩ resistor.

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9 Power Supply Recommendations

The TLV170x is specified for operation from 2.2 V to 36 V (±1.1 to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 5.5 V can permanently damage the device; see the *Specifications* section.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines* section

10 Layout

10.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, the following layout guidelines should be maintained:

- Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the comparator
- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to SLOA089, *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the topside ground plane between the output and inputs.

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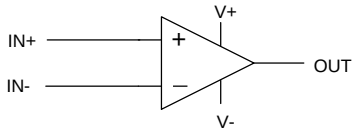
10.2 Layout Example



(Schematic Representation)

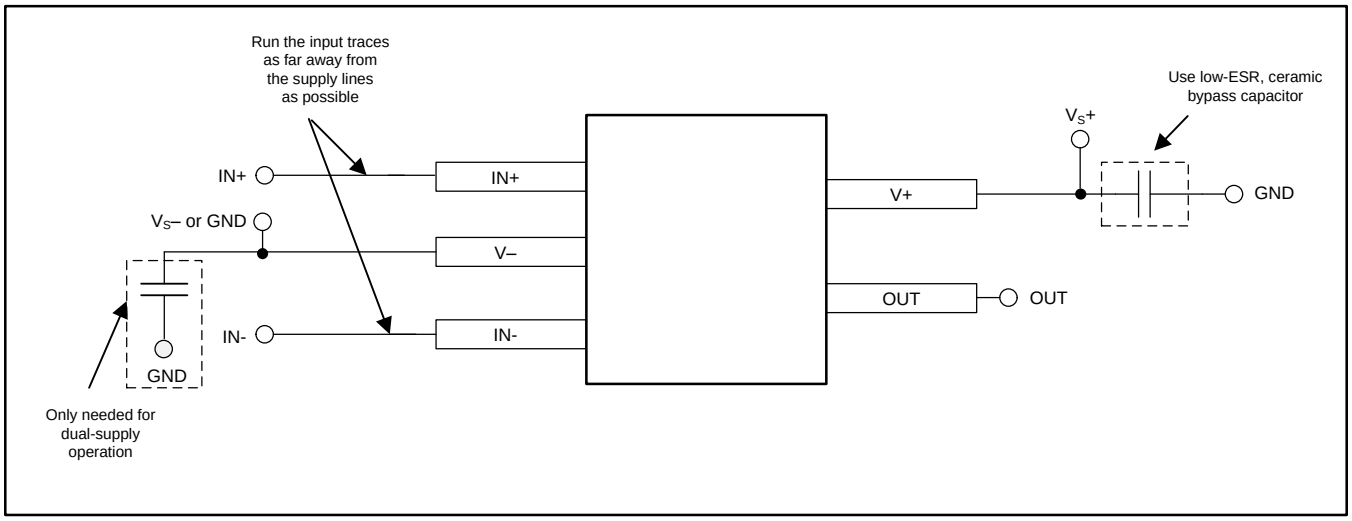


Figure 27. Comparator Board Layout

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LMV331-N PSPICE Model, SNOM073

LMV339-N PSPICE Model, SNOM074

LMV393-N PSPICE Model, SNOM059

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm

TI Universal Operational Amplifier Evaluation Module, http://www.ti.com/tool/opampevm

11.2 Documentation Support

11.2.1 Related Documentation

AN-74 - A Quad of Independently Functioning Comparators, SNOA654

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV331-N	Click here	Click here	Click here	Click here	Click here
LMV339-N	Click here	Click here	Click here	Click here	Click here
LMV393-N	Click here	Click here	Click here	Click here	Click here

11.4 Trademarks

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV331M5	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	C12	
LMV331M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C12	Samples
LMV331M5X	LIFEBUY	SOT-23	DBV	5	3000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	C12	
LMV331M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C12	Samples
LMV331M7	LIFEBUY	SC70	DCK	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	C13	
LMV331M7/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C13	Samples
LMV331M7X/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	C13	Samples
LMV339M/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMV339M	Samples
LMV339MT	LIFEBUY	TSSOP	PW	14	94	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LMV339 MT	
LMV339MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMV339 MT	Samples
LMV339MTX	LIFEBUY	TSSOP	PW	14	2500	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	LMV339 MT	
LMV339MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMV339 MT	Samples
LMV339MX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMV339M	Samples
LMV393M	LIFEBUY	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LMV 393M	
LMV393M/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMV 393M	Samples
LMV393MM	LIFEBUY	VSSOP	DGK	8	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	V393	
LMV393MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	V393	Samples
LMV393MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	V393	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV393MX	LIFEBUY	SOIC	D	8	2500	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LMV 393M	
LMV393MX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMV 393M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV331-N, LMV393-N :

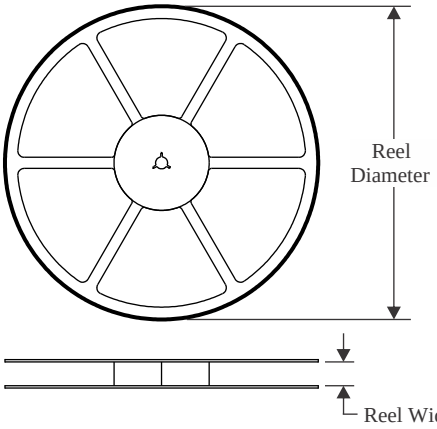
- Automotive : LMV331-Q1, LMV393-Q1

NOTE: Qualified Version Definitions:

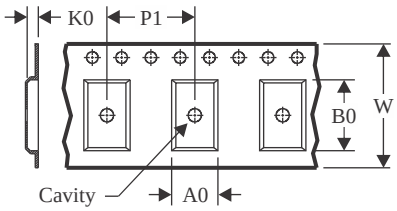
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

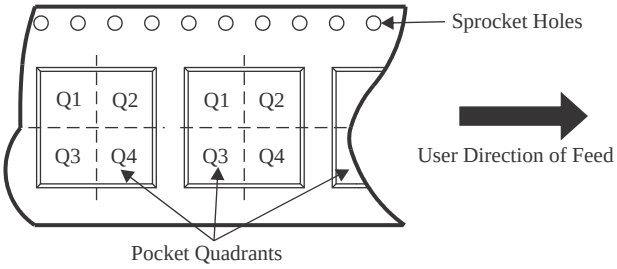


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

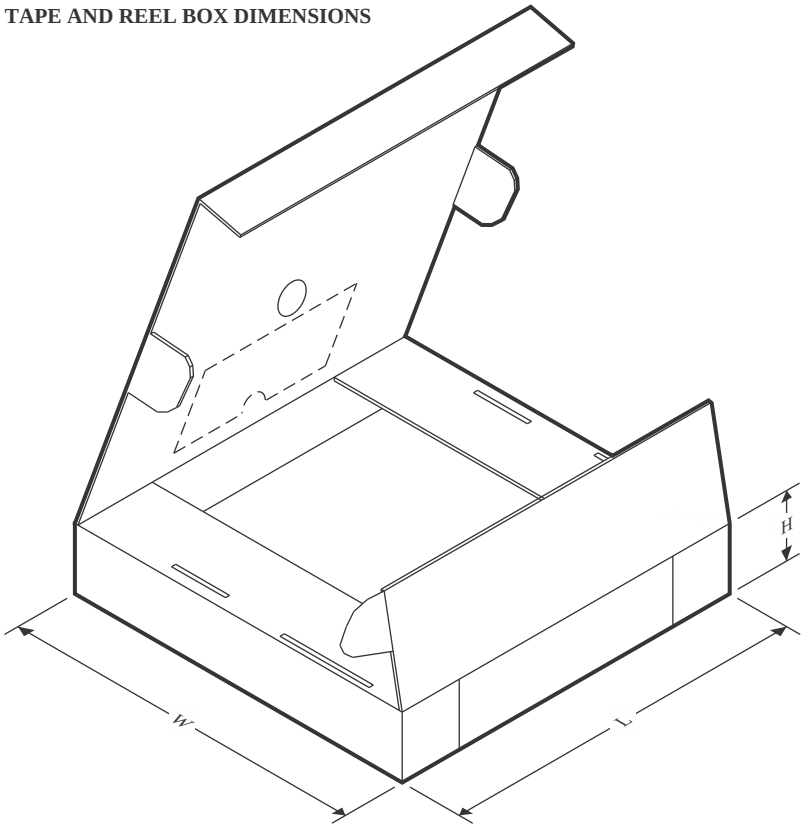
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV331M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV331M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV331M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV331M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV331M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV331M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV331M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV339MTX	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMV339MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMV339MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV393MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV393MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV393MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV393MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV393MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

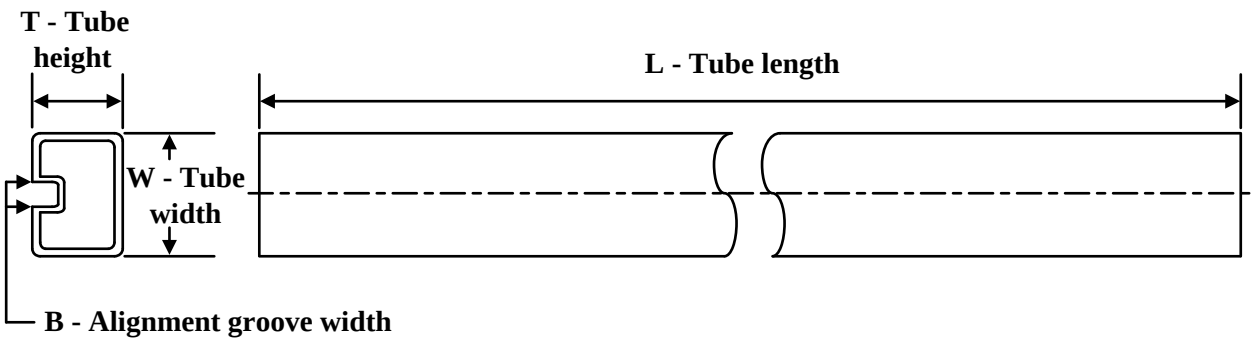
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

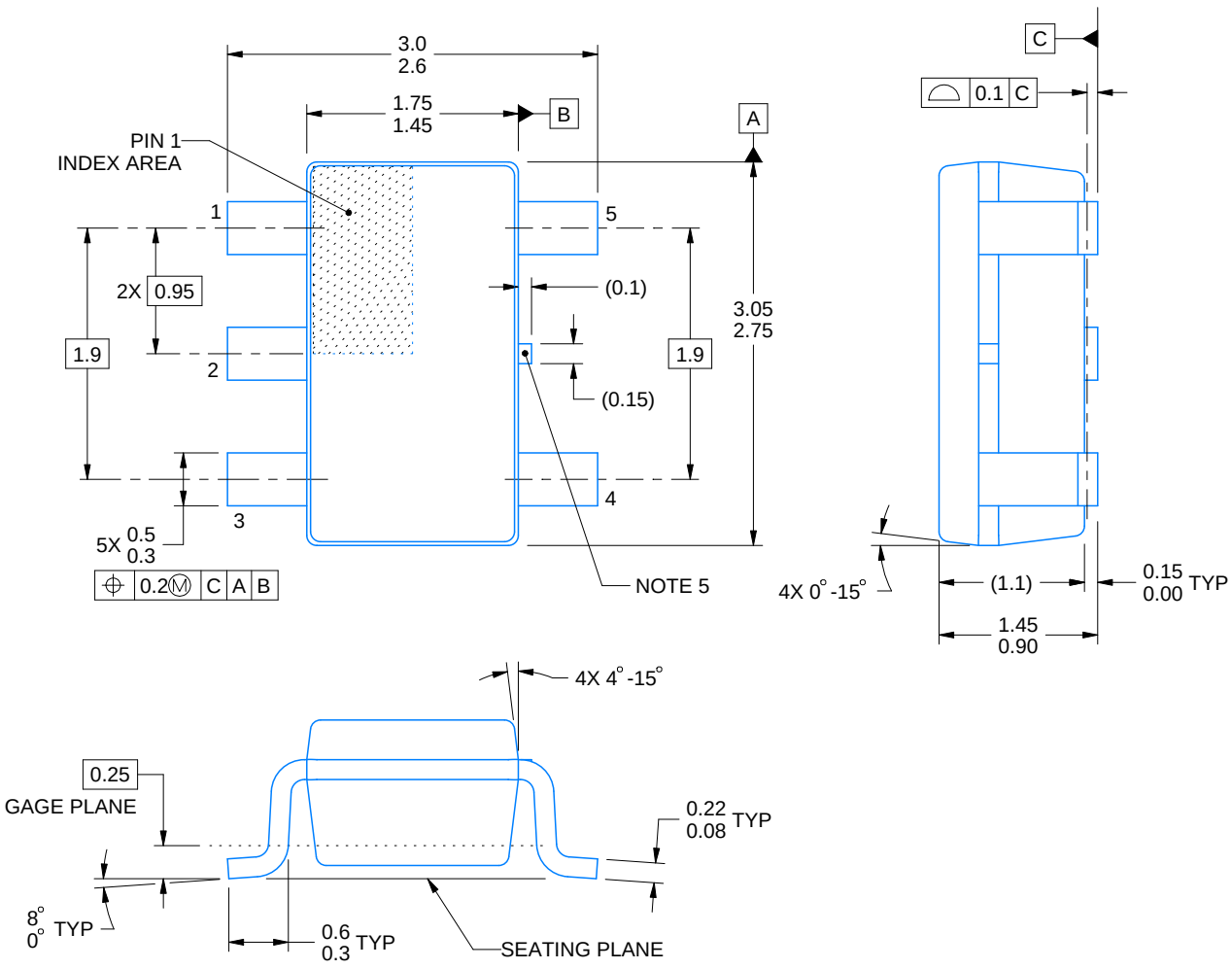
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV331M5	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV331M5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV331M5X	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV331M5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV331M7	SC70	DCK	5	1000	208.0	191.0	35.0
LMV331M7/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMV331M7X/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0
LMV339MTX	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV339MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV339MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMV393MM	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV393MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV393MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV393MX	SOIC	D	8	2500	367.0	367.0	35.0
LMV393MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

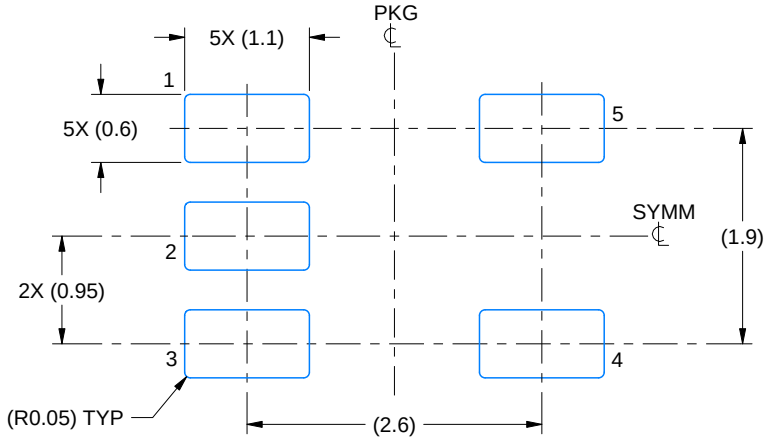
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMV339M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMV339MT	PW	TSSOP	14	94	495	8	2514.6	4.06
LMV339MT	PW	TSSOP	14	94	495	8	2514.6	4.06
LMV339MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LMV393M	D	SOIC	8	95	495	8	4064	3.05
LMV393M	D	SOIC	8	95	495	8	4064	3.05
LMV393M/NOPB	D	SOIC	8	95	495	8	4064	3.05



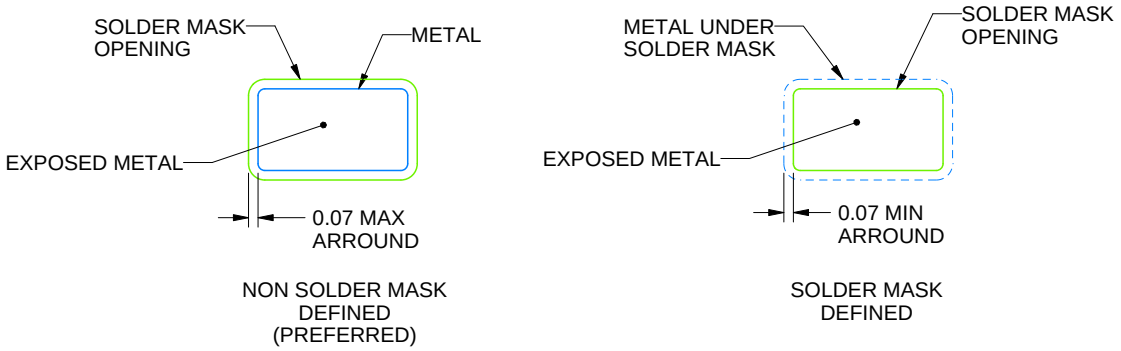
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

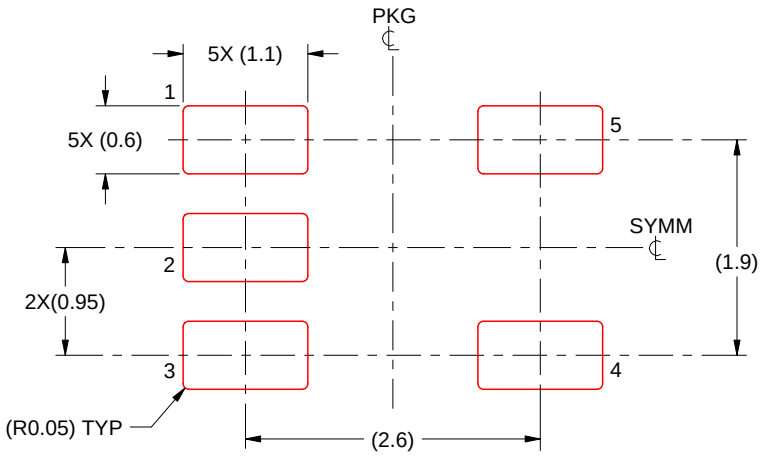


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

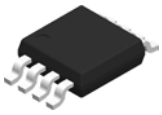
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

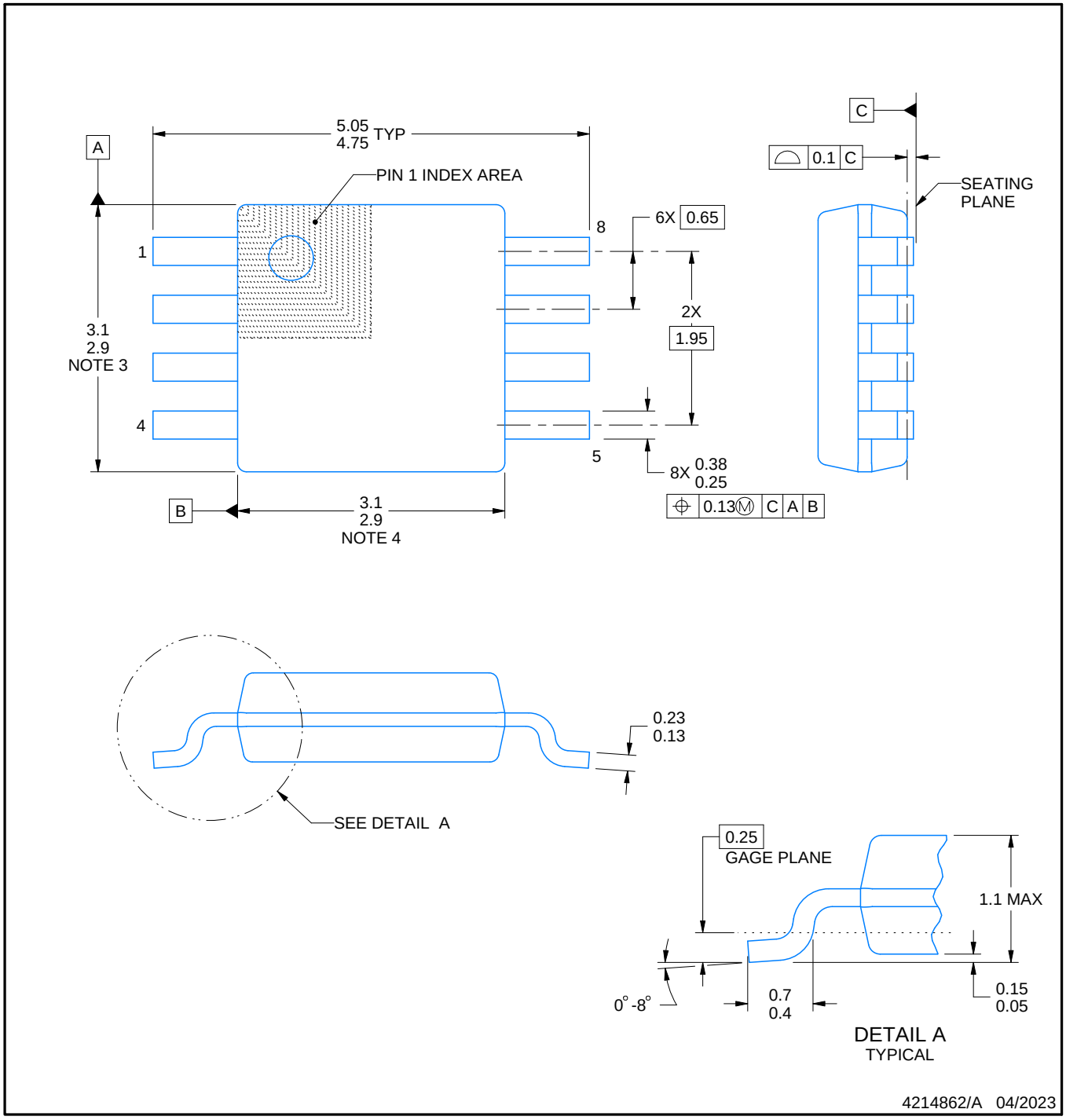
PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

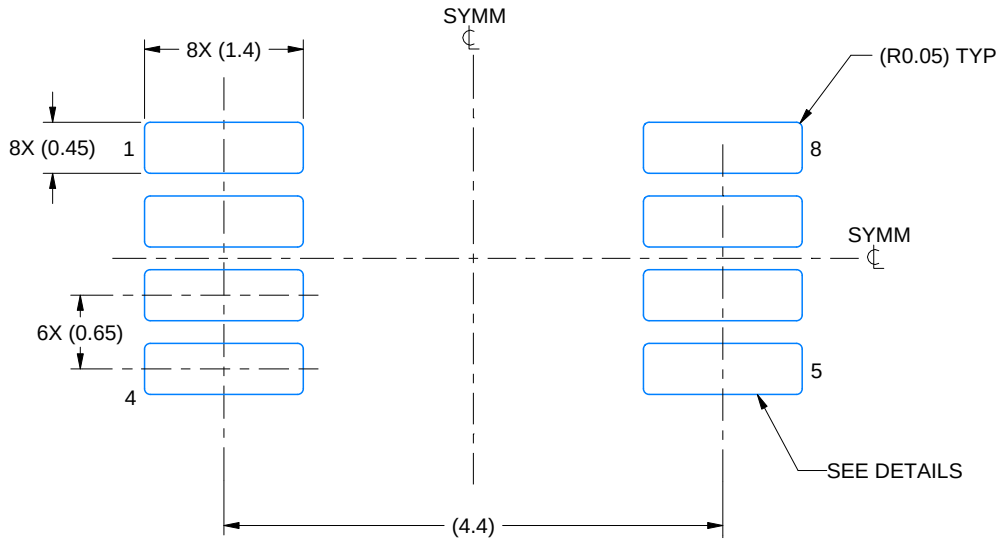
SMALL OUTLINE PACKAGE



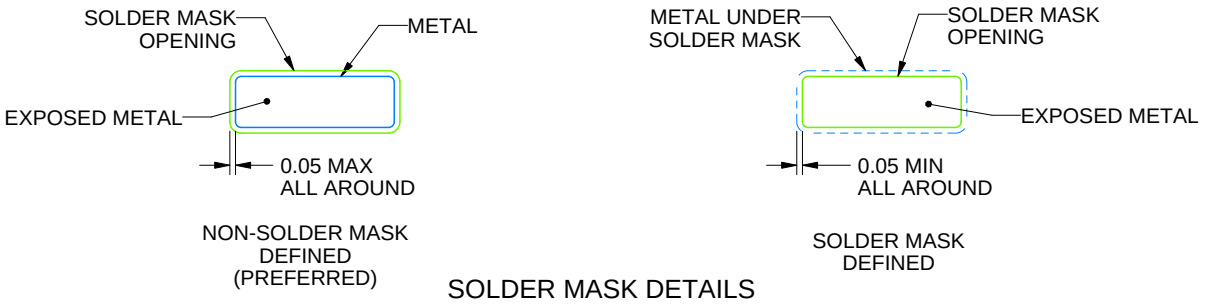
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

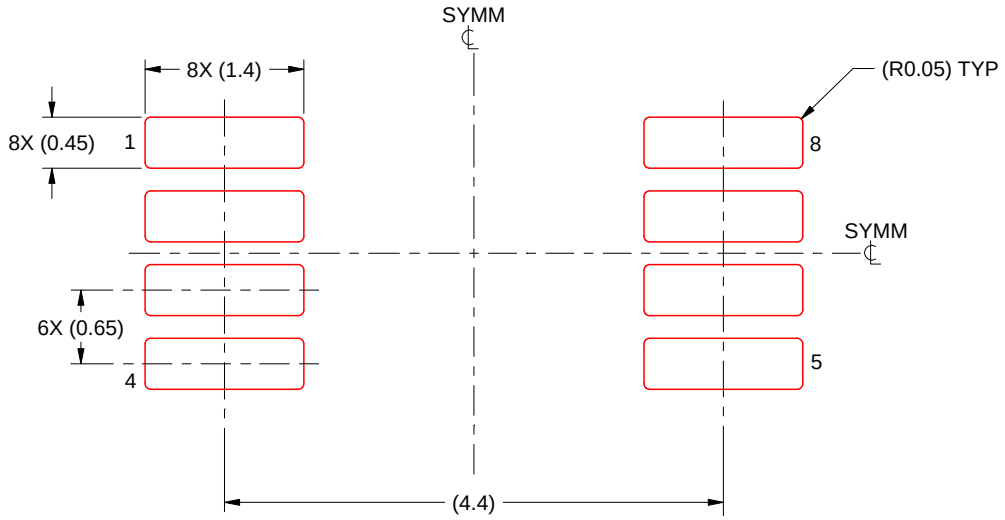


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

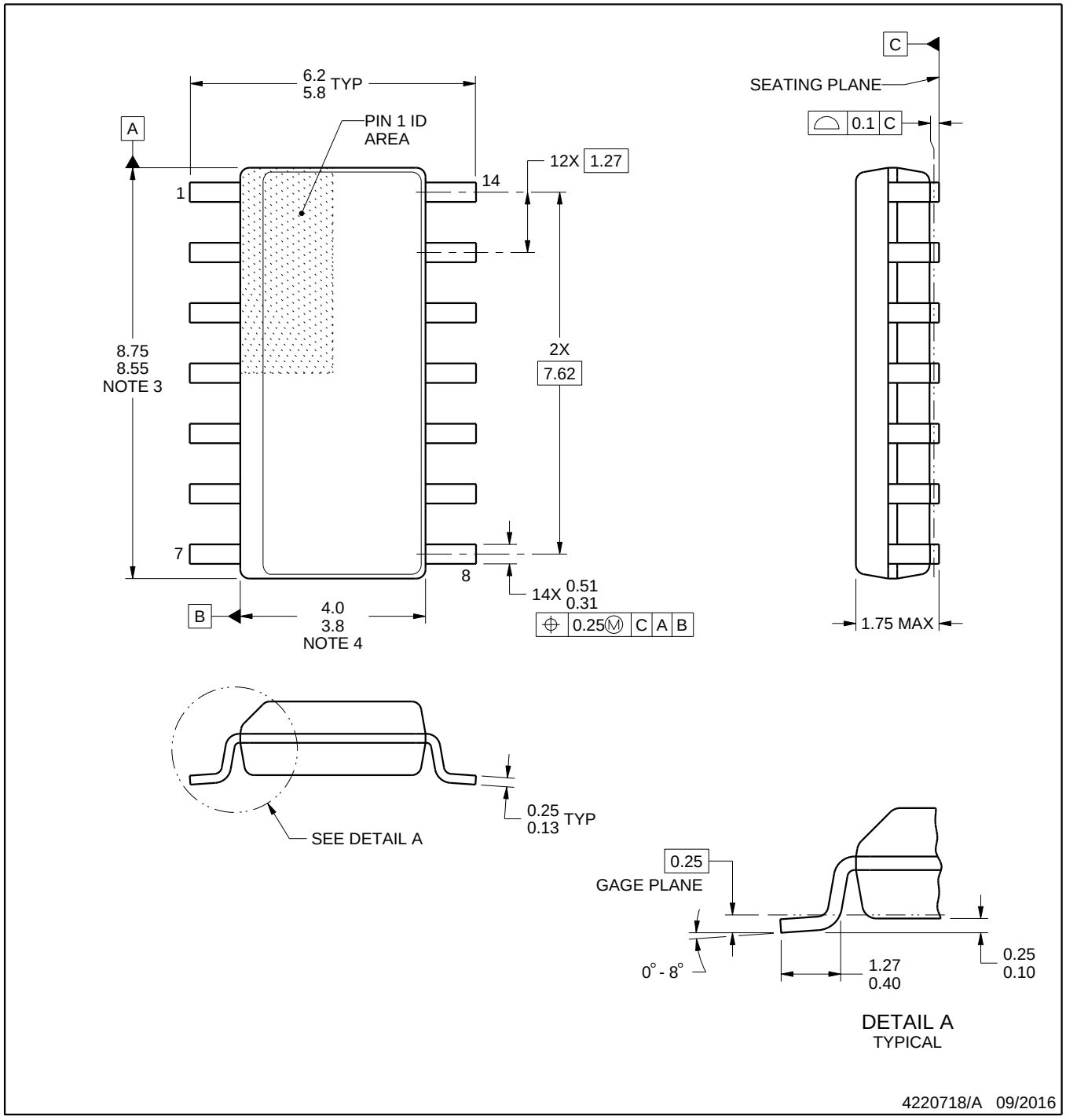


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

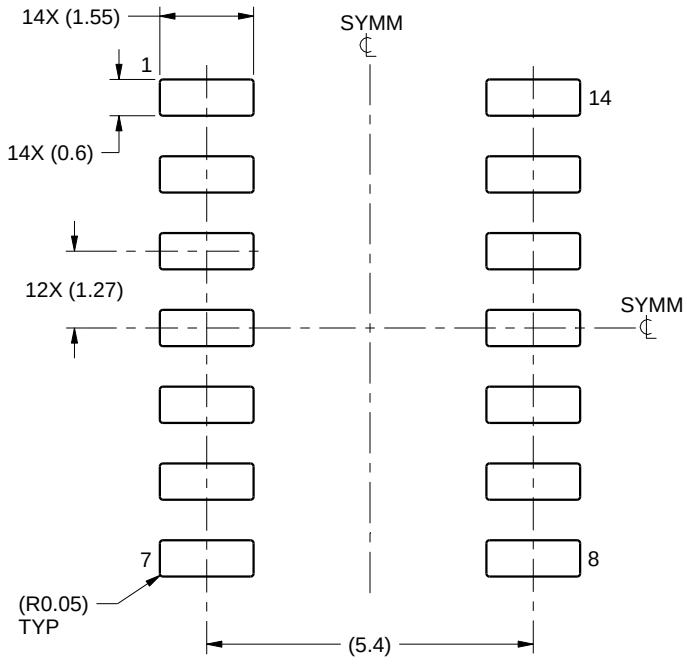
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

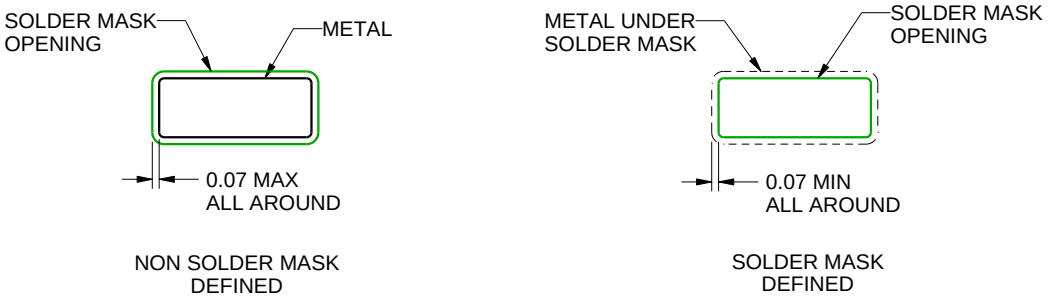


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

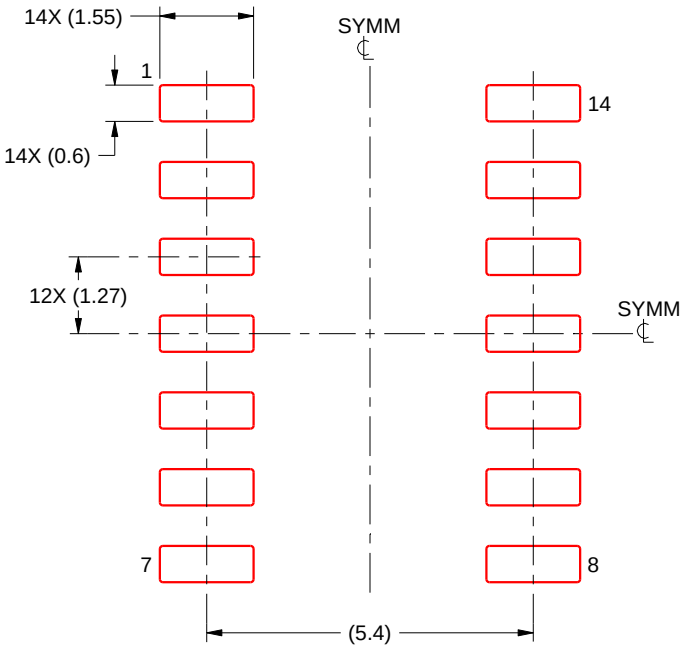


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

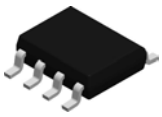


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

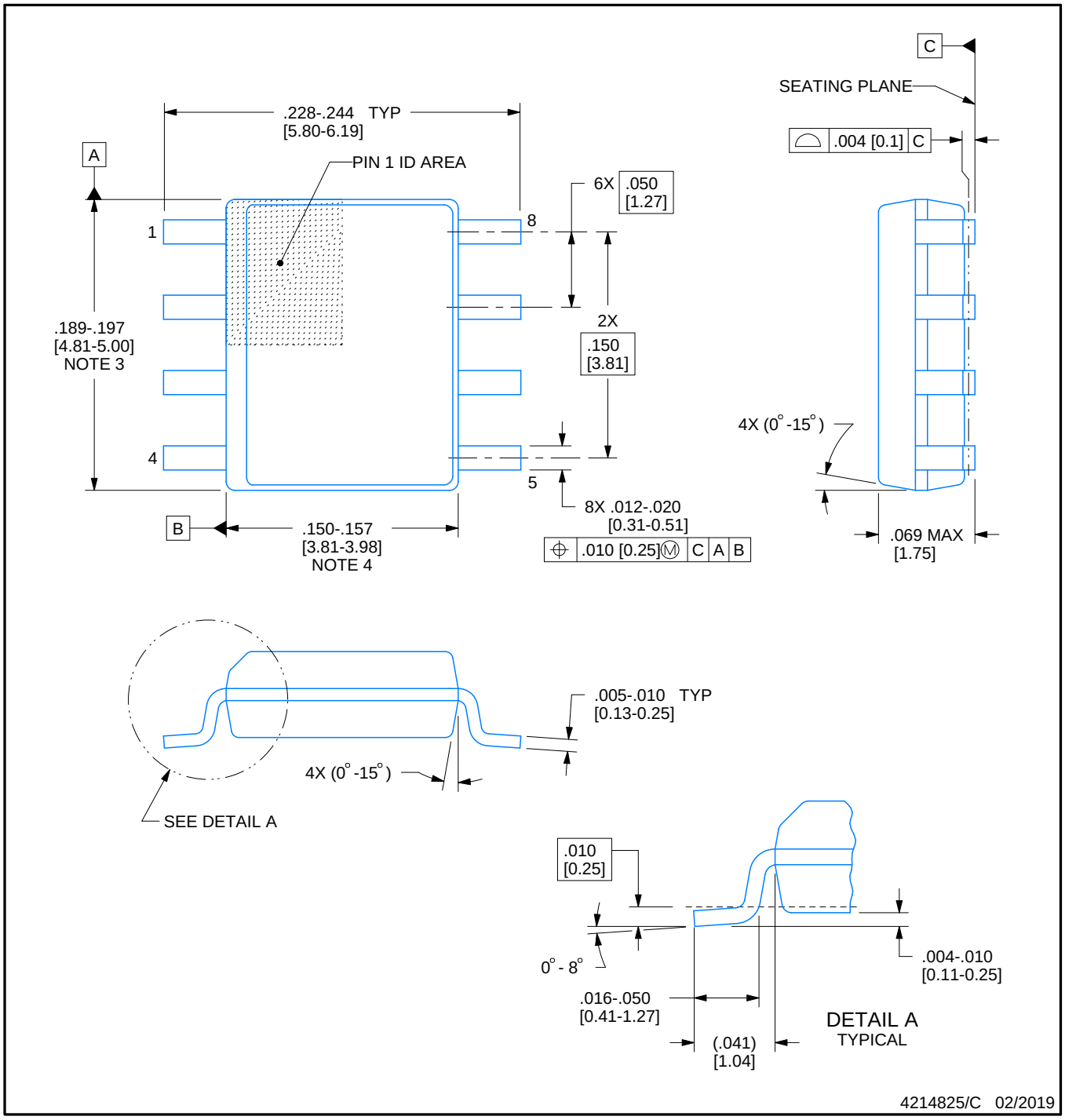


PACKAGE OUTLINE

D0008A

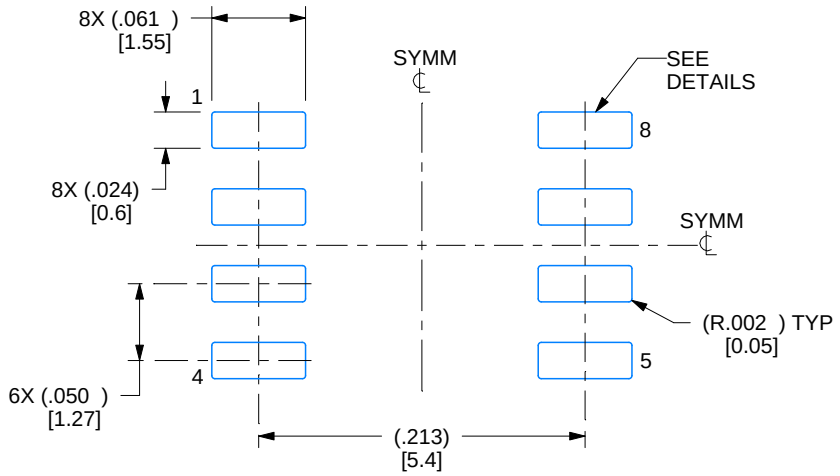
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

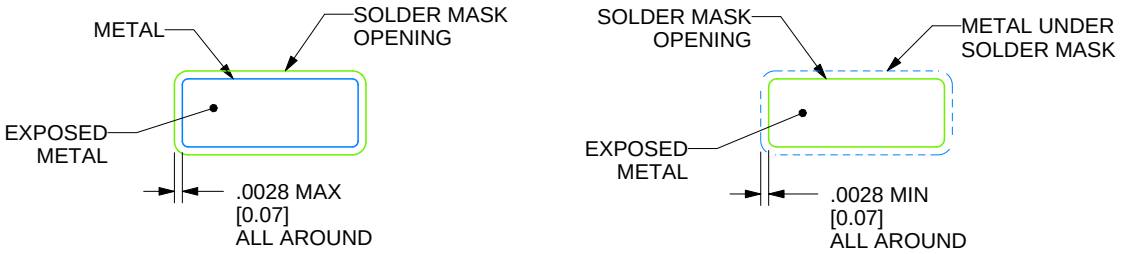


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

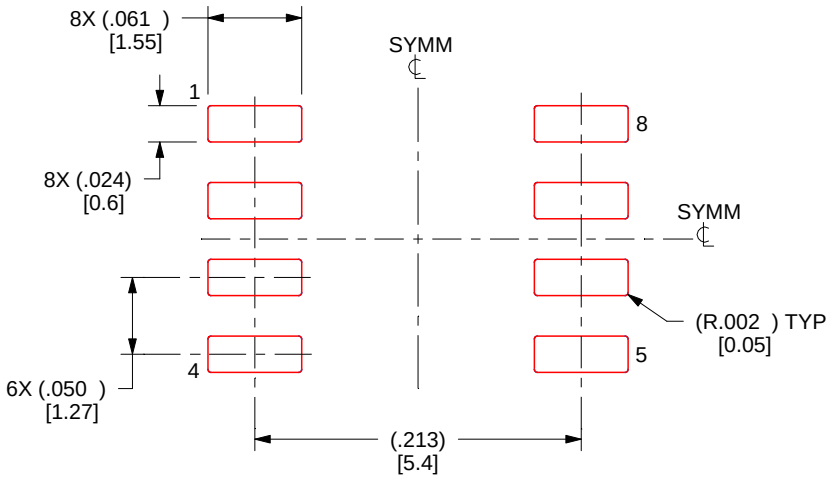


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

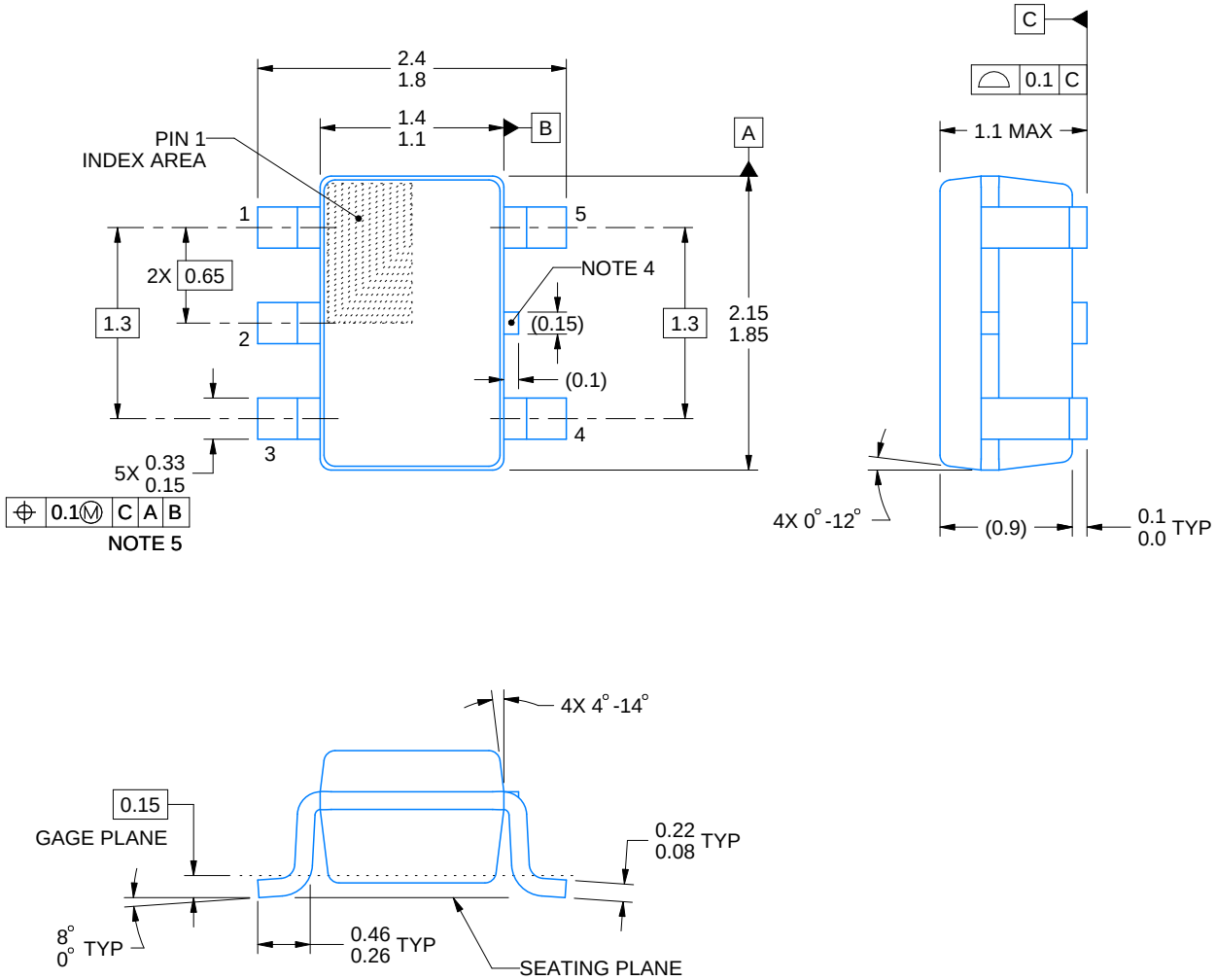


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

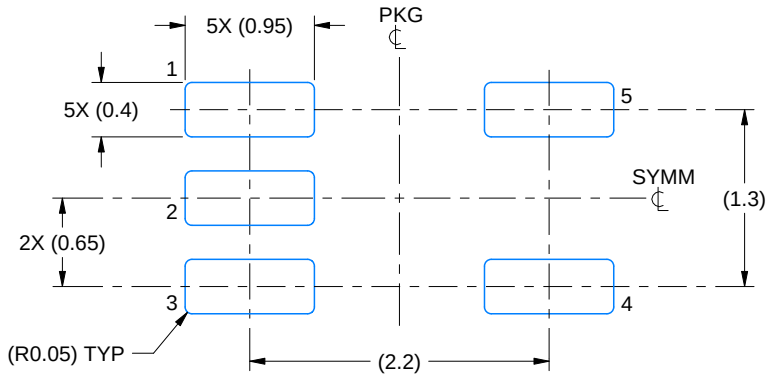
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



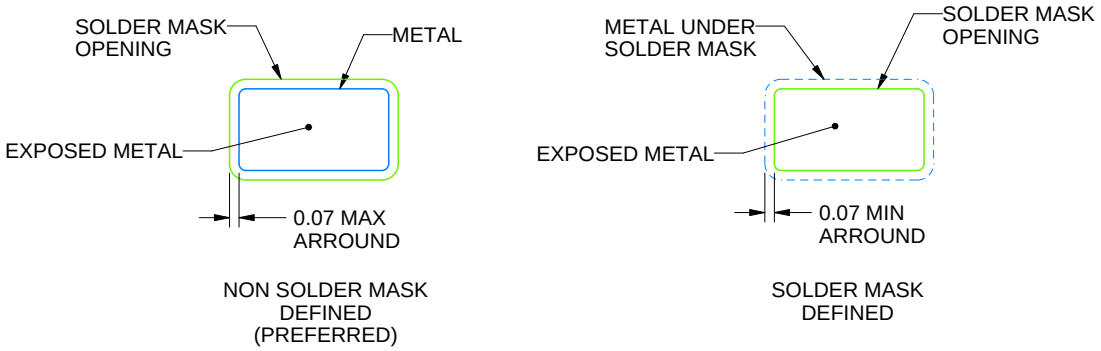
4214834/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

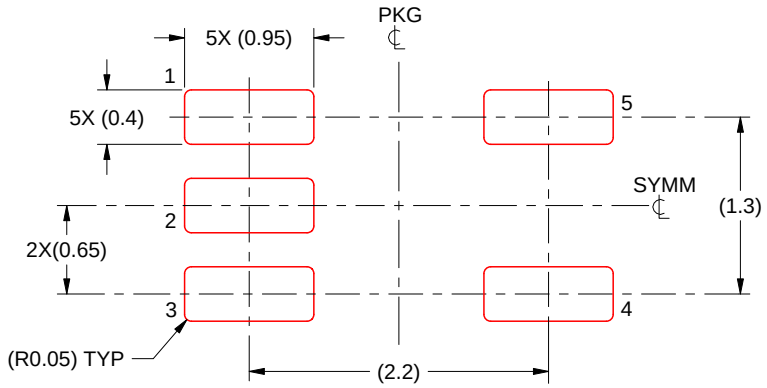


SOLDER MASK DETAILS

4214834/F 08/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



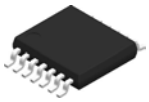
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/F 08/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

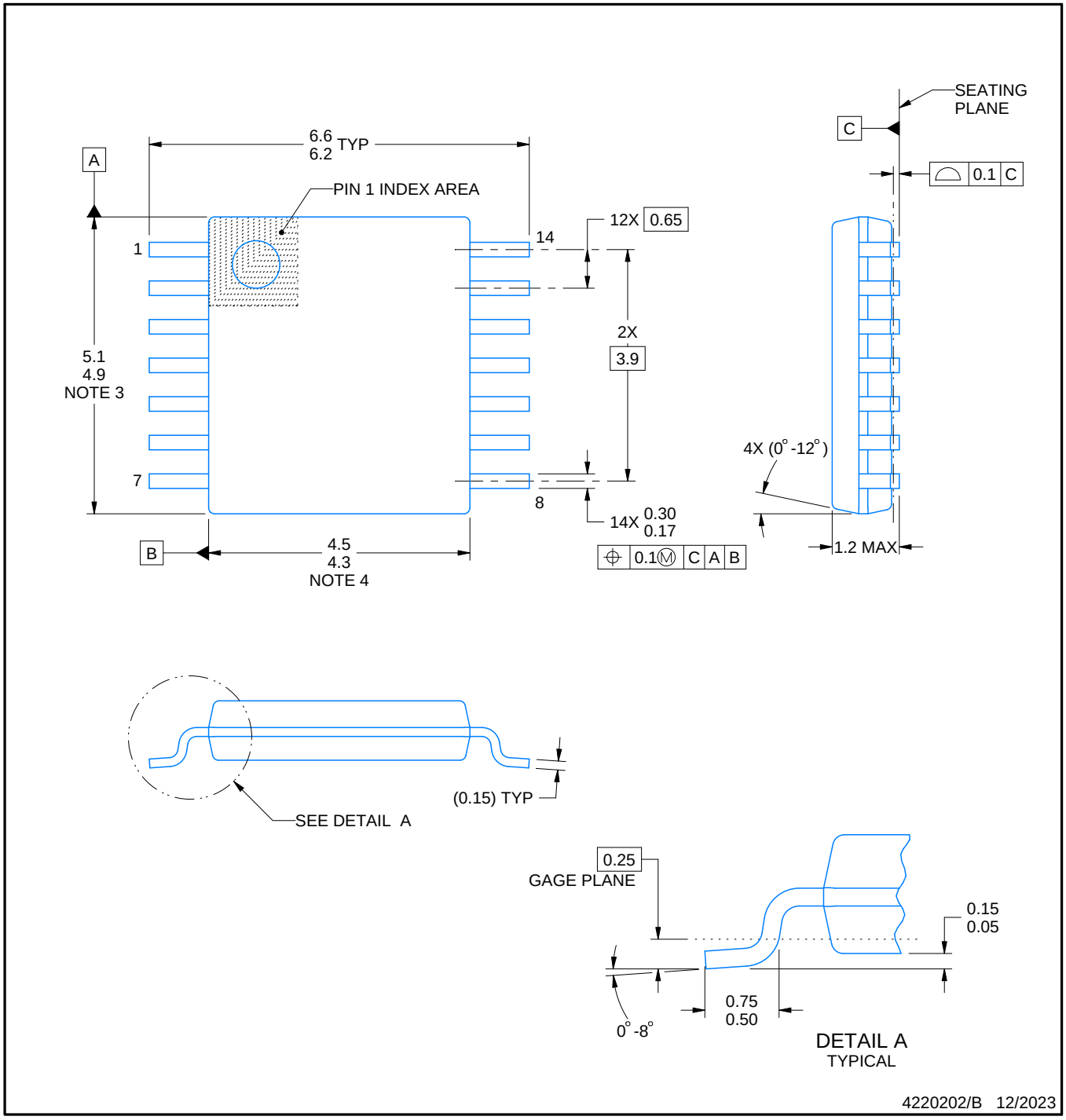
PW0014A



PACKAGE OUTLINE

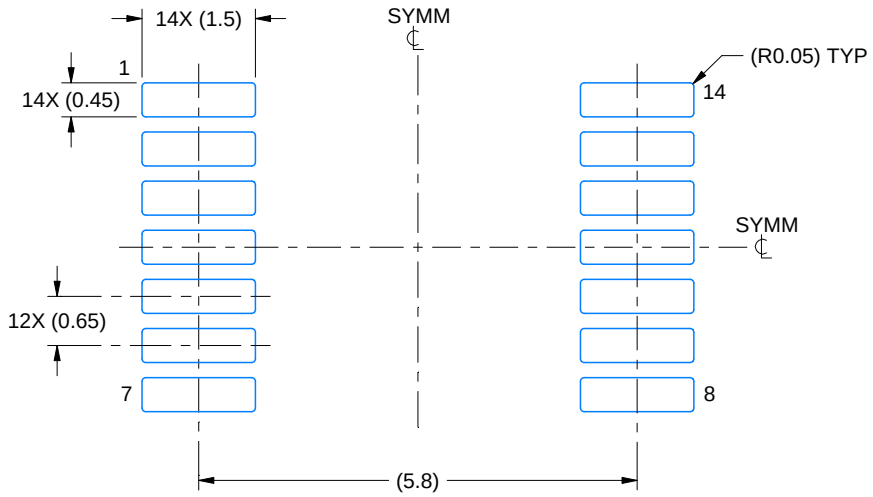
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

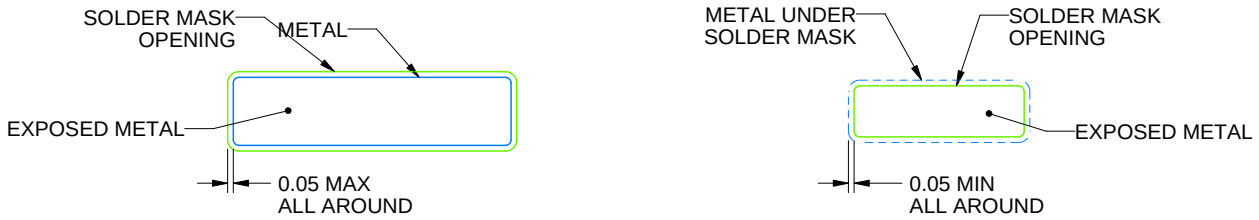


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

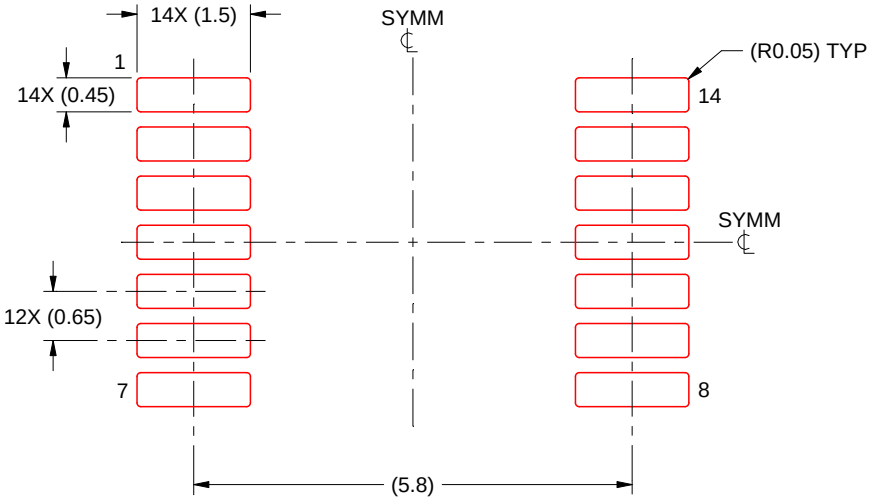
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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