LM8262 Dual RRIO, High Output Current and Unlimited Cap Load Op Amp in VSSOP

1 Features

(V_S = 5V, T_A = 25°C, Typical Values Unless Specified).

- GBWP 21MHz
- Wide Supply Voltage Range 2.5 V to 22 V
- Slew Rate 12V/µs
- Supply Current/channel 1.15 mA
- Cap Load Limit Unlimited
- Output Short Circuit Current +53mA/−75 mA
- +/−5% Settling Time 400ns (500 pF, 100 mV_{PP} step)
- Input Common Mode Voltage 0.3 V Beyond Rails
- Input Voltage Noise 15nV/$\sqrt{Hz}$
- Input Current Noise 1pA/$\sqrt{Hz}$
- THD+N < 0.05%

2 Applications

- TFT-LCD Flat Panel V_{COM} driver
- A/D Converter Buffer
- High Side/low Side Sensing
- Headphone Amplifier

3 Description

The LM8262 is a Rail-to-Rail input and output Op Amp which can operate with a wide supply voltage range. This device has high output current drive, greater than Rail-to-Rail input common mode voltage range, unlimited capacitive load drive capability, and provides tested and ensured high speed and slew rate. It is specifically designed to handle the requirements of flat panel TFT panel V_{COM} driver applications as well as being suitable for other low power and medium speed applications which require ease of use and enhanced performance over existing devices.

Greater than Rail-to-Rail input common mode voltage range with 50 dB of Common Mode Rejection allows high side and low side sensing for many applications without concern for exceeding the range and with no compromise in accuracy. In addition, most device parameters are insensitive to power supply variations. This design enhancement is yet another step in simplifying its usage. The output stage has low distortion (0.05% THD+N) and can supply a respectable amount of current (15 mA) with minimal headroom from either rail (300 mV).

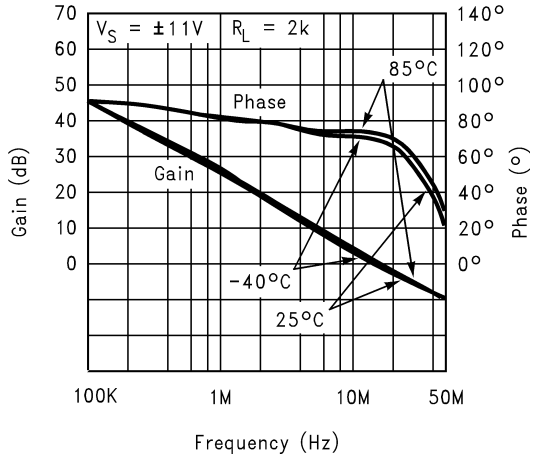
The LM8262 is offered in the space saving VSSOP package.

Device Information[1]

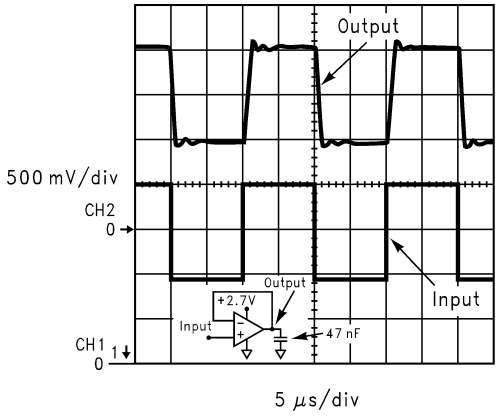
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM8262	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Gain/Phase vs. Frequency



Output Response with Heavy Capacitive Load



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (August 2014) to Revision G — **Page**

- Changed pin 5 From: -IN B To: +IN B Non-Inverting Input B in the *Pin Functions* table ... 3
- Changed pin 6 From: +IN B To: -IN B Inverting Input B in the *Pin Functions* table ... 3
- Moved "Storage temperature range" to the *Absolute Maximum Ratings* (1)(2) ... 4
- Changed *Handling Ratings* To: *ESD Ratings* ... 4

Changes from Revision E (April 2013) to Revision F — **Page**

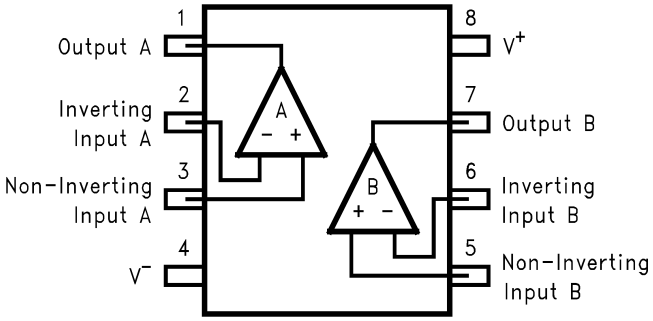
- Changed data sheet structure and organization. Added, updated, or renamed the following sections: Device and Documentation Support; Mechanical, Packaging, and Ordering Information ... 1
- Changed from "Junction Temperature Range" to "Operating Temperature Range" ... 4
- Deleted T_J = 25°C, ... 5
- Deleted T_J = 25°C, ... 6
- Deleted T_J = 25°C ... 7

Changes from Revision D (April 2013) to Revision E — **Page**

- Changed layout of National Data Sheet to TI format ... 10

5 Pin Configuration and Functions

8-Pin
VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUT A	O	Output A
2	-IN A	I	Inverting Input A
3	+IN A	I	Non-Inverting Input A
4	V-	I	Negative Supply
5	+IN B	I	Non-Inverting Input B
6	-IN B	I	Inverting Input B
7	OUT B	O	Output B
8	V+	I	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)

over operating free-air temperature range (unless otherwise noted) (3)

		MIN	MAX	UNIT
V_{IN} Differential			+/−10	V
Output Short Circuit Duration			See (4) (5)	
Supply Voltage (V^+ - V^-)			24	V
Voltage at Input/Output pins			V^+ +0.8, V^- −0.8	V
Junction Temperature (6)			+150	°C
Storage temperature range, T_{stg}		−65	+150	°C
Soldering Information:	Infrared or Convection (20 sec.)		235	°C
	Wave Soldering (10 sec.)		260	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(5) Output short circuit duration is infinite for $V_S \leq 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.
(6) The maximum power dissipation is a function of $T_J(max)$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(max) - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(2)	±2000	V
		Machine Model (MM)(3)	±200	

(1) Human Body Model, 1.5 kΩ in series with 100 pF. Machine Model, 0 Ω is series with 200 pF.
(2) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (V^+ - V^-)	2.5	22	V
Operating Temperature Range(1)	−40	+85	°C

(1) The maximum power dissipation is a function of $T_J(max)$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(max) - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.4 Thermal Information

THERMAL METRIC(1)		DGK	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	235	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_J(max)$,$R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(max) - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.5 2.7V Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

	PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 2.2V	–	+/−0.7	+/−5 **+/−7**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V & V_{CM} = 2.2V (3)	–	+/−2	–	µV/C
I_B	Input Bias Current	V_{CM} = 0.5V (4)	–	−1.20	−2.00 **−2.70**	µA
		V_{CM} = 2.2V (4)	–	+0.49	+1.00 **+1.60**	
I_{OS}	Input Offset Current	V_{CM} = 0.5V & V_{CM} = 2.2V	–	20	250 **400**	nA
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 1.0V	76 **60**	100	–	dB
		V_{CM} stepped from 1.7V to 2.7V	–	100	–	
		V_{CM} stepped from 0V to 2.7V	58 **50**	70	–	
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 2.7V to 5V	78 **74**	104	–	dB
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	–	−0.3	−0.1 **0.0**	V
			2.8 **2.7**	3.0	–	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 2.2V, R_L = 10k to V^-	70 **67**	78	–	dB
		V_O = 0.5 to 2.2V, R_L = 2k to V^-	67 **63**	73	–	dB
V_O	Output Swing High	R_L = 10k to V^-	2.49 **2.46**	2.59	–	V
		R_L = 2k to V^-	2.45 **2.41**	2.53	–	
	Output Swing Low	R_L = 10k to V^-	–	90	100 **120**	mV
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (5)(6)	30 **20**	48	–	mA
		Sinking to V^+ V_{ID} = −200mV (5)(6)	50 **30**	65	–	
I_S	Supply Current (both amps)	No load, V_{CM} = 0.5V	–	2.0	2.5 **3.0**	mA
SR	Slew Rate (7)	A_V = +1, V_I = $2V_{PP}$	–	9	–	V/µs
f_u	Unity Gain-Frequency	V_I = 10mV, R_L = 2kΩ to V^+/2	–	10	–	MHz
GBWP	Gain Bandwidth Product	f = 50KHz	15.5 **14**	21	–	MHz
Phi_m	Phase Margin	V_I = 10mV	–	50	–	Deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	–	15	–	nV/ √Hz
i_n	Input-Referred Current Noise	f = 2KHz	–	1	–	pA/ √Hz
f_{max}	Full Power Bandwidth	Z_L = (20pF || 10kΩ) to V^+/2	–	1	–	MHz

(1) All limits are ensured by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.
(3) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) Short circuit test is a momentary test.
(6) Output short circuit duration is infinite for V_S ≤ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(7) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

6.6 5V Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = 5V, V^- = 0V, V_{CM} = 1V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 1V & V_{CM} = 4.5V	–	+/−0.7	+/−5 **+/− 7**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 1V & V_{CM} = 4.5V (3)	–	+/−2	–	µV/°C
I_B	Input Bias Current	V_{CM} = 1V (4)	–	−1.18	−2.00 **−2.70**	µA
		V_{CM} = 4.5V (4)	–	+0.49	+1.00 **+1.60**	
I_{OS}	Input Offset Current	V_{CM} = 1V & V_{CM} = 4.5V	–	20	250 **400**	nA
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 3.3V	84 **72**	110	–	dB
		V_{CM} stepped from 4V to 5V	–	100	–	
		V_{CM} stepped from 0V to 5V	64 **61**	80	–	
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 2.7V to 5V, V_{CM} = 0.5V	78 **74**	104	–	dB
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	–	−0.3	−0.1 **0.0**	V
			5.1 **5.0**	5.3	–	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 4.5V, R_L = 10k to V^-	74 **70**	84	–	dB
		V_O = 0.5 to 4.5V, R_L = 2k to V^-	70 **66**	80	–	
V_O	Output Swing High	R_L = 10k to V^-	4.75 **4.72**	4.87	–	V
		R_L = 2k to V^-	4.70 **4.66**	4.81	–	
	Output Swing Low	R_L = 10k to V^-	–	86	125 **135**	mV
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (5)(6)	35 **20**	53	–	mA
		Sinking to V^+ V_{ID} = −200mV (5)(6)	60 **50**	75	–	
I_S	Supply Current (both amps)	No load, V_{CM} = 1V	–	2.3	2.8 **3.5**	mA
SR	Slew Rate (7)	A_V = +1, V_I = $5V_{PP}$	10 **7**	12	–	V/µs
f_u	Unity Gain Frequency	V_I = 10mV, R_L = 2kΩ to V^+/2	–	10.5	–	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	16 **15**	21	–	MHz
Phi_m	Phase Margin	V_I = 10mV	–	53	–	Deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	–	15	–	nV/ √Hz
i_n	Input-Referred Current Noise	f = 2KHz	–	1	–	pA/ √Hz

(1) All limits are ensured by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.
(3) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) Short circuit test is a momentary test.
(6) Output short circuit duration is infinite for V_S ≤ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(7) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V^+ = 5V, V^- = 0V, V_{CM} = 1V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
f_{max}	Full Power Bandwidth	Z_L = (20pF || 10kΩ) to V^+/2	–	900	–	KHz
t_S	Settling Time (+/−5%)	100mV_{PP} Step, 500pF load	–	400	–	ns
THD+N	Total Harmonic Distortion + Noise	R_L = 1kΩ to V^+/2 f = 10KHz to A_V= +2, 4V_{PP} swing	–	0.05%	–	

6.7 +/−11V Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = 11V, V^- = −11V, V_{CM} = 0V, V_O = 0V, and R_L > 1MΩ to 0V. **Boldface** limits apply at the temperature extremes.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = −10.5V & V_{CM} = 10.5V	–	+/−0.7	+/−7 **+/− 9**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} (3) = −10.5V & V_{CM} = 10.5V	–	+/−2	–	µV/°C
I_B	Input Bias Current	V_{CM} (4) = −10.5V	–	−1.05	−2.00 **−2.80**	µA
		V_{CM} (4) = 10.5V	–	+0.49	+1.00 **+1.50**	
I_{OS}	Input Offset Current	V_{CM} = −10.5V & V_{CM} = 10.5V	–	30	275 **550**	nA
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from −11V to 9V	84 **80**	100	–	dB
		V_{CM} stepped from 10V to 11V	–	100	–	
		V_{CM} stepped from −11V to 11V	74 **72**	88	–	
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 9V to 11V	70 **66**	100	–	dB
−PSRR	Negative Power Supply Rejection Ratio	V^- = −9V to −11V	70 **66**	100	–	dB
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	–	−11.3	−11.1 **−11.0**	V
			11.1 **11.0**	11.3	–	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0V to +/−9V, R_L = 10kΩ	78 **74**	85	–	dB
		V_O = 0V to +/−9V, R_L = 2kΩ	72 **66**	79	–	
V_O	Output Swing High	R_L = 10kΩ	10.65 **10.61**	10.77	–	V
		R_L = 2kΩ	10.6 **10.55**	10.69	–	
	Output Swing Low	R_L = 10kΩ	–	−10.98	−10.75 **−10.65**	V
		R_L = 2kΩ	–	−10.91	−10.65 **−10.6**	

(1) All limits are ensured by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.
(3) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(4) Positive current corresponds to current flowing into the device.

+/−11V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V^+ = 11V, V^- = −11V, V_{CM} = 0V, V_O = 0V, and R_L > 1MΩ to 0V. **Boldface** limits apply at the temperature extremes.

	PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
I_{SC}	Output Short Circuit Current	Sourcing to ground V_{ID} = 200mV (5)(6)	40 **25**	60	–	mA
		Sinking to ground V_{ID} = 200mV (5)(6)	65 **55**	100	–	
I_S	Supply Current	No load, V_{CM} = 0V	–	2.5	4 **5**	mA
SR	Slew Rate (7)	A_V = +1, V_I = 16V_{PP}	10 **8**	15	–	V/µs
f_U	Unity Gain Frequency	V_I = 10mV, R_L = 2kΩ	–	13	–	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	18 **16**	24	–	MHz
Phi_m	Phase Margin	V_I = 10mV	–	58	–	Deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	–	15	–	nV/ √Hz
i_n	Input-Referred Current Noise	f = 2KHz	–	1	–	pA/ √Hz
t_S	Settling Time (+/−1%, A_V = +1)	Positive Step, 5V_{PP}	–	320	–	ns
		Negative Step, 5V_{PP}	–	600	–	
THD+N	Total Harmonic Distortion +Noise	R_L = 1kΩ, f = 10KHz, A_V = +2, 15V_{PP} swing	–	0.01%	–	
CT_{REJ}	Cross-Talk Rejection	f = 5MHz, Driver R_L = 10kΩ	–	68	–	dB

(5) Short circuit test is a momentary test.
(6) Output short circuit duration is infinite for V_S ≤ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(7) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

6.8 Typical Performance Characteristics

T_A = 25°C, Unless Otherwise Noted

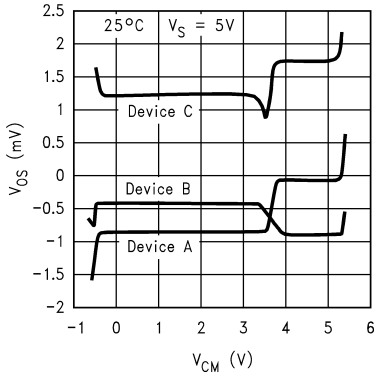


Figure 1. V_{OS} vs. V_{CM} for 3 Representative Units

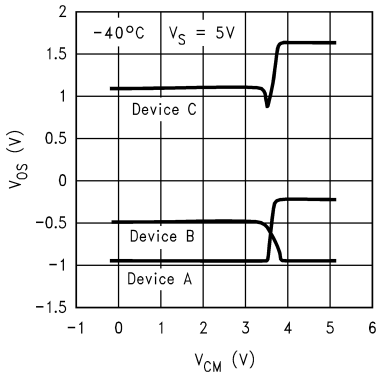


Figure 2. V_{OS} vs. V_{CM} for 3 Representative Units

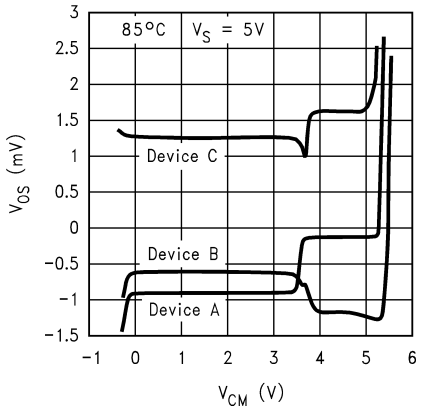


Figure 3. V_{OS} vs. V_{CM} for 3 Representative Units

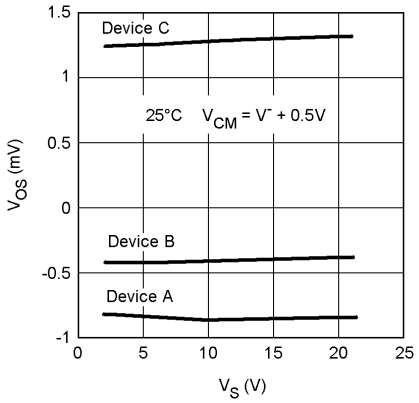


Figure 4. V_{OS} vs. V_S for 3 Representative Units

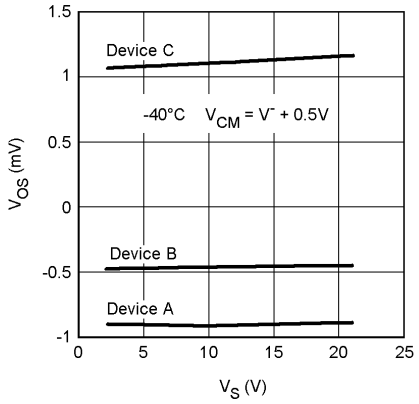


Figure 5. V_{OS} vs. V_S for 3 Representative Units

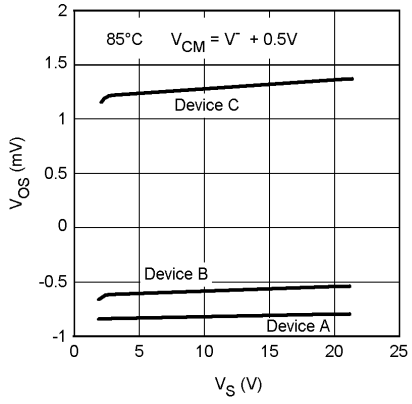


Figure 6. V_{OS} vs. V_S for 3 Representative Units

Typical Performance Characteristics (continued)

T_A = 25°C, Unless Otherwise Noted

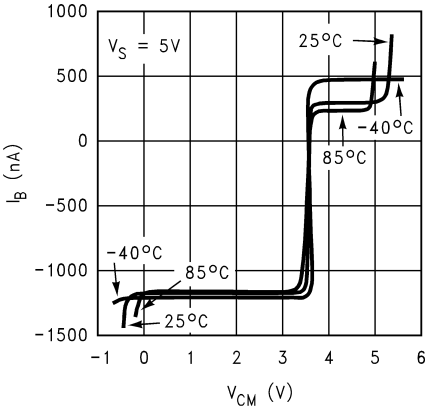


Figure 7. I_B vs. V_{CM}

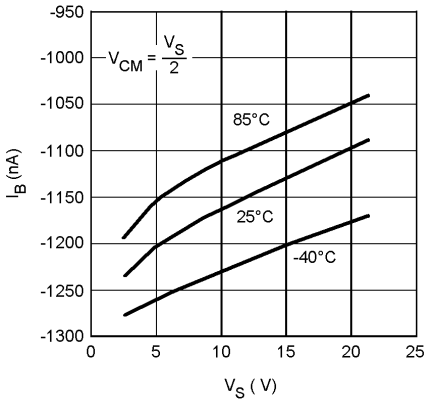


Figure 8. I_B vs. V_S

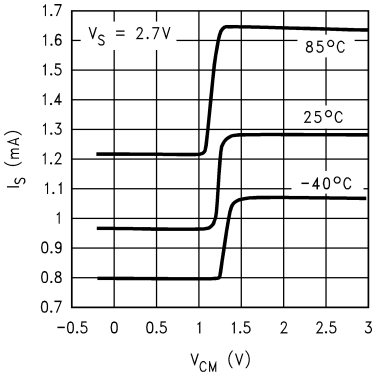


Figure 9. I_S vs. V_{CM}

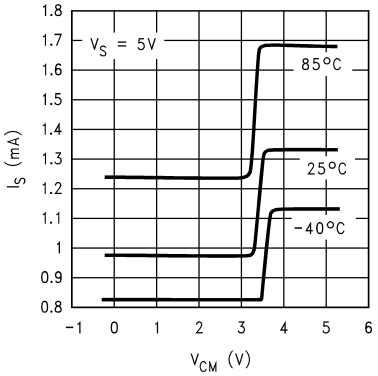


Figure 10. I_S vs. V_{CM}

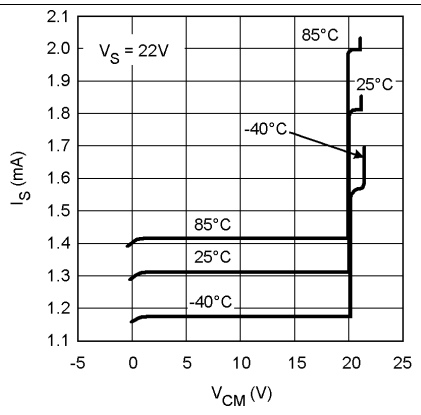


Figure 11. I_S vs. V_{CM}

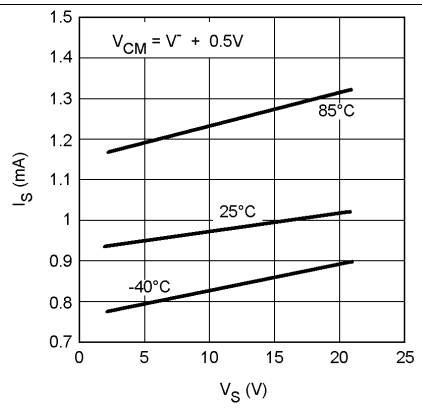


Figure 12. I_S vs. V_S (PNP side)

Typical Performance Characteristics (continued)

T_A = 25°C, Unless Otherwise Noted

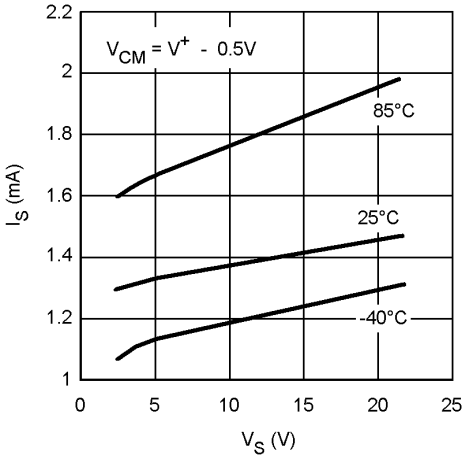


Figure 13. I_S vs. V_S (NPN side)

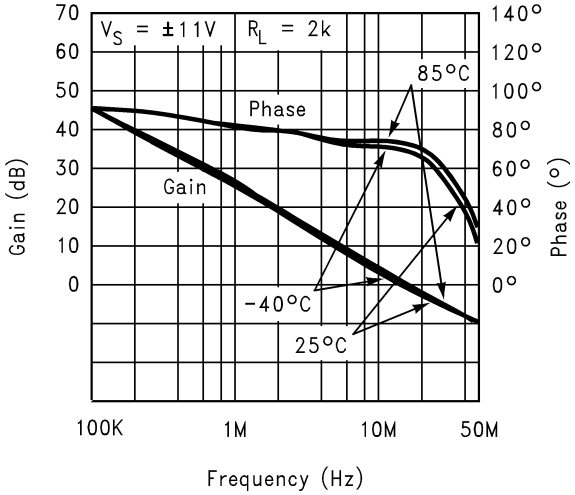


Figure 14. Gain/Phase vs. Frequency

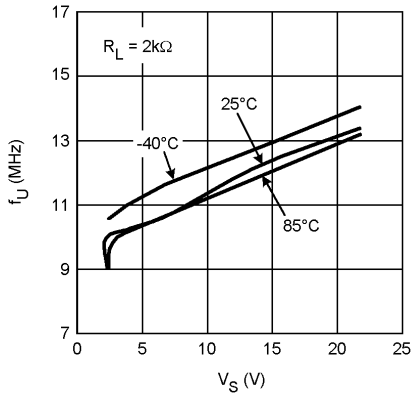


Figure 15. Unity Gain Frequency vs. V_S

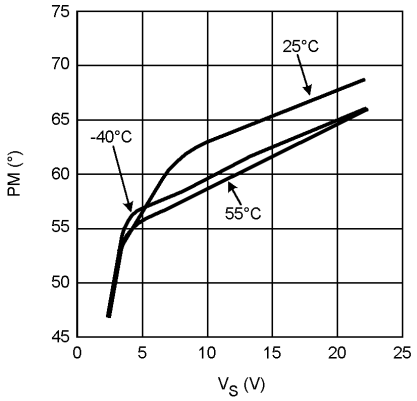


Figure 16. Phase Margin vs. V_S

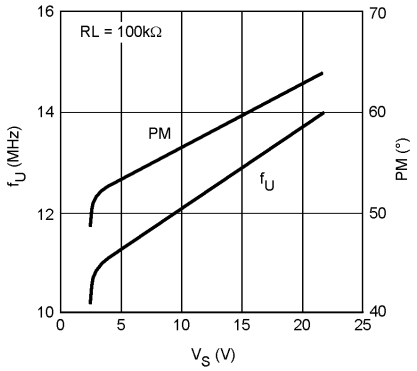


Figure 17. Unity Gain Freq. and Phase Margin vs. V_S

7 Device and Documentation Support

7.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

7.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

7.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

7.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM8262MM	LIFEBUY	VSSOP	DGK	8	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	A46	
LM8262MM/NOPB	LIFEBUY	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A46	
LM8262MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A46	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

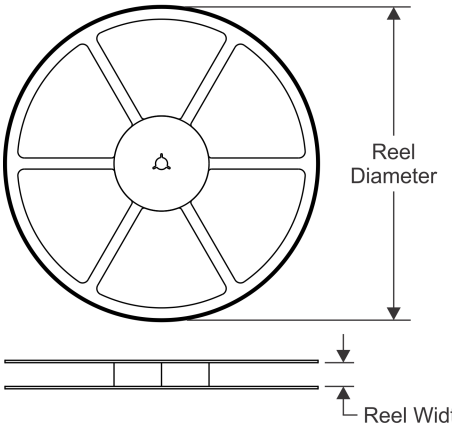
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

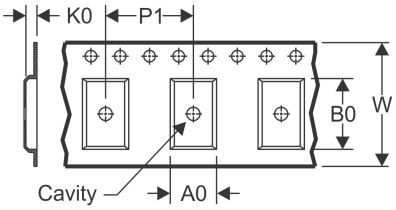
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

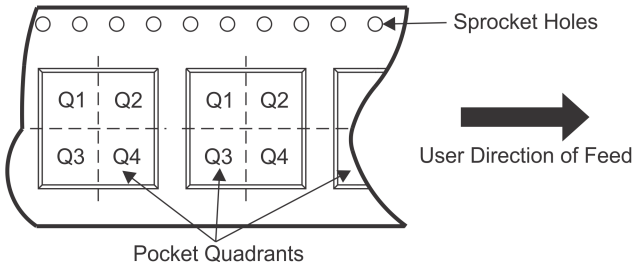


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

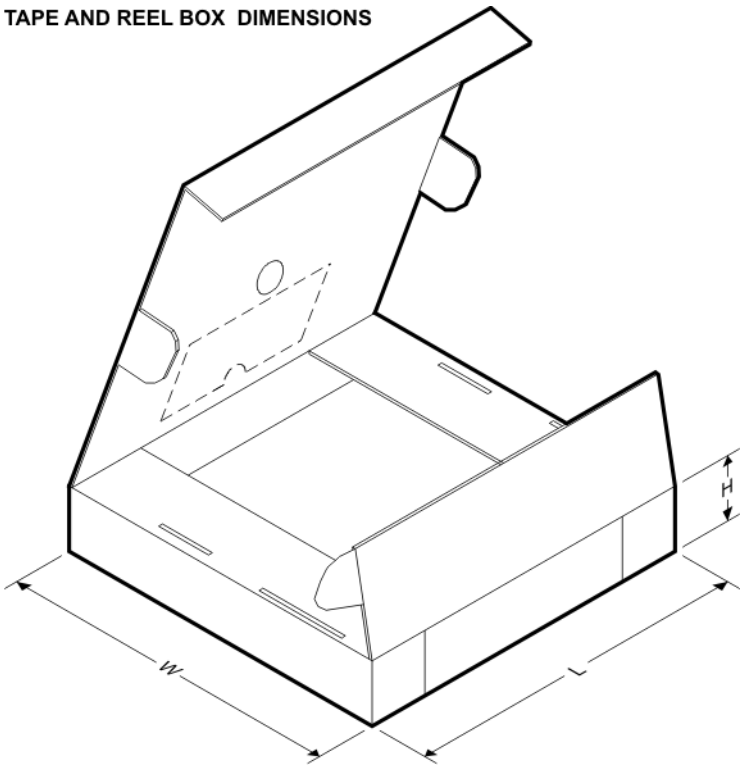
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM8262MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM8262MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM8262MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

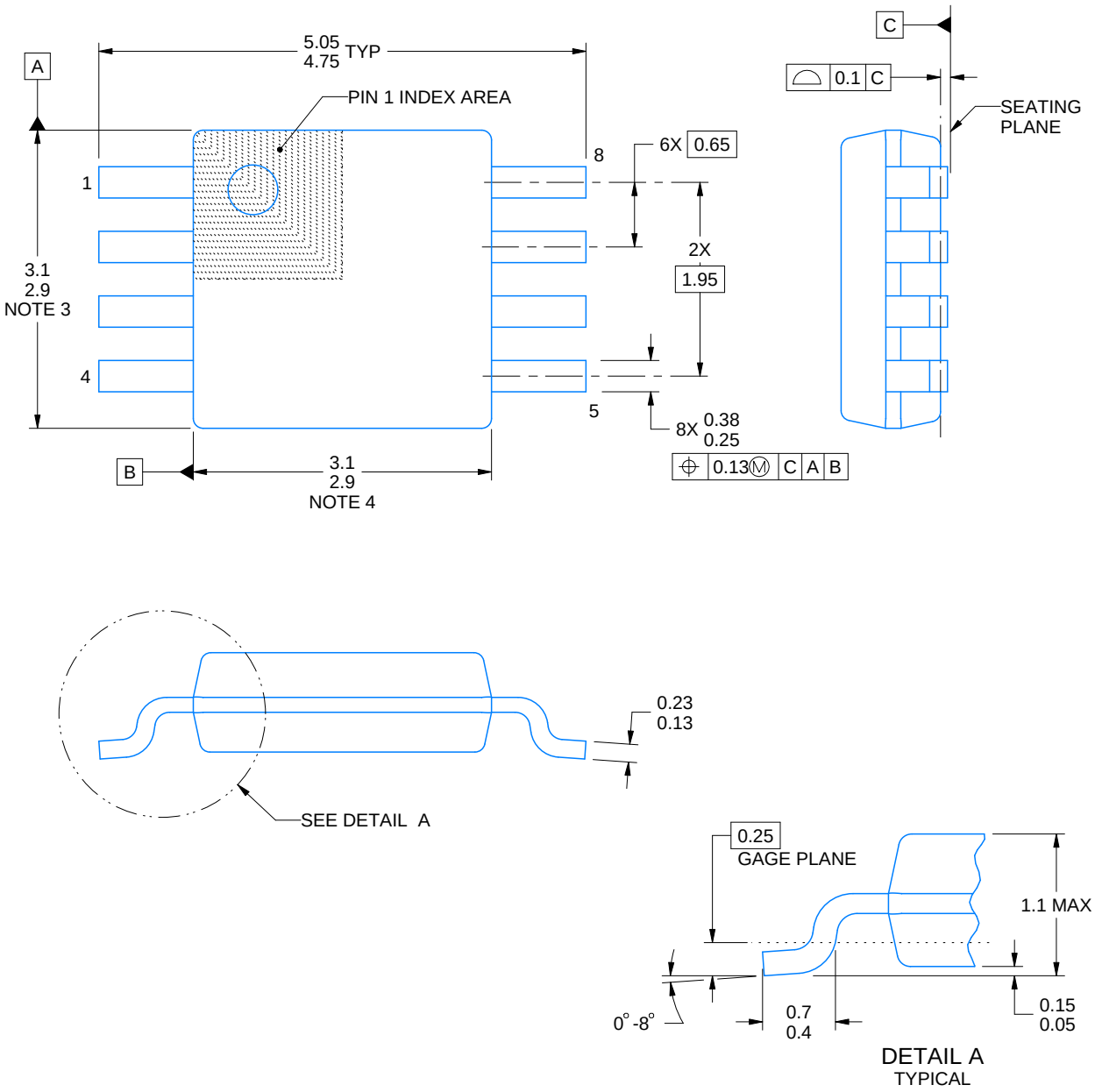
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM8262MM	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM8262MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM8262MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

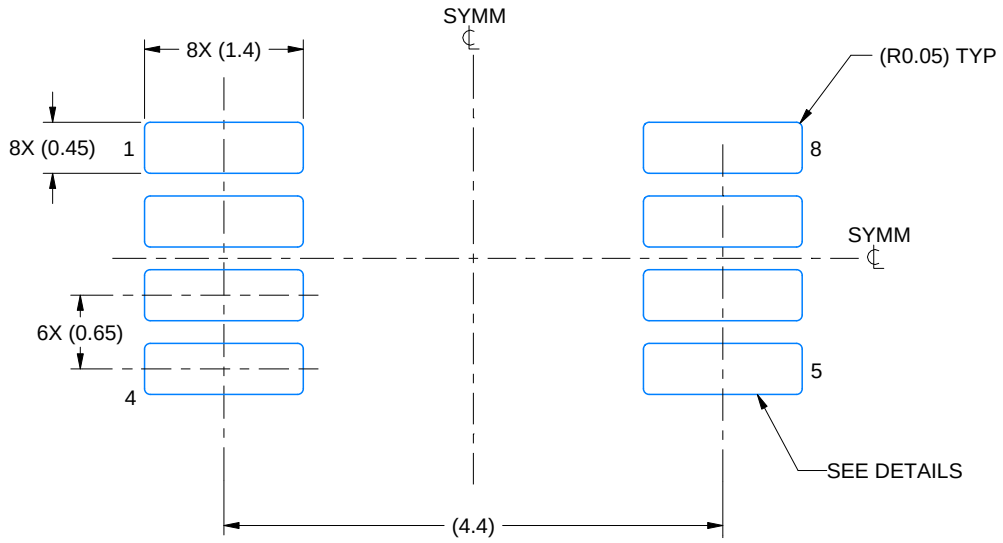
SMALL OUTLINE PACKAGE



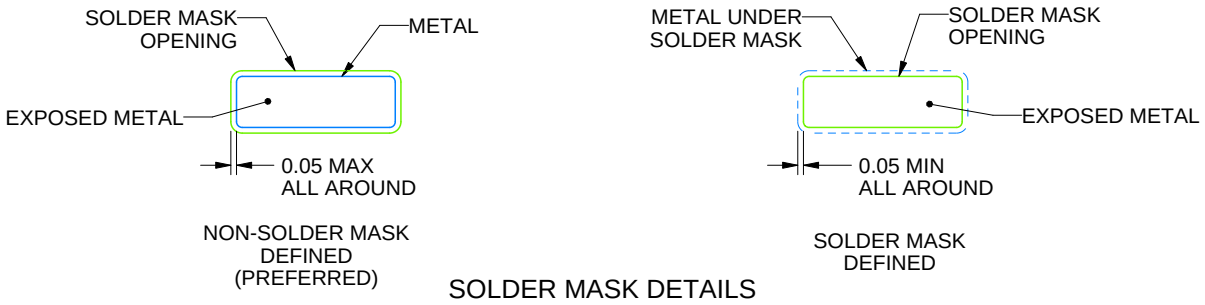
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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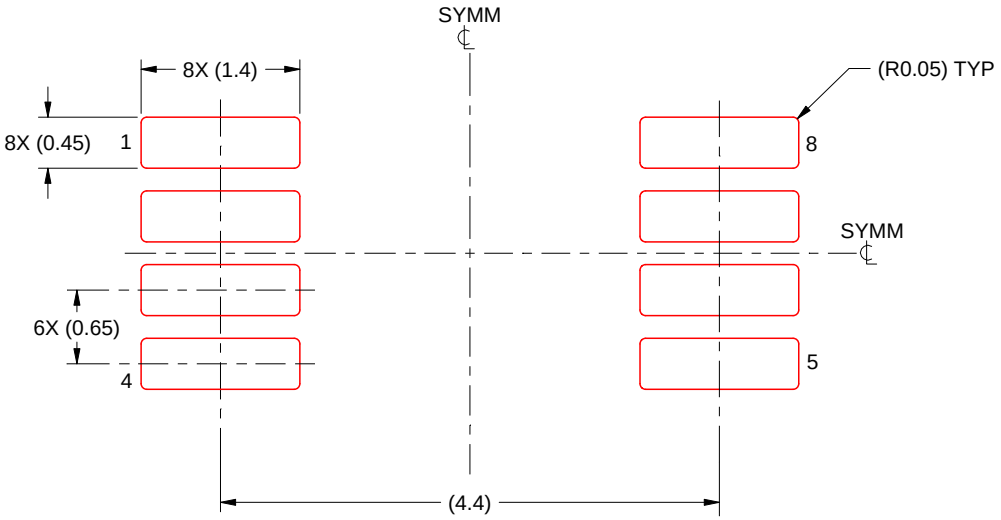
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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