LMV7291 Single 1.8V Low Power Comparator with Rail-to-Rail Input

Check for Samples: LMV7291

FEATURES

- \( V_S = 1.8V, \ T_A = 25^\circ C, \) Typical Values unless Specified
- Single Supply
- Ultra Low Supply Current 9\( \mu \)A per Channel
- Low Input Bias Current 10nA
- Low Input Offset Current 200pA
- Low ensured \( V_{OS} \) 4mV
- Propagation Delay 880ns (20mV Overdrive)
- Input Common Mode Voltage Range 0.1V beyond Rails

DESCRIPTION

The LMV7291 is a rail-to-rail input low power comparator, characterized at supply voltage 1.8V, 2.7V and 5.0V. It consumes only 9\( \mu \)A supply current per channel while achieving a 800ns propagation delay.

The LMV7291 is available in SC70 package. With this tiny package, the PC board area can be significantly reduced. It is ideal for low voltage, low power and space critical designs.

The LMV7291 features a push-pull output stage which allows operation with minimum power consumption when driving a load.

The LMV7291 is built with Texas Instruments’ advance submicron silicon-gate BiCMOS process. It has bipolar inputs for improved noise performance and CMOS outputs for rail-to-rail output swing.

APPLICATIONS

- Mobile Communications
- Laptops and PDA’s
- Battery Powered Electronics
- General Purpose Low Voltage Applications

Typical Circuit

![Typical Circuit Diagram](image)

Figure 1. Threshold Detector

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1)(2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD Tolerance</td>
<td>2KV (3)</td>
</tr>
<tr>
<td>ESD Tolerance</td>
<td>200V (4)</td>
</tr>
<tr>
<td>Differential Voltage</td>
<td>±Supply Voltage</td>
</tr>
<tr>
<td>Supply Voltage (V+ - V−)</td>
<td>5.5V</td>
</tr>
<tr>
<td>Voltage at Input/Output pins</td>
<td>V+ +0.1V, V− −0.1V</td>
</tr>
</tbody>
</table>

Soldering Information

<table>
<thead>
<tr>
<th>Method</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Infrared or Convection (20 sec.)</td>
<td>235°C</td>
</tr>
<tr>
<td>Wave Soldering (10 sec.)</td>
<td>260°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Junction Temperature (5)</td>
<td>+150°C</td>
</tr>
</tbody>
</table>

Operating Ratings (1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temperature Range</td>
<td>−40°C to +85°C</td>
</tr>
<tr>
<td>Package Thermal Resistance</td>
<td>265°C/W</td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) Human body model, 1.5kΩ in series with 100pF.

(4) Machine Model, 0Ω in series with 200pF.

(5) Typical values represent the most likely parametric norm.

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.
1.8V Electrical Characteristics

Unless otherwise specified, all limits ensured for T\textsubscript{J} = 25^\circ C, V\textsuperscript{+} = 1.8V, V\textsuperscript{−} = 0V. **Boldface** limits apply at the temperature extremes. \(^{(1)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min(^{(2)})</th>
<th>Typ(^{(3)})</th>
<th>Max(^{(2)})</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\textsubscript{OS}</td>
<td>Input Offset Voltage</td>
<td></td>
<td>0.3</td>
<td>4</td>
<td>6</td>
<td>mV</td>
</tr>
<tr>
<td>TC V\textsubscript{OS}</td>
<td>Input Offset Temperature Drift</td>
<td>V\textsubscript{CM} = 0.9V (^{(4)})</td>
<td>10</td>
<td></td>
<td></td>
<td>(\mu V/C)</td>
</tr>
<tr>
<td>I\textsubscript{B}</td>
<td>Input Bias Current</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>I\textsubscript{OS}</td>
<td>Input Offset Current</td>
<td></td>
<td>200</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>I\textsubscript{S}</td>
<td>Supply Current</td>
<td>LMV7291</td>
<td>9</td>
<td>12</td>
<td>14</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>I\textsubscript{SC}</td>
<td>Output Short Circuit Current</td>
<td>Sourcing, V\textsubscript{O} = 0.9V</td>
<td>3.5</td>
<td>6</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking, V\textsubscript{O} = 0.9V</td>
<td>4</td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{OL}</td>
<td>Output Voltage Low</td>
<td>I\textsubscript{O} = 0.5mA</td>
<td>1.7</td>
<td>1.74</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I\textsubscript{O} = 1.5mA</td>
<td>1.58</td>
<td>1.63</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>I\textsubscript{O} = −0.5mA</td>
<td>52</td>
<td>70</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I\textsubscript{O} = −1.5mA</td>
<td>166</td>
<td>220</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{CM}</td>
<td>Input Common Mode Voltage Range</td>
<td>CMRR &gt; 45 dB</td>
<td>1.9</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>−0.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>0 &lt; V\textsubscript{CM} &lt; 1.8V</td>
<td>47</td>
<td>78</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>V\textsuperscript{+} = 1.8V to 5V</td>
<td>55</td>
<td>80</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>I\textsubscript{LEAKAGE}</td>
<td>Output Leakage Current</td>
<td>V\textsubscript{O} = 1.8V</td>
<td>2</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T\textsubscript{J} = T\textsubscript{A}. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T\textsubscript{J} > T\textsubscript{A}. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

\(^{(2)}\) All limits are specified by testing or statistical analysis.

\(^{(3)}\) Typical values represent the most likely parametric norm.

\(^{(4)}\) Offset Voltage average drift determined by dividing the change in V\textsubscript{OS} at temperature extremes into the total temperature change.

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T\textsubscript{J} = 25^\circ C, V\textsuperscript{+} = 1.8V, V\textsuperscript{−} = 0V, V\textsubscript{CM} = 0.5V, V\textsubscript{O} = V\textsuperscript{+}/2 and R\textsubscript{L} > 1M\(\Omega\) to V\textsuperscript{−}. **Boldface** limits apply at the temperature extremes. \(^{(1)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min(^{(2)})</th>
<th>Typ(^{(3)})</th>
<th>Max(^{(2)})</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t\textsubscript{PHL}</td>
<td>Propagation Delay (High to Low)</td>
<td>Input Overdrive = 20mV Load = 50pF//5k(\Omega)</td>
<td>880</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input Overdrive = 50mV Load = 50pF//5k(\Omega)</td>
<td>570</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t\textsubscript{PLH}</td>
<td>Propagation Delay (Low to High)</td>
<td>Input Overdrive = 20mV Load = 50pF//5k(\Omega)</td>
<td>1100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input Overdrive = 50mV Load = 50pF//5k(\Omega)</td>
<td>800</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T\textsubscript{J} = T\textsubscript{A}. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T\textsubscript{J} > T\textsubscript{A}. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

\(^{(2)}\) All limits are specified by testing or statistical analysis.

\(^{(3)}\) Typical values represent the most likely parametric norm.
### 2.7V Electrical Characteristics

Unless otherwise specified, all limits ensured for \( T_J = 25^\circ C, V^+ = 2.7V, V^- = 0V \). **Boldface** limits apply at the temperature extremes.  

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min(^{(2)})</th>
<th>Typ(^{(3)})</th>
<th>Max(^{(2)})</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td></td>
<td>0.3</td>
<td>4</td>
<td>6</td>
<td>mV</td>
</tr>
<tr>
<td>( TC \ V_{OS} )</td>
<td>Input Offset Temperature Drift</td>
<td>( V_{CM} = 1.35V ) (^{(4)})</td>
<td>10</td>
<td></td>
<td></td>
<td>( \mu )V/C</td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Input offset Current</td>
<td>LMV7291</td>
<td>200</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td></td>
<td>9</td>
<td>13</td>
<td>15</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( I_{SC} )</td>
<td>Output Short Circuit Current</td>
<td>Sourcing, ( V_O = 1.35V )</td>
<td>12</td>
<td>15</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking, ( V_O = 1.35V )</td>
<td>12</td>
<td>15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{DH} )</td>
<td>Output Voltage High</td>
<td>( I_O = 0.5mA )</td>
<td>2.63</td>
<td>2.66</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_O = 2.0mA )</td>
<td>2.48</td>
<td>2.55</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output Voltage Low</td>
<td>( I_O = -0.5mA )</td>
<td>50</td>
<td>70</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_O = -2mA )</td>
<td>155</td>
<td>220</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{CM} )</td>
<td>Input Common Voltage Range</td>
<td>CMRR &gt; 45dB</td>
<td>2.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(-0.1)</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>( 0 &lt; V_{CM} &lt; 2.7V )</td>
<td>47</td>
<td>78</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>( V^+ = 1.8V ) to 5V</td>
<td>55</td>
<td>80</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( I_{LEAKAGE} )</td>
<td>Output Leakage Current</td>
<td>( V_O = 2.7V )</td>
<td>2</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that \( T_J = T_A \). No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where \( T_J > T_A \). Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

\(^{(2)}\) All limits are specified by testing or statistical analysis.

\(^{(3)}\) Typical values represent the most likely parametric norm.

\(^{(4)}\) Offset Voltage average drift determined by dividing the change in \( V_{OS} \) at temperature extremes into the total temperature change.

### 2.7V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for \( T_J = 25^\circ C, V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2 \) and \( R_L > 1\Omega \) to \( V^- \). **Boldface** limits apply at the temperature extremes.  

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min(^{(2)})</th>
<th>Typ(^{(3)})</th>
<th>Max(^{(2)})</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PHL} )</td>
<td>Propagation Delay</td>
<td>Input Overdrive = 20mV</td>
<td>1200</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>(High to Low)</td>
<td>Load = 50pF//5kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input Overdrive = 50mV</td>
<td>810</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Load = 50pF//5kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation Delay</td>
<td>Input Overdrive = 20mV</td>
<td>1300</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>(Low to High)</td>
<td>Load = 50pF//5kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input Overdrive = 50mV</td>
<td>860</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Load = 50pF//5kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that \( T_J = T_A \). No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where \( T_J > T_A \). Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

\(^{(2)}\) All limits are specified by testing or statistical analysis.

\(^{(3)}\) Typical values represent the most likely parametric norm.
## 5V Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J = 25^\circ C$, $V^+ = 5V$, $V^- = 0V$. Boldface limits apply at the temperature extremes. (1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min(2)</th>
<th>Typ(3)</th>
<th>Max(2)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td></td>
<td>0.3</td>
<td>4</td>
<td>6</td>
<td>mV</td>
</tr>
<tr>
<td>$TC V_{OS}$</td>
<td>Input Offset Temperature Drift</td>
<td>$V_{CM} = 2.5V$ (4)</td>
<td></td>
<td>10</td>
<td></td>
<td>$\mu V/C$</td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input Bias Current</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current</td>
<td>LMV7291</td>
<td></td>
<td>200</td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td></td>
<td>10</td>
<td>14</td>
<td>16</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Output Short Circuit Current</td>
<td>Sourcing, $V_O = 2.5V$</td>
<td>28</td>
<td>34</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking, $V_O = 2.5V$</td>
<td>28</td>
<td>34</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DH}$</td>
<td>Output Voltage High</td>
<td>$I_O = 0.5mA$</td>
<td>4.93</td>
<td>4.96</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_O = 4.0mA$</td>
<td>4.70</td>
<td>4.77</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Voltage Low</td>
<td>$I_O = -0.5mA$</td>
<td>27</td>
<td>70</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_O = -4.0mA$</td>
<td>225</td>
<td>300</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CM}$</td>
<td>Input Common Voltage Range</td>
<td>CMRR &gt; 45dB</td>
<td></td>
<td>5.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$-0.1$</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>$0 &lt; V_{CM} &lt; 5.0V$</td>
<td>47</td>
<td>78</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>$V^+ = 1.8V$ to $5V$</td>
<td>55</td>
<td>80</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$I_{LEAKAGE}$</td>
<td>Output Leakage Current</td>
<td>$V_O = 5V$</td>
<td>2</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
</tbody>
</table>

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

(2) All limits are specified by testing or statistical analysis.

(3) Typical values represent the most likely parametric norm.

(4) Offset Voltage average drift determined by dividing the change in $V_{OS}$ at temperature extremes into the total temperature change.

### 5.0V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J = 25^\circ C$, $V^+ = 5.0V$, $V^- = 0V$, $V_{CM} = 0.5V$, $V_O = V^+/2$ and $R_L > 1M\Omega$ to $V^-$. Boldface limits apply at the temperature extremes. (1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
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<td>Input Overdrive = 50mV Load = 50pF/5k$\Omega$</td>
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<td>$t_{PLH}$</td>
<td>Propagation Delay (Low to High)</td>
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<td></td>
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<td>Input Overdrive = 50mV Load = 50pF/5k$\Omega$</td>
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<td></td>
<td></td>
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(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

(2) All limits are specified by testing or statistical analysis.

(3) Typical values represent the most likely parametric norm.
Figure 2. 5-Pin SC70 – Top View
See Package Number DCK
Typical Performance Characteristics

\( T_A = 25^\circ C \), Unless otherwise specified.

**Figure 3.**

**Figure 4.**

**Figure 5.**

**Figure 6.**

**Figure 7.**

**Figure 8.**
Typical Performance Characteristics (continued)

(\(T_A = 25^\circ C\), Unless otherwise specified).

**Supply Current vs. Supply Voltage**

![Supply Current vs. Supply Voltage](image1)

**Output Positive Swing vs. \(V_{SUPPLY}\)**

![Output Positive Swing vs. \(V_{SUPPLY}\)](image2)

**Output Negative Swing vs. \(V_{SUPPLY}\)**

![Output Negative Swing vs. \(V_{SUPPLY}\)](image3)

**Output Positive Swing vs. \(I_{SOURCE}\)**

![Output Positive Swing vs. \(I_{SOURCE}\)](image4)

**Output Negative Swing vs. \(I_{SINK}\)**

![Output Negative Swing vs. \(I_{SINK}\)](image5)

**Output Positive Swing vs. \(I_{SOURCE}\)**

![Output Positive Swing vs. \(I_{SOURCE}\)](image6)
Typical Performance Characteristics (continued)

\(T_A = 25^\circ C\), Unless otherwise specified.

**Output Negative Swing**

\[ V_{S\text{UPPLY}} = 2.7V \]

\[ V_{\text{OUT}} = V(V) \]

\[ I_{\text{SINK}} = \text{mA} \]

**Output Positive Swing**

\[ V_{\text{S\text{UPPLY}}} = 5V \]

\[ V_{\text{OUT}} = V(V) \]

\[ I_{\text{SOURCE}} = \text{mA} \]

**Propagation Delay (\(t_{\text{PLH}}\))**

\[ V_{\text{CC}} = 1.8V \]

\[ \text{TEMP} = 25^\circ C \]

\[ \text{LOAD} = 5k\Omega/50pF \]

\[ 50mV \]

\[ 20mV \]

\[ 50pF \]

**Propagation Delay (\(t_{\text{PHL}}\))**

\[ V_{\text{CC}} = 2.7V \]

\[ \text{TEMP} = 25^\circ C \]

\[ \text{LOAD} = 5k\Omega/50pF \]

\[ 50mV \]

\[ 20mV \]

\[ 50pF \]
Typical Performance Characteristics (continued)

\(T_A = 25°C,\) Unless otherwise specified.

![Figure 21. Propagation Delay \(t_{PHL}\)](image)

![Figure 22. Propagation Delay \(t_{PLH}\)](image)

![Figure 23. Propagation Delay \(t_{PHL}\)](image)

![Figure 24. \(t_{PHL} \text{ vs. Overdrive}\)](image)

![Figure 25. \(t_{PLH} \text{ vs. Overdrive}\)](image)
APPLICATION NOTES

BASIC COMPARATOR

A comparator is often used to convert an analog signal to a digital signal. As shown in Figure 26, the comparator compares an input voltage ($V_{IN}$) to a reference voltage ($V_{REF}$). If $V_{IN}$ is less than $V_{REF}$, the output ($V_O$) is low. However, if $V_{IN}$ is greater than $V_{REF}$, the output voltage ($V_O$) is high.

![Figure 26. LMV7291 Basic Comparator](image)

RAIL-TO-RAIL INPUT STAGE

The LMV7291 has an input common mode voltage range ($V_{CM}$) of $-0.1V$ below the $V^-$ to $0.1V$ above $V^+$. This is achieved by using paralleled PNP and NPN differential input pairs. When the $V_{CM}$ is near $V^+$, the NPN pair is on and the PNP pair is off. When the $V_{CM}$ is near $V^-$, the NPN pair is off and the PNP pair is on. The crossover point between the NPN and PNP input stages is around 950mV from $V^+$. Since each input stage has its own offset voltage ($V_{OS}$), the $V_{OS}$ of the comparator becomes a function of the $V_{CM}$. See Figure 3, Figure 4, and Figure 5 in Typical Performance Characteristics. In application design, it is recommended to keep the $V_{CM}$ away from the crossover point to avoid problems. The wide input voltage range makes LMV7291 ideal in power supply monitoring circuits, where the comparators are used to sense signals close to gnd and power supplies.

OUTPUT STAGE

The LMV7291 has a push-pull output stage. This output stage keeps the total system power consumption to the absolute minimum. The only current consumed is the low supply current and the current going directly into the load. When output switches, both PMOS and NMOS at the output stage are on at the same time for a very short time. This allows current to flow directly between $V^+$ and $V^-$ through output transistors. The result is a short spike of current (shoot-through current) drawn from the supply and glitches in the supply voltages. The glitches can spread to other parts of the board as noise. To prevent the glitches in supply lines, power supply bypass capacitors must be installed. See CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS for details.

HYSTERESIS

It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier of its own noise.

Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three resistor network that are referenced to the supply voltage $V_{CC}$ of the comparator (Figure 27). When $V_{IN}$ at the inverting input is less than $V_A$, the voltage at the non-inverting node of the comparator ($V_{IN} < V_A$), the output voltage is high (for simplicity assume $V_O$ switches as high as $V_{CC}$). The three network resistors can be represented as $R_1 || R_3$ in series with $R_2$. The lower input trip voltage $V_{A1}$ is defined as
When $V_{IN}$ is greater than $V_A$ ($V_{IN} > V_A$), the output voltage is low and very close to ground. In this case the three network resistors can be presented as $R_2//R_3$ in series with $R_1$. The upper trip voltage $V_{A2}$ is defined as

$$V_{A2} = \frac{V_{CC} (R_2||R_3)}{R_1 + (R_2||R_3)}$$

The total hysteresis provided by the network is defined as

$$\Delta V_A = V_{A1} - V_{A2}$$

A good typical value of $\Delta V_A$ would be in the range of 5 to 50 mV. This is easily obtained by choosing $R_3$ as 1000 to 100 times $(R_1||R_2)$ for 5V operation, or as 300 to 30 times $(R_1||R_2)$ for 1.8V operation.

**Non-Inverting Comparator with Hysteresis**

A non-inverting comparator with hysteresis requires a two resistor network, and a voltage reference ($V_{REF}$) at the inverting input (Figure 28). When $V_{IN}$ is low, the output is also low. For the output to switch from low to high, $V_{IN}$ must rise up to $V_{IN1}$, where $V_{IN1}$ is calculated by

$$V_{IN1} = \frac{V_{ref} (R_1 + R_2)}{R_2}$$
When \( V_{IN} \) is high, the output is also high. To make the comparator switch back to its low state, \( V_{IN} \) must equal \( V_{REF} \) before \( V_A \) will again equal \( V_{REF} \). \( V_{IN} \) can be calculated by:

\[
V_{IN2} = \frac{v_{ref} (R_1 + R_2) - V_{CC} R_1}{R_2}
\]

The hysteresis of this circuit is the difference between \( V_{IN1} \) and \( V_{IN2} \).

\[
\Delta V_{IN} = V_{CC} R_1 / R_2
\]

Figure 28. Non-Inverting Comparator with Hysteresis

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

Feedback to almost any pin of a comparator can result in oscillation. In addition, when the input signal is a slow voltage ramp or sine wave, the comparator may also burst into oscillation near the crossing point. To avoid oscillation or instability, PCB layout should be engineered thoughtfully. Several precautions are recommended:

1. Power supply bypassing is critical, and will improve stability and transient response. Resistance and inductance from power supply wires and board traces increase power supply line impedance. When supply current changes, the power supply line will move due to its impedance. Large enough supply line shift will cause the comparator to mis-operate. To avoid problems, a small bypass capacitor, such as 0.1\( \mu \)F ceramic, should be placed immediately adjacent to the supply pins. An additional 6.8\( \mu \)F or greater tantalum capacitor should be placed at the point where the power supply for the comparator is introduced onto the board. These capacitors act as an energy reservoir and keep the supply impedance low. In dual supply application, a 0.1\( \mu \)F capacitor is recommended to be placed across \( V^+ \) and \( V^- \) pins.

2. Keep all leads short to reduce stray capacitance and lead inductance. It will also minimize any unwanted coupling from any high-level signals (such as the output). The comparators can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Try to avoid a long loop which could act as an inductor (coil).

3. It is a good practice to use an unbroken ground plane on a printed circuit board to provide all components with a low inductive ground connection. Make sure ground paths are low-impedance where heavier currents are flowing to avoid ground level shift. Preferably there should be a ground plane under the component.

4. The output trace should be routed away from inputs. The ground plane should extend between the output and inputs to act as a guard.
5. When the signal source is applied through a resistive network to one input of the comparator, it is usually advantageous to connect the other input with a resistor with the same value, for both DC and AC consideration. Input traces should be laid out symmetrically if possible.

6. All pins of any unused comparators should be tied to the negative supply.

Typical Applications

POSITIVE PEAK DETECTOR

A positive peak detect circuit is basically a comparator operated in a unity gain follower configuration, with a capacitor as a load to maintain the highest voltage. A diode is added at the output to prevent the capacitor from discharging through the output, and a 1MΩ resistor added in parallel to the capacitor to provide a high impedance discharge path. When the input $V_{IN}$ increases, the inverting input of the comparator follows it, thus charging the capacitor. When it decreases, the cap discharges through the 1MΩ resistor. The decay time can be modified by changing the resistor. The output should be accessed through a follower circuit to prevent loading.

NEGATIVE PEAK DETECTOR

For the negative detector, the output transistor of the comparator acts as a low impedance current sink. Since there is no pull-up resistor, the only discharge path will be the 1MΩ resistor and any load impedance used. Decay time is changed by varying the 1MΩ resistor.

SQUARE WAVE GENERATOR

A typical application for a comparator is as a square wave oscillator. The circuit below generates a square wave whose period is set by the RC time constant of the capacitor $C_1$ and resistor $R_4$. The maximum frequency is limited by the large signal propagation delay of the comparator, and by the capacitive loading at the output, which limits the output slew rate.
To analyze the circuit, consider it when the output is high. That implies that the inverted input ($V_C$) is lower than the non-inverting input ($V_A$). This causes the $C_1$ to get charged through $R_4$, and the voltage $V_C$ increases till it is equal to the non-inverting input. The value of $V_A$ at this point is

$$V_{A1} = \frac{V_{CC}R_2}{R_2 + R_1||R_3}$$

(7)

If $R_1 = R_2 = R_3$ then $V_{A1} = 2V_{CC}/3$

At this point the comparator switches pulling down the output to the negative rail. The value of $V_A$ at this point is

$$V_{A2} = \frac{V_{CC}(R_2||R_3)}{R_1 + (R_2||R_3)}$$

(8)

If $R_1 = R_2 = R_3$ then $V_{A2} = V_{CC}/3$

The capacitor $C_1$ now discharges through $R_4$, and the voltage $V_C$ decreases till it is equal to $V_{A2}$, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge $C_1$ from $2V_{CC}/3$ to $V_{CC}/3$, which is given by $R_4C_1\ln2$. Hence the formula for the frequency is:

$$F = \frac{1}{2(R_4C_1\ln2)}$$
## REVISION HISTORY

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## PACKAGING INFORMATION

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<td>C36</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD:** The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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<td>8.0</td>
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*All dimensions are nominal.*

A0: Dimension designed to accommodate the component width
B0: Dimension designed to accommodate the component length
K0: Dimension designed to accommodate the component thickness
W: Overall width of the carrier tape
P1: Pitch between successive cavity centers

*www.ti.com 23-Sep-2013*
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

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<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
DCK (R-PDSO-G5)  PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.
LAND PATTERN DATA

DCK (R-PDSO-G5)  PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005 inch).

2.2

6x0.35

0.85

2x0.65

2x1.30

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7521 for other stencil recommendations.

4210556-2/C  07/11

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