

LM741QML Operational Amplifier

Check for Samples: LM741QML

FEATURES

The amplifier offers many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations

DESCRIPTION

The LM741 is a general purpose operational amplifier which features improved performance over industry standards such as the LM709. They are direct, plugin replacements for the 709C, LM201, MC1439 and 748 in most applications.

Connection Diagrams

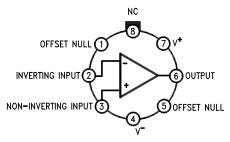


Figure 1. Metal Can Package See Package Number LMC0008C

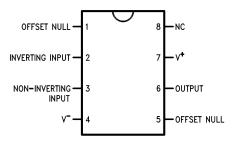


Figure 2. Dual-In-Line Package See Package Number NAB0008A

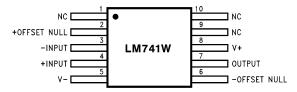
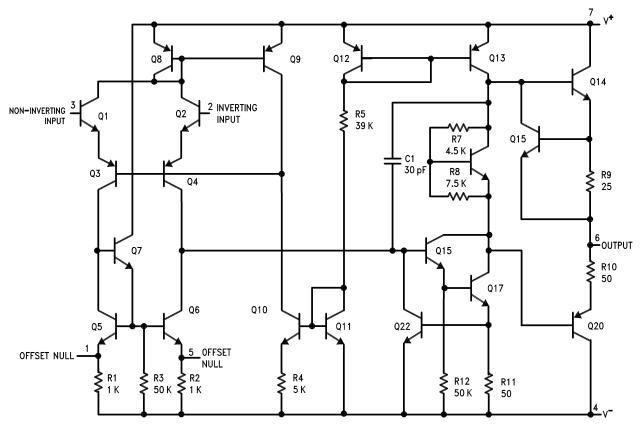


Figure 3. Ceramic Flatpak and SOIC Package See Package Number NAD0010A & NAC0010A

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet. All trademarks are the property of their respective owners.



Schematic Diagram





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

www.ti.com

Absolute Maximum Ratings(1)

Supply Voltage			±22V		
Power Dissipation (2)	500 mW				
Differential Input Voltage			±30V		
Input Voltage (3)	±15V				
Output Short Circuit Duration	Continuous				
Operating Temperature Range	-55°C ≤ T _A ≤ +125°C				
Storage Temperature Range			-65°C ≤ T _A ≤ +150°C		
Junction Temperature (T _J)			150°C		
Lead Temperature (Soldering, 10	Seconds)		300°C		
Thermal Resistance	θ_{JA}	Metal Can (Still Air)	167°C/W		
		Metal Can (500LF / Min Air Flow)	100°C/W		
		CERDIP (Still Air)	TBD		
		CERDIP (500LF / Min Air Flow)	TBD		
		CERPACK (Still Air)	228°C/W		
		CERPACK (500LF / Min Air Flow)	154°C/W		
		Ceramic SOIC (Still Air)	228°C/W		
		Ceramic SOIC (500LF / Min Air Flow)	154°C/W		
	θ_{JC}	Metal Can	44°C/W		
		CERDIP	TBD		
		CERPACK	27°C/W		
		Ceramic SOIC	27°C/W		
Package Weight (typical)	Metal Can		1000mg		
	CERDIP		1100mg		
	CERPACK		260mg		
	Ceramic S	Ceramic SOIC			
ESD Tolerance ⁽⁴⁾			400V		

- Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
- Human body model, 1.5 kΩ in series with 100 pF.



Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

Electrical Characteristics DC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

DC: $V_{CC} = \pm 15V, V_{CM} = 0V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub- group
V _{IO} In	Input Offset Voltage	Offset Voltage $V_{CM} = -12V$			5.0	mV	1
				-6.0	6.0	mV	2, 3
		V _{CM} = 12V		-5.0	5.0	mV	1
				-6.0	6.0	mV	2, 3
				-5.0	5.0	mV	1
				-6.0	6.0	mV	2, 3
		+V _{CC} = ± 5V		-5.0	5.0	mV	1
				-6.0	6.0	mV	2, 3
-V _{IO} Adj	Offset Null				-6.0	mV	1, 2, 3
+V _{IO} Adj	Offset Null			6.0		mV	1, 2, 3
I _{IO}	Input Offset Current	V _{CM} = -12V		-200	200	nA	1
				-500	500	nA	2, 3
		V _{CM} = 12V		-200	200	nA	1
				-500	500	nA	2, 3
				-200	200	nA	1
				-500	500	nA	2, 3
		$V_{CC} = \pm 5V$		-200	200	nA	1
				-500	500	nA	2, 3
±l _{IB}	Input Bias Current	V _{CM} = -12V		0.0	500	nA	1
				0.0	1500	nA	2, 3
		V _{CM} = 12V		0.0	500	nA	1
				0.0	1500	nA	2, 3
				0.0	500	nA	1
				0.0	1500	nA	2, 3
		V _{CC} = ± 5V		0.0	500	mA	1
		-		0.0	1500	nA	2, 3

Submit Documentation Feedback

Copyright © 2005–2013, Texas Instruments Incorporated



Electrical Characteristics DC Parameters (continued)

The following conditions apply to all the following parameters, unless otherwise specified.

DC: $V_{CC} = \pm 15V$, $V_{CM} = 0V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub- group
I _{CC}	Power Supply Current				2.8	mA	1
					2.5	mA	2
					3.5	mA	3
+A _{VS}	Open Loop Voltage Gain	$R_L = 2K\Omega$, $V_O = 0$ to 10V	See ⁽¹⁾	50		V/mV	1
			See ⁽¹⁾	25		V/mV	2, 3
-A _{VS}	Open Loop Voltage Gain	$R_L = 2K\Omega$, $V_O = 0$ to $-10V$	See ⁽¹⁾	50		V/mV	1
			See ⁽¹⁾	25		V/mV	2, 3
+PSRR	Power Supply Rejection Ratio	$+V_{CC} = 15V \text{ to } 5V, -V_{CC} = -15V$		77		dB	1, 2, 3
-PSRR	Power Supply Rejection Ratio	$-V_{CC} = -15V \text{ to } -5V,$ $+V_{CC} = +15V$		77		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	-12V ≤ V _{CM} ≤ 12V		70		dB	1, 2, 3
+l _{OS}	Output Short Circuit Current			-45	-5.0	mA	1,2
				-50	-5.0	mA	3
-l _{os}	Output Short Circuit Current			5.0	45	mA	1,2
				5.0	50	mA	3
+V _{Opp}	Output Voltage Swing	$R_L = 10K\Omega$		12		V	1, 2, 3
		$R_L = 2K\Omega$		10		V	1, 2, 3
		$V_{CC} = \pm 20V$, $R_L = 10K\Omega$		16		V	1, 2, 3
		$V_{CC} = \pm 20V, R_L = 2K\Omega$		15		V	1, 2, 3
-V _{Opp}	Output Voltage Swing	$R_L = 10K\Omega$			-12	V	1, 2, 3
		$R_L = 2K\Omega$			-10	V	1, 2, 3
		$V_{CC} = \pm 20V$, $R_L = 10K\Omega$			-16	V	1, 2, 3
		$V_{CC} = \pm 20V, R_L = 2K\Omega$			-15	V	1, 2, 3
R _I	Input Resistance		See (2)	0.3		ΜΩ	1
V _I	Input Voltage Range	V _{CC} = ± 15V	See (3)	±12		V	1, 2, 3
Vo	Output Voltage Swing	V _{CC} = ± 5V	See ⁽²⁾	±2.0		V	1, 2, 3

Electrical Characteristics AC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

AC: $V_{CC} = \pm 15V$, $V_{CM} = 0V$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub- group
+SR	Slew Rate	$V_I = -5V$ to 5V, $A_V = 1$, $R_L = 2K\Omega$		0.2		V/µS	7
-SR	Slew Rate	$V_I = 5V$ to -5V, $A_V = 1$, $R_L = 2K\Omega$		0.2		V/µS	7
t _R	Rise Time	$R_L = 2K\Omega, A_V = 1, C_L = 100pF$			1.0	μS	7
os	Overshoot	$R_L = 2K\Omega, A_V = 1, C_L = 100pF$			30	%	7
GBW	Gain Bandwidth	$V_{\rm I}$ = 50m $V_{\rm RMS}$, f = 20KHz, $R_{\rm L}$ = 2K Ω		250		KHz	-

Product Folder Links: LM741QML

⁽¹⁾ Datalog reading in K = V/mV(2) Specified parameter, not tested.

Ensured by CMRR, I_{IB}, I_{IO}, V_{IO}



Typical Application

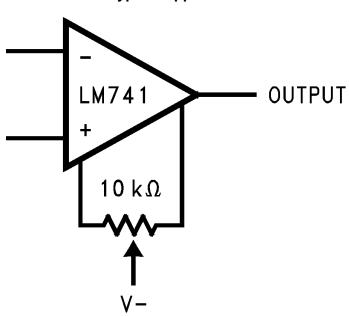


Figure 4. Offset Nulling Circuit



REVISION HISTORY

Date Released	Revision	Section	Originator	Changes
08/22/05	A	New Release to the corporate format	L. Lytle	1 MDS datasheet converted into one corporate datasheet format. Since drift is not performed on 883 product, the table was removed. MNLM741-X Rev 1A0 will be archived.
03/26/13	А	All	-	Changed layout of National Data Sheet to TI format.

Product Folder Links: LM741QML

www.ti.com 17-Jun-2023

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LM741 MD8	ACTIVE	DIESALE	Y	0	400	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM741H/883	ACTIVE	TO-99	LMC	8	20	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM741H/883 Q ACO LM741H/883 Q >T	Samples
LM741J/883	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM741J /883 Q ACO /883 Q >T	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and



PACKAGE OPTION ADDENDUM

www.ti.com 17-Jun-2023

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 9-Aug-2022

TUBE



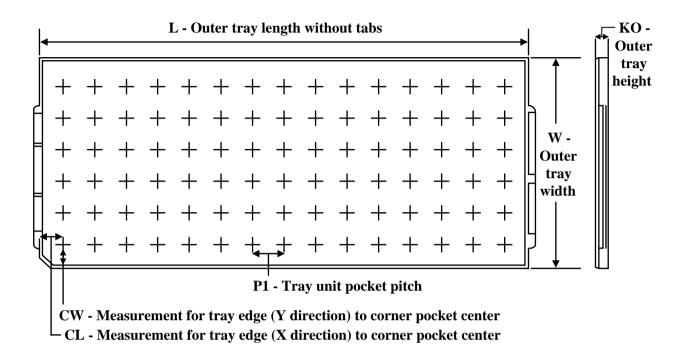
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)	
LM741J/883	NAB	CDIP	8	40	506.98	15.24	13440	NA	



www.ti.com 9-Aug-2022

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	Κ0 (μm)	P1 (mm)	CL (mm)	CW (mm)
LM741H/883	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

LMC (O-MBCY-W8)

METAL CYLINDRICAL PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
- D. Pin numbers shown for reference only. Numbers may not be marked on package.
- E. Falls within JEDEC MO-002/TO-99.





IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2023, Texas Instruments Incorporated