LMC6484QML CMOS Quad Rail-to-Rail Input and Output Operational Amplifier

Check for Samples: LMC6484QML

FEATURES
- (Typical Unless Otherwise Noted)
- Rail-to-Rail Input Common-Mode Voltage Range (Ensured Over Temperature)
- Rail-to-Rail Output Swing (within 20 mV of Supply Rail, 100 KΩ Load)
- Ensured 5V and 15V Performance
- Operates at 3V.
- Excellent CMRR and PSRR: 82 dB
- Ultra Low Input Current: 20 fA
- High Voltage Gain (R_L = 500 KΩ): 130 dB
- Specified for 2 KΩ and 600 Ω Loads

APPLICATIONS
- Data Acquisition Systems
- Transducer Amplifiers
- Hand-Held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC274, TLC279

DESCRIPTION
The LMC6484 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6484 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC274 and TLC279.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6484’s rail-to-rail output swing. The LMC6484’s rail-to-rail output swing is ensured for loads down to 600 Ω.

Ensured low voltage characteristics and low power dissipation make the LMC6484 especially well-suited for battery-operated systems.

See the LMC6482 data sheet for a Dual CMOS operational amplifier with these same features.

Connection Diagram

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
3V Single Supply Buffer Circuit

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.
**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage ((V^+ - V^-))</td>
<td>16V</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>± Supply Voltage</td>
</tr>
<tr>
<td>Voltage at Input/Output Pin ((V^+) + 0.3V, (V^-) - 0.3V)</td>
<td></td>
</tr>
<tr>
<td>Current at Input Pin ((2))</td>
<td>±5 mA</td>
</tr>
<tr>
<td>Current at Output Pin ((3), (4))</td>
<td>±30 mA</td>
</tr>
<tr>
<td>Current at Power Supply Pin</td>
<td>40 mA</td>
</tr>
<tr>
<td>Maximum Junction Temperature (T_{J\text{max}}) ((5), (3))</td>
<td>150°C</td>
</tr>
<tr>
<td>Power Dissipation ((5))</td>
<td>315mW</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C ≤ TA ≤ +150°C</td>
</tr>
<tr>
<td>Thermal Resistance ((6))</td>
<td></td>
</tr>
<tr>
<td>(\theta_{JA}) 14LD CDIP (Still Air)</td>
<td>86.0°C/W</td>
</tr>
<tr>
<td>14LD CDIP (500LF/Min Air Flow)</td>
<td>49.0°C/W</td>
</tr>
<tr>
<td>14LD CLGA (Still Air)</td>
<td>116.0°C/W</td>
</tr>
<tr>
<td>14LD CLGA (500LF/Min Air Flow)</td>
<td>72.0°C/W</td>
</tr>
<tr>
<td>(\theta_{JC}) 14LD CDIP</td>
<td>16.0°C/W</td>
</tr>
<tr>
<td>14LD CLGA</td>
<td>11.0°C/W</td>
</tr>
<tr>
<td>Package Weight</td>
<td></td>
</tr>
<tr>
<td>14LD CDIP</td>
<td>TBD</td>
</tr>
<tr>
<td>14LD CLGA</td>
<td>460mg</td>
</tr>
<tr>
<td>Lead Temp. (Soldering, 10 sec.)</td>
<td>260°C</td>
</tr>
<tr>
<td>ESD Tolerance ((7))</td>
<td>2.0KV</td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

(3) Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

(4) Do not short circuit output to \(V^+\), when \(V^+\) is greater than 13V or reliability will be adversely affected.

(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by \(P_{D\text{max}} = (T_{J\text{max}} - TA)/\theta_{JA}\) or the number given in the Absolute Maximum Ratings, whichever is lower.

(6) All numbers apply for packages soldered directly into a PC board.

(7) Human body model, 1.5 KΩ in series with 100 pF.

**Recommended Operating Range**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>3.0V ≤ (V^+) ≤ 15.5V</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>−55°C ≤ TA ≤ +125°C</td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Table 1. Quality Conformance Inspection Mil-Std-883, Method 5005 - Group A**

<table>
<thead>
<tr>
<th>Subgroup</th>
<th>Description</th>
<th>Temp °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Static tests at</td>
<td>-25</td>
</tr>
<tr>
<td>2</td>
<td>Static tests at</td>
<td>+125</td>
</tr>
<tr>
<td>3</td>
<td>Static tests at</td>
<td>-55</td>
</tr>
<tr>
<td>4</td>
<td>Dynamic tests at</td>
<td>+25</td>
</tr>
<tr>
<td>5</td>
<td>Dynamic tests at</td>
<td>+125</td>
</tr>
</tbody>
</table>
### Table 1. Quality Conformance Inspection Mil-Std-883, Method 5005 - Group A (continued)

<table>
<thead>
<tr>
<th>Subgroup</th>
<th>Description</th>
<th>Temp °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>Dynamic tests at</td>
<td>-55</td>
</tr>
<tr>
<td>7</td>
<td>Functional tests at</td>
<td>+25</td>
</tr>
<tr>
<td>8A</td>
<td>Functional tests at</td>
<td>+125</td>
</tr>
<tr>
<td>8B</td>
<td>Functional tests at</td>
<td>-55</td>
</tr>
<tr>
<td>9</td>
<td>Switching tests at</td>
<td>+25</td>
</tr>
<tr>
<td>10</td>
<td>Switching tests at</td>
<td>+125</td>
</tr>
<tr>
<td>11</td>
<td>Switching tests at</td>
<td>-55</td>
</tr>
<tr>
<td>12</td>
<td>Settling time at</td>
<td>+25</td>
</tr>
<tr>
<td>13</td>
<td>Settling time at</td>
<td>+125</td>
</tr>
<tr>
<td>14</td>
<td>Settling time at</td>
<td>-55</td>
</tr>
</tbody>
</table>

### LMC6484 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. \( V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2 \) and \( R_L > 1M \).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Notes</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Subgroups</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IO} )</td>
<td>Input Offset Voltage</td>
<td>( 0V \leq V_{CM} \leq 15.0V )</td>
<td></td>
<td>0.75</td>
<td>mV</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = 15V )</td>
<td></td>
<td>1.35</td>
<td>mV</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td>( I_{IB} )</td>
<td>Input Bias Current</td>
<td>( 0V \leq V_{CM} \leq 5.0V )</td>
<td></td>
<td>25</td>
<td>pA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>( I_{IO} )</td>
<td>Input Offset Current</td>
<td>( 0V \leq V_{CM} \leq 15.0V )</td>
<td></td>
<td>100</td>
<td>pA</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = 15V )</td>
<td></td>
<td>25</td>
<td>pA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = 15V )</td>
<td></td>
<td>100</td>
<td>pA</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>( 0V \leq V_{CM} \leq 5.0V )</td>
<td></td>
<td>65</td>
<td>dB</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>+PSRR</td>
<td>Positive Power Supply Rejection Ratio</td>
<td>( 5V \leq V^+ \leq 15V )</td>
<td></td>
<td>62</td>
<td>dB</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_O = 2.5V )</td>
<td></td>
<td>65</td>
<td>dB</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td>-PSRR</td>
<td>Negative Power Supply Rejection Ratio</td>
<td>(-15V \leq V^+ \leq -5V )</td>
<td></td>
<td>62</td>
<td>dB</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_O = -2.5V ), ( V^+ = 0V )</td>
<td></td>
<td>65</td>
<td>dB</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td>( V_{CM} )</td>
<td>Input Common Mode Voltage Range</td>
<td>( 5V \leq V_{CM} \leq 15V )</td>
<td></td>
<td>62</td>
<td>dB</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>For CMRR \geq 50dB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = 0.25 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^- = 0.25 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = 0.0 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^- = 0.0 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISCC</td>
<td>Output Short Circuit Current</td>
<td>Sourcing, ( V_O = 0V )</td>
<td></td>
<td>16</td>
<td>mA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking, ( V_O = 5V )</td>
<td></td>
<td>12</td>
<td>mA</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = 15V )</td>
<td></td>
<td>11</td>
<td>mA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = 15V )</td>
<td></td>
<td>9.0</td>
<td>mA</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sourcing, ( V_O = 0V )</td>
<td></td>
<td>28</td>
<td>mA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking, ( V_O = 12V )</td>
<td></td>
<td>22</td>
<td>mA</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = 15V )</td>
<td></td>
<td>30</td>
<td>mA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = 15V )</td>
<td></td>
<td>24</td>
<td>mA</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>All four Amps</td>
<td></td>
<td>2.8</td>
<td>mA</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>All four Amps</td>
<td></td>
<td>3.6</td>
<td>mA</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = +15V )</td>
<td></td>
<td>3.0</td>
<td>mA</td>
<td>2, 3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = +15V )</td>
<td></td>
<td>4.0</td>
<td>mA</td>
<td>2, 3</td>
<td></td>
</tr>
</tbody>
</table>

(1) Do not short circuit output to \( V^+ \); when \( V^+ \) is greater than 13V or reliability will be adversely affected.
### LMC6484 Electrical Characteristics DC Parameters (continued)

The following conditions apply, unless otherwise specified. \( V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+ / 2 \) and \( R_L > 1M \).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Notes</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Sub-grps</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_O )</td>
<td>Output Swing</td>
<td>( V^+ = 5V ) ( R_L = 2\Omega ) to ( V^+ / 2 )</td>
<td></td>
<td>4.8</td>
<td>0.18</td>
<td>V</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = 5V ) ( R_L = 600\Omega ) to ( V^+ / 2 )</td>
<td></td>
<td>4.24</td>
<td>0.65</td>
<td>V</td>
<td>5, 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = 15V ) ( R_L = 2\Omega ) to ( V^+ / 2 )</td>
<td></td>
<td>14.4</td>
<td>0.32</td>
<td>V</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = 15V ) ( R_L = 600\Omega ) to ( V^+ / 2 )</td>
<td></td>
<td>13.4</td>
<td>1.00</td>
<td>V</td>
<td>4</td>
</tr>
<tr>
<td>( A_V )</td>
<td>Large Signal Voltage Gain</td>
<td>( R_L = 2\Omega ) Sourcing</td>
<td>(2)</td>
<td>140</td>
<td>V/mV</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 600\Omega ) Sourcing</td>
<td>(2)</td>
<td>80</td>
<td>V/mV</td>
<td>5, 6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 2\Omega ) Sinking</td>
<td>(2)</td>
<td>35</td>
<td>V/mV</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 600\Omega ) Sinking</td>
<td>(2)</td>
<td>48</td>
<td>V/mV</td>
<td>5, 6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 600\Omega ) Sinking</td>
<td>(2)</td>
<td>18</td>
<td>V/mV</td>
<td>4</td>
<td></td>
</tr>
</tbody>
</table>

(2) \( V^+ = 15V, V_{CM} = 7.5V \) and \( R_L \) connected to 7.5V. For Sourcing tests, \( 7.5V \leq V_O \leq 11.5V \). For Sinking tests, \( 3.5V \leq V_O \leq 7.5V \).

### LMC6484 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified. \( V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+ / 2 \) and \( R_L > 1M \).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Notes</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Sub-grps</th>
</tr>
</thead>
<tbody>
<tr>
<td>( SR )</td>
<td>Slew Rate</td>
<td></td>
<td>(1)</td>
<td>0.9</td>
<td>V/\mu S</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.6</td>
<td>V/\mu S</td>
<td>5, 6</td>
<td></td>
</tr>
<tr>
<td>( GBW )</td>
<td>Gain Bandwidth</td>
<td>( V^+ = 15V ) Set up for non-inverting</td>
<td></td>
<td>1.25</td>
<td>MHz</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.15</td>
<td>MHz</td>
<td>5, 6</td>
<td></td>
</tr>
</tbody>
</table>

(1) \( V^+ = 15V \). Connected as Voltage Follower with 10V step input, 2.5V to 12.5V for +slew, and 12.5V to 2.5V for −slew. Number specified is the slower of either the positive or negative slew rates.
Typical Performance Characteristics

\( V_S = +15 \text{V}, \text{Single Supply, } T_A = 25^\circ C \) unless otherwise specified

**Supply Current vs. Supply Voltage**

![Figure 4](image)

**Input Current vs. Temperature**

![Figure 5](image)

**Source Current vs. Output Voltage**

\( V_S = 15 \text{V} \)

![Figure 6](image)

**Sink Current vs. Output Voltage**

\( V_S = 15 \text{V} \)

![Figure 9](image)
Typical Performance Characteristics (continued)

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified

**Sinking Current vs. Output Voltage**

![Sinking Current vs. Output Voltage](image)

Output Voltage Referenced to GND (V)

*Figure 10.*

**Sinking Current vs. Output Voltage**

![Sinking Current vs. Output Voltage](image)

Output Voltage Referenced to GND (V)

*Figure 11.*

**Output Voltage Swing vs. Supply Voltage**

![Output Voltage Swing vs. Supply Voltage](image)

Supply Voltage (V)

*Figure 12.*

**Input Voltage Noise vs. Frequency**

![Input Voltage Noise vs. Frequency](image)

Frequency (Hz)

*Figure 13.*

**Input Voltage Noise vs. Input Voltage**

![Input Voltage Noise vs. Input Voltage](image)

Common Mode Input Voltage (V)

*Figure 14.*

**Input Voltage Noise vs. Input Voltage**

![Input Voltage Noise vs. Input Voltage](image)

Common Mode Input Voltage (V)

*Figure 15.*
Typical Performance Characteristics (continued)

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified

**Input Voltage Noise vs. Input Voltage**

![Graph showing Input Voltage Noise vs. Input Voltage](image1)

**Figure 16.**

**Crosstalk Rejection vs. Frequency**

![Graph showing Crosstalk Rejection vs. Frequency](image2)

**Figure 17.**

**Positive PSRR vs. Frequency**

![Graph showing Positive PSRR vs. Frequency](image3)

**Figure 18.**

**Negative PSRR vs. Frequency**

![Graph showing Negative PSRR vs. Frequency](image4)

**Figure 19.**

**CMRR vs. Frequency**

![Graph showing CMRR vs. Frequency](image5)

**Figure 20.**
Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

**Figure 22.**
CMRR vs. Input Voltage

**Figure 23.**
CMRR vs. Input Voltage

**Figure 24.**
CMRR vs. Input Voltage

**Figure 25.**
ΔV_Os vs. CMR

**Figure 26.**
ΔV_Os vs. CMR

**Figure 27.**
Input Voltage vs. Output Voltage
Typical Performance Characteristics (continued)

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified

**Input Voltage vs. Output Voltage**

![Input Voltage vs. Output Voltage Graph](image)

**Open Loop Frequency Response**

![Open Loop Frequency Response Graph](image)

**Open Loop Frequency Response vs. Temperature**

![Open Loop Frequency Response vs. Temperature Graph](image)

**Maximum Output Swing vs. Frequency**

![Maximum Output Swing vs. Frequency Graph](image)

**Gain and Phase vs. Capacitive Load**

![Gain and Phase vs. Capacitive Load Graph](image)
**Typical Performance Characteristics (continued)**

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified

### Gain and Phase vs. Capacitive Load

<table>
<thead>
<tr>
<th>Capacitive Load</th>
<th>Frequency (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_L = 0$</td>
<td>10k</td>
</tr>
<tr>
<td>$C_L = 500 \text{pF}$</td>
<td>100k</td>
</tr>
<tr>
<td>$C_L = 1000 \text{pF}$</td>
<td>1M</td>
</tr>
</tbody>
</table>

**Figure 34.**

### Open Loop Output Impedance vs. Frequency

**Figure 35.**

### Slew Rate vs. Supply Voltage

**Figure 37.**

### Non-Inverting Large Signal Pulse Response

**Figure 36.**

### Non-Inverting Large Signal Pulse Response

**Figure 38.**
Typical Performance Characteristics (continued)

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified

Non-Inverting Large Signal Pulse Response

Non-Inverting Small Signal Pulse Response

Inverting Large Signal Pulse Response

Inverting Small Signal Pulse Response

Figure 40.

Figure 41.

Figure 42.

Figure 43.

Figure 44.

Figure 45.
Typical Performance Characteristics (continued)

$V_S = +15V$, Single Supply, $T_A = 25°C$ unless otherwise specified

**Inverting Large Signal Pulse Response**

![Inverting Large Signal Pulse Response](image)

**Inverting Small Signal Pulse Response**

![Inverting Small Signal Pulse Response](image)

**Stability vs. Capacitive Load**

![Stability vs. Capacitive Load](image)
Typical Performance Characteristics (continued)

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified

**Stability vs. Capacitive Load**

*Figure 52.*

*Figure 53.*

*Figure 54.*

*Figure 55.*
APPLICATION INFORMATION

AMPLIFIER TOPOLOGY

The LMC6484 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, cross-over distortion, and open-loop gain variation.

The LMC6484’s input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

INPUT COMMON-MODE VOLTAGE RANGE

Unlike Bi-FET amplifier designs, the LMC6484 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 56 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

Figure 56. An Input Voltage Signal Exceeds the LMC6484 Power Supply Voltages with No Output Phase Inversion

The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 57, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

Figure 57. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in Figure 58 Causing No Phase Inversion Due to $R_I$

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor as shown in Figure 58.

Figure 58. $R_I$ Input Current Protection for Voltages Exceeding the Supply Voltage
RAIL-TO-RAIL OUTPUT

The approximated output resistance of the LMC6484 is 180\(\Omega\) sourcing and 130\(\Omega\) sinking at \(V_S = 3V\) and 110\(\Omega\) sourcing and 83\(\Omega\) sinking at \(V_S = 5V\). Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

CAPACITIVE LOAD TOLERANCE

The LMC6484 can typically directly drive a 100 pF load with \(V_S = 15V\) at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 59. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

![Figure 59. Resistive Isolation of a 330 pF Capacitive Load](image)

![Figure 60. Pulse Response of the LMC6484 Circuit in Figure 59](image)

Improved frequency response is achieved by indirectly driving capacitive loads as shown in Figure 61.

![Figure 61. LMC6484 Non-Inverting Amplifier, Compensated to Handle a 330 pF Capacitive Load](image)

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response can be seen in Figure 62.
COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6484. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 63), $C_f$, is first estimated by:

$$\frac{1}{2\pi R_1 C_{in}} \geq \frac{1}{2\pi R_2 C_t}$$

(1)

or

$$R_1 C_t \leq R_2 C_t$$

(2)

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for $C_f$ may be different. The values of $C_t$ should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. when one wishes to take advantage of the ultra-low input current of the LMC6484, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6484's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 64. To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6484's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figure 67 for typical connections of guard rings for standard op-amp configurations.

Figure 64. Example of Guard Ring in P.C. Board Layout

![Figure 64](image)

Figure 65. Inverting Amplifier

![Figure 65](image)

Figure 66. Non-Inverting Amplifier

![Figure 66](image)
The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 68.

![Figure 68. Air Wiring](Image)

**OFFSET VOLTAGE ADJUSTMENT**

Offset voltage adjustment circuits are illustrated in Figure 70 Figure 71. Large value resistances and potentiometers are used to reduce power consumption while providing typically \( \pm 2.5 \) mV of adjustment range, referred to the input, for both configurations with \( V_S = \pm 5V \).

![Figure 69. Inverting Configuration Offset Voltage Adjustment](Image)

![Figure 70. Non-Inverting Configuration Offset Voltage Adjustment](Image)
UPGRADING APPLICATIONS

The LMC6484 quads and LMC6482 duals have industry standard pin outs to retrofit existing applications. System performance can be greatly increased by the LMC6484’s features. The key benefit of designing in the LMC6484 is increased linear signal range. Most op-amps have limited input common mode ranges. Signals that exceed this range generate a non-linear output response that persists long after the input signal returns to the common mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common mode ranges resulting in output phase inversion or severe distortion.

DATA ACQUISITION SYSTEMS

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6484 (Figure 71). Capable of using the full supply range, the LMC6484 does not require input signals to be scaled down to meet limited common mode voltage ranges. The LMC6484 CMRR of 82 dB maintains integral linearity of a 12-bit data acquisition system to ±0.325 LSB. Other rail-to-rail input amplifiers with only 50 dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.

![Figure 71. Operating from the same Supply Voltage, the LMC6484 buffers the ADC12038 maintaining excellent accuracy](image)

INSTRUMENTATION CIRCUITS

The LMC6484 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6484 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6484 an excellent choice for noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with Rg to set the differential gain of the 3 op-amp instrumentation circuit in Figure 72. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.
A 2 op-amp instrumentation amplifier designed for a gain of 100 is shown in Figure 73. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

**SPICE MACROMODEL**

A spice macromodel is available for the LMC6484. This model includes accurate simulation of:

- input common-mode voltage range
- frequency and transient response
- GBW dependence on loading conditions
- quiescent and dynamic supply current
- output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact your local Texas Instruments sales office to obtain an operational amplifier spice model library disk.
Typical Single-Supply Applications

Figure 74. Half-Wave Rectifier with Input Current Protection (R_I)

![Half-Wave Rectifier Waveform](image)

Figure 75. Half-Wave Rectifier Waveform

The circuit in Figure 74 uses a single supply to half wave rectify a sinusoid centered about ground. R_I limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in Figure 76.

Figure 76. Full Wave Rectifier with Input Current Protection (R_I)
Figure 77. Full Wave Rectifier Waveform

Figure 78. Large Compliance Range Current Source

Figure 79. Positive Supply Current Sense

Figure 80. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range
In Figure 80 dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of $C_H$ and diode leakage current. The ultra-low input current of the LMC6484 has a negligible effect on droop.

![Figure 81. Rail-to-Rail Sample and Hold](image)

The LMC6484’s high CMRR (85 dB) allows excellent accuracy throughout the circuit’s rail-to-rail dynamic capture range.

![Figure 82. Rail-to-Rail Single Supply Low Pass Filter](image)

The low pass filter circuit in Figure 82 can be used as an anti-aliasing filter with the same voltage supply as the A/D converter.

Filter designs can also take advantage of the LMC6484 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.
Table 2. Revision History

<table>
<thead>
<tr>
<th>Released</th>
<th>Revision</th>
<th>Section</th>
<th>Changes</th>
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<tr>
<td>10/26/2010</td>
<td>A</td>
<td>New Release, Corporate format</td>
<td>1 MDS data sheet converted into one Corp. data sheet format. The drift table was eliminated from the 883 section since it did not apply; MNLMC6484AM-X Rev 1A2 will be archived.</td>
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<tr>
<td>03/27/2013</td>
<td>A</td>
<td>All</td>
<td>Changed layout of National Data Sheet to TI format.</td>
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## PACKAGING INFORMATION

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<th>Package</th>
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<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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</thead>
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<td>CDIP</td>
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<td>Samples</td>
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<td>-55 to 125</td>
<td>LMC6484AMJ/883</td>
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<tr>
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<td>Call TI</td>
<td>-55 to 125</td>
<td>LMC6484AMWG/883</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. This package is hermetically sealed with a ceramic lid using glass frit.

4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

EXAMPLE BOARD LAYOUT

LAND PATTERNS EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

DETAIL A
SCALE: 15X

SOLDER MASK OPENING

METAL

DETAL B
13X, SCALE: 15X

SOLDER MASK OPENING

METAL

.002 MAX
[0.05]
ALL AROUND

(R.002 ) TYP
[0.05]

(0.063)
[1.6]

(0.300 ) TYP
[7.62]

SEE DETAIL A

SEE DETAIL B

SYMM

SYMM
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