1 Features
- Input Range: ±15 pF
- Measurement Resolution: 0.5 fF
- Maximum Offset Capacitance: 100 pF
- Programmable Output Rates: 100/200/400 S/s
- Maximum Shield Load: 400 pF
- Supply Voltage: 3.3 V
- Temp Range: –40 to 85°C
- Current Consumption:
  - Active: 750 µA
  - Standby: 29 µA
- Interface: I²C
- Number of Channels: 4

2 Applications
- Proximity Wake-up
- Gesture Sensing
- Automotive Door / Kick Sensors
- Automotive Rain Sensor
- Remote and Direct Liquid Level Sensing
- High-resolution Metal Profiling
- Rain / Fog / Ice / Snow Detection
- Material Size Detection
- Material Stack Height

3 Description
Capacitive sensing with grounded capacitor sensors is a very low-power, low-cost, high-resolution contactless sensing technique that can be applied to a variety of applications ranging from proximity detection and gesture sensing to material analysis and remote liquid level sensing. The sensor in a capacitive sensing system is any metal or conductor, allowing for low cost and highly flexible system design.

The FDC1004 is a high-resolution, 4-channel capacitance-to-digital converter for implementing capacitive sensing solutions. Each channel has a full scale range of ±15 pF and can handle a sensor offset capacitance of up to 100 pF, which can be either programmed internally or can be an external capacitor for tracking environmental changes over time and temperature. The large offset capacitance capability allows for the use of remote sensors.

The FDC1004 also includes shield drivers for sensor shields, which can reduce EMI interference and help focus the sensing direction of a capacitive sensor. The small footprint of the FDC1004 allows for use in space-constrained applications. The FDC1004 is available in a 10-pin WSON package and features an I²C interface for interfacing to an MCU.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDC1004</td>
<td>WSON</td>
<td>3.0 mm x 3.0 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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5 Revision History

Changes from Original (August 2014) to Revision A

• Added Parameter not tested in production ............................. 5
• Changed CINx to CINn throughout ................................... 9
• Added note for Applications and Implementation section. .................. 19

Submit Documentation Feedback

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Product Folder Links: FDC1004
## 6 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>NO.</th>
<th>TYPE&lt;sup&gt;(1)&lt;/sup&gt;</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>SHLD1</td>
<td>1</td>
<td>A</td>
<td>Capacitive Input Active AC Shielding.</td>
</tr>
<tr>
<td>CIN1</td>
<td>2</td>
<td>A</td>
<td>Capacitive Input. The measured capacitance is connected between the CIN1 pin and GND. If not used, this pin should be left as an open circuit.</td>
</tr>
<tr>
<td>CIN2</td>
<td>3</td>
<td>A</td>
<td>Capacitive Input. The measured capacitance is connected between the CIN2 pin and GND. If not used, this pin should be left as an open circuit.</td>
</tr>
<tr>
<td>CIN3</td>
<td>4</td>
<td>A</td>
<td>Capacitive Input. The measured capacitance is connected between the CIN3 pin and GND. If not used, this pin should be left as an open circuit.</td>
</tr>
<tr>
<td>CIN4</td>
<td>5</td>
<td>A</td>
<td>Capacitive Input. The measured capacitance is connected between the CIN4 pin and GND. If not used, this pin should be left as an open circuit.</td>
</tr>
<tr>
<td>SHLD2</td>
<td>6</td>
<td>A</td>
<td>Capacitive Input Active AC Shielding.</td>
</tr>
<tr>
<td>GND</td>
<td>7</td>
<td>G</td>
<td>Ground</td>
</tr>
<tr>
<td>VDD</td>
<td>8</td>
<td>P</td>
<td>Power Supply Voltage. This pin should be decoupled to GND, using a low impedance capacitor, for example in combination with a 1-μF tantalum and a 0.1-μF multilayer ceramic.</td>
</tr>
<tr>
<td>SCL</td>
<td>9</td>
<td>I</td>
<td>Serial Interface Clock Input. Connects to the master clock line. Requires pull-up resistor if not already provided elsewhere in the system.</td>
</tr>
<tr>
<td>SDA</td>
<td>10</td>
<td>I/O</td>
<td>Serial Interface Bidirectional Data. Connects to the master data line. Requires a pull-up resistor if not provided elsewhere in the system.</td>
</tr>
<tr>
<td>DAP&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>-</td>
<td>N/A</td>
<td>Connect to GND</td>
</tr>
</tbody>
</table>

<sup>(1) P=Power, G=Ground, I=Input, O=Output, A=Analog</sup>

<sup>(2) There is an internal electrical connection between the exposed Die Attach Pad (DAP) and the GND pin of the device. Although the DAP can be left floating, for best performance the DAP should be connected to the same potential as the device's GND pin. Do not use the DAP as the primary ground for the device. The device GND pin must always be connected to ground.</sup>
7 Specifications

7.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>$-0.3$</td>
<td>6 V</td>
</tr>
<tr>
<td>SCL, SDA</td>
<td>$-0.3$</td>
<td>6 V</td>
</tr>
<tr>
<td>at any other pin</td>
<td>$-0.3$</td>
<td>VDD+0.3 V</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{θJA}$, and the ambient temperature, $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A) / R_{θJA}$. All numbers apply for packages soldered directly onto a PC board.

7.2 Handling Ratings

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{STG}$</td>
<td>Storage Temperature</td>
<td>$-65$</td>
</tr>
<tr>
<td>$V_{(ESD)}$</td>
<td>Electrostatic discharge</td>
<td>$-1000$</td>
</tr>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins</td>
<td>$-1000$</td>
<td>1000 V</td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification -500 500 JESD22-C101, all pins</td>
<td>$-250$</td>
<td>250 V</td>
</tr>
</tbody>
</table>

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (VDD-GND)</td>
<td>3</td>
<td>3.3</td>
<td>3.6 V</td>
</tr>
<tr>
<td>Temperature</td>
<td>$-40$</td>
<td>85 °C</td>
<td></td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>FDC1004</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{θJA}$</td>
<td>Junction-to-ambient thermal resistance</td>
<td>46.8</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
7.5 Electrical Characteristics

Over recommended operating temperature range, \( V_{DD} = 3.3 \text{ V} \), for \( T_A = 25^\circ \text{C} \) (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>POWER SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{DD} )</td>
<td>Supply current Conversion mode; Digital input to VDD or GND</td>
<td>750</td>
<td>950</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Standby; Digital input to VDD or GND</td>
<td>29</td>
<td>70</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>CAPACITIVE INPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( ICR )</td>
<td>Input conversion range</td>
<td>±15</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( C_{OMAX} )</td>
<td>Max input offset capacitance per channel, Series resistance at ( C_{INn} = 1.4 \Omega )</td>
<td>100</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>RES</td>
<td>Effective resolution (^{(1)}) Sample rate = 100S/s (^{(2)})</td>
<td>16</td>
<td>bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ERR</td>
<td>Absolute error after offset calibration</td>
<td>±6</td>
<td>F</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( TcC_{OFF} )</td>
<td>Offset deviation over temperature (-40^\circ \text{C} &lt; T &lt; 85^\circ \text{C} )</td>
<td>30</td>
<td>IF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( G_{ERR} )</td>
<td>Gain error</td>
<td>0.07</td>
<td>% of FS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( tG )</td>
<td>Gain drift vs. temperature (-40^\circ \text{C} &lt; T &lt; 85^\circ \text{C} )</td>
<td>2.1</td>
<td>ppm of FSR/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>DC power supply rejection 3 V &lt; ( V_{DD} &lt; 3.6 \text{ V} )</td>
<td>11</td>
<td>IF/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CAPDAC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( FR_{CAPDAC} )</td>
<td>Full-scale range</td>
<td>96.875</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( RES_{CAPDAC} )</td>
<td>Resolution</td>
<td>5</td>
<td>bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( TcC_{OFF, CAPDAC} )</td>
<td>Offset drift vs. temperature (-40^\circ \text{C} &lt; T &lt; 85^\circ \text{C} )</td>
<td>1</td>
<td>ppm of FSR/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EXCITATION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f )</td>
<td>Frequency</td>
<td>25</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{AC} )</td>
<td>AC voltage across capacitance</td>
<td>2.4</td>
<td>Vpp</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{DC} )</td>
<td>Average DC voltage across capacitance</td>
<td>1.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHIELD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( DRV )</td>
<td>Driver capability ( f = 25 \text{ kHz}, \text{SHLDn to GND, } n = 1.2 )</td>
<td>400</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Effective resolution is the ratio of converter full scale range to RMS measurement noise.

\(^{(2)}\) No external capacitance connected.

7.6 I²C Interface Voltage Level

Over recommended operating free-air temperature range, \( V_{DD} = 3.3 \text{ V} \), for \( T_A = T_J = 25^\circ \text{C} \) (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IH} )</td>
<td>Input high voltage</td>
<td>0.7*( V_{DD} )</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Input low voltage</td>
<td>0.3*( V_{DD} )</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output low voltage</td>
<td>Sink current 3 mA</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( HYS )</td>
<td>Hysteresis (^{(1)})</td>
<td>0.1*( V_{DD} )</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) This parameter is specified by design and/or characterization and is not tested in production.
7.7 I²C Interface Timing

Over recommended operating free-air temperature range, \( V_{DD} = 3.3 \) V, for \( T_A = T_J = 25^\circ C \) (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{SCL} )</td>
<td>Clock frequency(^{(1)})</td>
<td>10</td>
<td>400</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>( t_{LOW} )</td>
<td>Clock low time(^{(1)})</td>
<td>1.3</td>
<td></td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>( t_{HIGH} )</td>
<td>Clock high time(^{(1)})</td>
<td>0.6</td>
<td></td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>( t_{HD;STA} )</td>
<td>Hold time (repeated) START condition(^{(1)})</td>
<td>After this period, the first clock pulse is generated</td>
<td>0.6</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>( t_{SU;STA} )</td>
<td>Set-up time for a repeated START condition(^{(1)})</td>
<td></td>
<td>0.6</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>( t_{HD;DAT} )</td>
<td>Data hold time(^{(1)}(2))</td>
<td></td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{SU;DAT} )</td>
<td>Data setup time(^{(1)})</td>
<td></td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_F )</td>
<td>SDA fall time(^{(1)})</td>
<td></td>
<td></td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{SU;STO} )</td>
<td>Set-up time for STOP condition(^{(1)})</td>
<td></td>
<td>0.6</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>( t_{BUF} )</td>
<td>Bus free time between a STOP and START condition(^{(1)})</td>
<td></td>
<td>1.3</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>( t_{VD;DAT} )</td>
<td>Data valid time(^{(1)})</td>
<td></td>
<td></td>
<td>0.9</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{VD;ACK} )</td>
<td>Data valid acknowledge time(^{(1)})</td>
<td></td>
<td>0.9</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{SP} )</td>
<td>Pulse width of spikes that must be suppressed by the input filter(^{(1)})</td>
<td></td>
<td></td>
<td>50</td>
<td>ns</td>
</tr>
</tbody>
</table>

\(^{(1)}\) This parameter is specified by design and/or characterization and is not tested in production.

\(^{(2)}\) The FDC1004 provides an internal 300 ns minimum hold time to bridge the undefined region of the falling edge of SCL.

---

**Figure 1. I²C Timing**
7.8 Typical Characteristics

Figure 2. Active Conversion Mode Supply Current vs. Temperature

Gain Drift vs. Temperature

CINn = 10 pF  n = 1...4

Figure 3. Stand-by Mode Supply Current vs. Temperature

Offset Drift vs. Temperature

CINn = open  n = 1...4

Figure 4. Frequency Response 100S/s

Figure 5. Frequency Response 200S/s
Figure 8. Frequency Response 400S/s
8 Detailed Description

8.1 Overview
The FDC1004 is a high-resolution, 4-channel capacitance-to-digital converter for implementing capacitive sensing solutions. Each channel has a full scale range of ±15 pF and can handle a sensor offset capacitance of up to 100 pF, which can be either programmed internally or can be an external capacitor for tracking environmental changes over time and temperature. The large offset capacitance capability allows for the use of remote sensors. The FDC1004 also includes shield drivers for sensor shields, which can reduce EMI interference and help focus the sensing direction of a capacitive sensor. The small footprint of the FDC1004 allows for use in space-constrained applications.

8.2 Functional Block Diagram

8.3 Feature Description

8.3.1 The Shield
The FDC1004 measures capacitance between CINn and ground. That means any capacitance to ground on signal path between the FDC1004 CINn pins and sensor is included in the FDC1004 conversion result.

In some applications, the parasitic capacitance of the sensor connections can be larger than the capacitance of the sensor. If that parasitic capacitance is stable, it can be treated as a constant capacitive offset. However, the parasitic capacitance of the sensor connections can have significant variation due to environmental changes (such as mechanical movement, temperature shifts, humidity changes). These changes are seen as drift in the conversion result and may significantly compromise the system accuracy.

To eliminate the CINn parasitic capacitance to ground, the FDC1004 SHLDx signals can be used for shielding the connection between the sensor and CINn. The SHLDx output is the same signal waveform as the excitation of the CINn pin; the SHLDx is driven to the same voltage potential as the CINn pin. Therefore, there is no current between CINn and SHLDx pins, and any capacitance between these pins does not affect the CINn charge transfer. Ideally, the CINn to SHLD capacitance does not have any contribution to the FDC1004 result.

In differential measurements, SHLD1 is assigned to Cn and SHLD2 is assigned to Cm, where n < m. For instance in the measurement CIN2 – CIN1, where CHA = CIN2 and CHB = CIN1 (see Table 4), SHDL1 is assigned to CIN1 and SHDL2 is assigned to CIN2.
Feature Description (continued)

In a single ended configuration, such as CINn vs. GND, SHLD1 is internally shorted to SHLD2. In a single ended configuration, such as CINn vs. GND with CAPDAC enabled, SHLD1 is assigned to the selected channel, SHLD2 is floating.

For best results, locate the FDC1004 as close as possible to the capacitive sensor. Minimize the connection length between the sensor and FDC1004 CINn pins and between the sensor ground and the FDC1004 GND pin. Shield the PCB traces to the CINn pins and connect the shielding to the FDC1004 SHLDx pins. In addition, if a shielded cable is used to connect the FDC1004 to the sensor, the shield should be connected to the appropriate SHLDx pin.

In applications where only one SHLDx pin is used, the unused SHLDx pin can be left unconnected.

8.3.2 The CAPDAC

The FDC1004 full-scale input range is ±15 pF. The part can accept a higher capacitance on the input and the common-mode or offset (constant component) capacitance can be balanced by the programmable on-chip CAPDACs. The CAPDAC can be viewed as a negative capacitance connected internally to the CINn pin. The relation between the input capacitance and output data can be expressed as \( \text{DATA} = (C_{\text{INn}} - \text{CAPDAC}) \).

The CAPDACs have a 5-bit resolution, monotonic transfer function, are well matched to each other, and have a defined temperature coefficient.

8.3.3 Capacitive System Offset Calibration

The capacitive offset can be due to many factors including the initial capacitance of the sensor, parasitic capacitances of board traces, and the capacitance of any other connections between the sensor and the FDC.

The parasitic capacitances of the FDC1004 are calibrated out at production. If there are other sources of offset in the system, it may be necessary to calibrate the system capacitance offset in the application. Any offset in the capacitance input larger than ½ LSB of the CAPDAC should first be removed using the on-chip CAPDACs. Any residual offset of approximately 1 pF can then be removed by using the capacitance offset calibration register. The offset calibration register is reloaded by the default value at power-on or after reset. Therefore, if the offset calibration is not repeated after each system power-up, the calibration coefficient value should be stored by the host controller and reloaded as part of the FDC1004 setup.

8.3.4 Capacitive Gain Calibration

The gain is factory calibrated up to ±15 pF in the production for each part individually. The factory gain coefficient is stored in a one-time programmable (OTP) memory.

The gain can be temporarily changed by setting the Gain Calibration Register (registers 0x11 to 0x14) for the appropriate CINn pin, although the factory gain coefficient will be restored after power-up or reset.

The part is tested and specified for use only with the default factory calibration coefficient. Adjusting the Gain calibration can be used to normalize the capacitance measurement of the CINn input channels.

8.4 Device Functional Modes

8.4.1 Single Ended Measurement

The FDC1004 can be used for interfacing to a single-ended capacitive sensor. In this configuration the sensor should be connected to the input CINn (n = 1..4) pins of the FDC1004 and GND. The capacitance-to-digital convertor (without using the CAPDAC, \( \text{CAPDAC} = 0\text{pF} \)) measures the positive (or the negative) input capacitance in the range of 0 pF to 15 pF. The CAPDAC can be used for programmable shifting of the input range. In this case it is possible to measure input capacitance in the range of 0 pF to ±15 pF which are on top of an offset capacitance up to 100 pF. In single ended measurements with CAPDAC disabled SHLD1 is internally shorted to SHLD2 (see Figure 9); if CAPDAC is enabled SHLD2 is floating (see Figure 10). The single ended mode is enabled when the CHB register of the Measurements configuration registers (see Table 4) are set to b100 or b111.
Device Functional Modes (continued)

Figure 9. Single-Ended Configuration with CAPDAC Disabled

Figure 10. Single-Ended Configuration with CAPDAC Enabled

8.4.2 Differential Measurement

When the FDC1004 is used for interfacing to a differential capacitive sensor, each of the two input capacitances must be less than 115 pF. In this configuration the CAPDAC is disabled. The absolute value of the difference between the two input capacitances should be kept below 15 pF to avoid introducing errors in the measurement. In differential measurements, SHLD1 is assigned to CHn and SHLD2 is assigned to CHm, where n < m. For instance in the measurement CIN2 – CIN1, where CHA = CIN2 and CHB = CIN1 (see Table 4), SHDL1 is
Device Functional Modes (continued)

assigned to CIN1 and SHDL2 is to CIN2. In the picture below a couple of differential sensors made with S1 versus S3 and S2 versus S4 is shown. S1 and S2 are alternatively connected to CHA and the S3 and S4 are alternatively connected to CHB, the shield signals are connected as explained in previous paragraph. The FDC1004 will perform a differential measurement when CHB field of the Measurements Configuration Registers (refer to Table 4) is less than to b100.

This configuration is very useful in applications where environment conditions need to be tracked. The differential measurement between the main electrode and the environment electrode makes the measurement independent of the environment conditions.

8.5 Programming

The FDC1004 operates only as a slave device on the two-wire bus interface. Every device on the bus must have a unique address. Connection to the bus is made via the open-drain I/O lines, SDA, and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The FDC1004 supports fast mode frequencies 10 kHz to 400 kHz. All data bytes are transmitted MSB first.

8.5.1 Serial Bus Address

To communicate with the FDC1004, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits and a direction bit that indicates the intent to execute a read or write operation. The seven bit address for the FDC1004 is (MSB first): b101 0000.

8.5.2 Read/Write Operations

Access a particular register on the FDC1004 by writing the appropriate value to the Pointer Register. The pointer value is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the FDC1004 requires a value for the pointer register. When reading from the FDC1004, the last value stored in the pointer by a write operation is used to determine which register is read by a read operation. To change the pointer register for a read operation, a new value must be written to the pointer. This transaction is accomplished by issuing the slave address byte with the R/W bit low, followed by the pointer byte. No additional data is
Programming (continued)

required. The master can then generate a START condition and send the slave address byte with the R/W bit high to initiate the read command. Note that register bytes are sent MSB first, followed by the LSB. A write operation in a read only registers such as MANUFACTURER ID or SERIAL ID returns a NACK after each data byte; read/write operation to unused address returns a NACK after the pointer; a read/write operation with incorrect I\(_2\)C address returns a NACK after the I\(_2\)C address.

8.5.3 Device Usage

The basic usage model of the FDC1004 is to simply follow these steps:

1. Configure measurements (for details, refer to Measurement Configuration).
2. Trigger a measurement set (for details, refer to Triggering Measurements).
3. Wait for measurement completion (for details, refer to Wait for Measurement Completion).
4. Read measurement data (for details, refer to Read of Measurement Result).

8.5.3.1 Measurement Configuration

Configuring a measurement involves setting the input channels and the type of measurement (single-ended or differential).

The FDC1004 can be configured with up to 4 separate measurements, where each measurement can be any valid configuration (that is, a specific channel can be used in multiple measurements). There is a dedicated configuration register for each of the 4 possible measurements (e.g MEAS_CONF1 in register 0x08 configures measurement 1, MEAS_CONF2 in register 0x09 configures measurement 2, ...). Configuring only one measurement is fine, and it can be any one of the 4 possible measurement configuration.
Programming (continued)

1. Setup the input channels for each measurement. Determine which of the 4 measurement configuration
   registers to use (registers 0x08 to 0x0A) and set the following:
   (a) For single-ended measurement:
       (a) Select the positive input pin for the measurement by setting the CHA field (bits[15:13]).
       (b) Set CAPDAC (bits[9:5]) if the channel offset capacitance is more than 15pF.
   (b) For a differential measurement:
       (a) Select the positive input pin for the measurement by setting the CHA field (bits[15:13]).
       (b) Select the negative input pin for the measurement by setting the CHB field (bits[12:10]). Note that the
           CAPDAC setting has no effect for a differential measurement.

2. Determine the appropriate sample rate. The sample rate sets the resolution of the measurement. Lower the
   sample rate higher is the resolution of the measurement.

8.5.3.2 Triggering Measurements

For a single measurement, trigger the desired measurement (i.e. which one of the configured measurements)
when needed by:
1. Setting REPEAT (Register 0x0C:bit[8]) to 0.
2. Setting the corresponding MEAS_x field (Register 0x0C:bit[7:4]) to 1.
   – For example, to trigger a single measurement of Measurement 2 at a rate of 100S/s, set Address 0x0C to
     0x0540.
Note that, at a given time, only one measurement of the configured measurements can be triggered in this
manner (i.e. MEAS_1 and MEAS_2 cannot both be triggered in a single operation).

The FDC1004 can also trigger a new measurement on the completion of the previous measurement (repeated
measurements). This is setup by:
1. Setting REPEAT (Register 0x0C:bit[8]) to 1.
2. Setting the corresponding MEAS_x field (Register 0x0C:bit[7:4]) to 1.

When the FDC1004 is setup for repeated measurements, multiple configured measurements (up to a maximum
of 4) can be performed in this manner, but Register 0x0C must be written in a single transaction.

8.5.3.3 Wait for Measurement Completion

Wait for the triggered measurements to complete. When the measurements are complete, the corresponding
DONE_x field (Register 0x0C:bits[3:0]) will be set to 1.

8.5.3.4 Read of Measurement Result

Read the result of the measurement from the corresponding registers:
• 0x00/0x01 for Measurement 1
• 0x02/0x03 for Measurement 2
• 0x04/0x05 for Measurement 3
• 0x06/0x07 for Measurement 4

The measurement results span 2 register addresses; both registers must be read to have a complete conversion
result. The lower address (e.g. 0x00 for Measurement 1) must be read first, then the upper address read
afterwards (for example, 0x01 for Measurement 1).

Once the measurement read is complete, the corresponding DONE_x field (Register 0x0C:bits[3:0]) will return to
0.

If an additional single triggered measurement is desired, simply perform the Trigger, Wait, Read steps again.

If the FDC1004 is setup for repeated measurements (Register 0x0C:bit[8]) = 1), the FDC1004 will continuously
measure until the REPEAT field (Register 0x0C:bit[8]) is set to 0, even if the results are not read back.
8.6 Register Maps

<table>
<thead>
<tr>
<th>Pointer</th>
<th>Register Name</th>
<th>Reset Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>MEAS1_MSB</td>
<td>0x0000</td>
<td>MSB portion of Measurement 1</td>
</tr>
<tr>
<td>0x01</td>
<td>MEAS1_LSB</td>
<td>0x0000</td>
<td>LSB portion of Measurement 1</td>
</tr>
<tr>
<td>0x02</td>
<td>MEAS2_MSB</td>
<td>0x0000</td>
<td>MSB portion of Measurement 2</td>
</tr>
<tr>
<td>0x03</td>
<td>MEAS2_LSB</td>
<td>0x0000</td>
<td>LSB portion of Measurement 2</td>
</tr>
<tr>
<td>0x04</td>
<td>MEAS3_MSB</td>
<td>0x0000</td>
<td>MSB portion of Measurement 3</td>
</tr>
<tr>
<td>0x05</td>
<td>MEAS3_LSB</td>
<td>0x0000</td>
<td>LSB portion of Measurement 3</td>
</tr>
<tr>
<td>0x06</td>
<td>MEAS4_MSB</td>
<td>0x0000</td>
<td>MSB portion of Measurement 4</td>
</tr>
<tr>
<td>0x07</td>
<td>MEAS4_LSB</td>
<td>0x0000</td>
<td>LSB portion of Measurement 4</td>
</tr>
<tr>
<td>0x08</td>
<td>CONF_MEAS1</td>
<td>0x1C00</td>
<td>Measurement 1 Configuration</td>
</tr>
<tr>
<td>0x09</td>
<td>CONF_MEAS2</td>
<td>0x1C00</td>
<td>Measurement 2 Configuration</td>
</tr>
<tr>
<td>0x0A</td>
<td>CONF_MEAS3</td>
<td>0x1C00</td>
<td>Measurement 3 Configuration</td>
</tr>
<tr>
<td>0x0B</td>
<td>CONF_MEAS4</td>
<td>0x1C00</td>
<td>Measurement 4 Configuration</td>
</tr>
<tr>
<td>0x0C</td>
<td>FDC_CONF</td>
<td>0x0000</td>
<td>Capacitance to Digital Configuration</td>
</tr>
<tr>
<td>0x0D</td>
<td>OFFSET_CAL_CIN1</td>
<td>0x0000</td>
<td>CIN1 Offset Calibration</td>
</tr>
<tr>
<td>0x0E</td>
<td>OFFSET_CAL_CIN2</td>
<td>0x0000</td>
<td>CIN2 Offset Calibration</td>
</tr>
<tr>
<td>0x0F</td>
<td>OFFSET_CAL_CIN3</td>
<td>0x0000</td>
<td>CIN3 Offset Calibration</td>
</tr>
<tr>
<td>0x10</td>
<td>OFFSET_CAL_CIN4</td>
<td>0x0000</td>
<td>CIN4 Offset Calibration</td>
</tr>
<tr>
<td>0x11</td>
<td>GAIN_CAL_CIN1</td>
<td>0x4000</td>
<td>CIN1 Gain Calibration</td>
</tr>
<tr>
<td>0x12</td>
<td>GAIN_CAL_CIN2</td>
<td>0x4000</td>
<td>CIN2 Gain Calibration</td>
</tr>
<tr>
<td>0x13</td>
<td>GAIN_CAL_CIN3</td>
<td>0x4000</td>
<td>CIN3 Gain Calibration</td>
</tr>
<tr>
<td>0x14</td>
<td>GAIN_CAL_CIN4</td>
<td>0x4000</td>
<td>CIN4 Gain Calibration</td>
</tr>
<tr>
<td>0xFE</td>
<td>Manufacturer ID</td>
<td>0x5449</td>
<td>ID of Texas Instruments</td>
</tr>
<tr>
<td>0xFF</td>
<td>Device ID</td>
<td>0x1004</td>
<td>ID of FDC1004 device</td>
</tr>
</tbody>
</table>

Registers from 0x15 to 0xFD are reserved and should not be written to.

8.6.1 Registers

The FDC1004 has an 8-bit pointer used to address a given data register. The pointer identifies which of the data registers should respond to a read or write command on the two-wire bus. This register is set with every write command. A write command must be issued to set the proper value in the pointer before executing a read command. The power-on reset (POR) value of the pointer is 0x00.

8.6.1.1 Capacitive Measurement Registers

The capacitance measurement registers are 24-bit result registers in binary format (the 8 LSBs D[7:0] are always 0x00). The result of the acquisition is always a 24 bit value, while the accuracy is related to the selected conversion time (refer to Electrical Characteristics). The data is encoded in a Two’s complement format. The result of the measurement can be calculated by the following formula:

\[
\text{Capacitance (pf)} = \frac{\text{Two's Complement (measurement [23:0])}}{2^{19}} + C_{\text{offset}}
\]

where

- \(C_{\text{offset}}\) is based on the CAPDAC setting.

Table 2. Measurement Registers Description (0x00, 0x02, 0x04, 0x06)

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB_MEASn(1)</td>
<td>[15:0]</td>
<td>Most significant 16 bits of Measurement n (read only)</td>
</tr>
</tbody>
</table>

(1) MSB_MEAS1 = register 0x00, MSB_MEAS2 = register 0x02, MSB_MEAS3 = register 0x04, MSB_MEAS4 = register 0x06
Table 3. Measurement Registers Description (0x01, 0x03, 0x05, 0x07)

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSB_MEASN^(1)</td>
<td>[15:8]</td>
<td>Least significant 8 bits of Measurement n (read only)</td>
</tr>
<tr>
<td></td>
<td>[7:0]</td>
<td>Reserved, always 0 (read only)</td>
</tr>
</tbody>
</table>

(1) LSB_MEAS1 = register 0x01, LSB_MEAS2 = register 0x03, LSB_MEAS3 = register 0x05, LSB_MEAS4 = register 0x07

8.6.2 Measurement Configuration Registers

These registers configure the input channels and CAPDAC setting for a measurement.

Table 4. Measurement Configuration Registers Description (0x08, 0x09, 0x0A, 0x0B)

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHA^(1)(2)</td>
<td>[15:13]</td>
<td>Positive input channel capacitive to digital converter</td>
</tr>
<tr>
<td></td>
<td>b000</td>
<td>CIN1</td>
</tr>
<tr>
<td></td>
<td>b001</td>
<td>CIN2</td>
</tr>
<tr>
<td></td>
<td>b010</td>
<td>CIN3</td>
</tr>
<tr>
<td></td>
<td>b011</td>
<td>CIN4</td>
</tr>
<tr>
<td>CHB^(1)(2)</td>
<td>[12:10]</td>
<td>Negative input channel capacitive to digital converter</td>
</tr>
<tr>
<td></td>
<td>b000</td>
<td>CIN1</td>
</tr>
<tr>
<td></td>
<td>b001</td>
<td>CIN2</td>
</tr>
<tr>
<td></td>
<td>b010</td>
<td>CIN3</td>
</tr>
<tr>
<td></td>
<td>b011</td>
<td>CIN4</td>
</tr>
<tr>
<td></td>
<td>b100</td>
<td>CAPDAC</td>
</tr>
<tr>
<td></td>
<td>b111</td>
<td>DISABLED</td>
</tr>
<tr>
<td></td>
<td>b00000</td>
<td>0pF (minimum programmable offset)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Configure the single-ended measurement capacitive offset:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C_{\text{offset}} = \text{CAPDAC} \times 3.125pF</td>
</tr>
<tr>
<td></td>
<td>b11111</td>
<td>96.875pF (maximum programmable offset)</td>
</tr>
<tr>
<td>RESERVED</td>
<td>[04:00]</td>
<td>Reserved, always 0 (read only)</td>
</tr>
</tbody>
</table>

(1) It is not permitted to configure a measurement where the CHA field and CHB field hold the same value (for example, if CHA=b010, CHB cannot also be set to b010).
(2) It is not permitted to configure a differential measurement between CHA and CHB where CHA > CHB (for example, if CHA=b010, CHB cannot be b001 or b000).

8.6.3 FDC Configuration Register

This register configures measurement triggering and reports measurement completion.

Table 5. FDC Register Description (0x0C)

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RST</td>
<td>[15]</td>
<td>Reset</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Normal operation</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Software reset: write a 1 to initiate a device reset; after completion of reset this field will return to 0</td>
</tr>
<tr>
<td>RESERVED</td>
<td>[14:12]</td>
<td>Reserved, always 0 (read only)</td>
</tr>
<tr>
<td>RATE</td>
<td>[11:10]</td>
<td>Measurement Rate</td>
</tr>
<tr>
<td></td>
<td>b00</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>b01</td>
<td>100S/s</td>
</tr>
<tr>
<td></td>
<td>b10</td>
<td>200S/s</td>
</tr>
<tr>
<td></td>
<td>b11</td>
<td>400S/s</td>
</tr>
<tr>
<td>RESERVED</td>
<td>[9]</td>
<td>Reserved, always 0 (read only)</td>
</tr>
<tr>
<td>REPEAT</td>
<td>[8]</td>
<td>Repeat Measurements</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Repeat disabled</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Repeat enabled, all the enabled measurement are repeated</td>
</tr>
<tr>
<td>MEAS_1</td>
<td>[7]</td>
<td>Initiate Measurements</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Measurement 1 disabled</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Measurement 1 enabled</td>
</tr>
<tr>
<td>MEAS_2</td>
<td>[6]</td>
<td>Initiate Measurements</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Measurement 2 disabled</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Measurement 2 enabled</td>
</tr>
</tbody>
</table>
Table 5. FDC Register Description (0x0C) (continued)

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEAS_3</td>
<td>[5]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Initiate Measurements</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Measurement 3 disabled</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Measurement 3 enabled</td>
</tr>
<tr>
<td>MEAS_4</td>
<td>[4]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Initiate Measurements</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Measurement 4 disabled</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Measurement 4 enabled</td>
</tr>
<tr>
<td>DONE_1</td>
<td>[3]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Measurement Done</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Measurement 1 not completed</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Measurement 1 completed</td>
</tr>
<tr>
<td>DONE_2</td>
<td>[2]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Measurement Done</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Measurement 2 not completed</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Measurement 2 completed</td>
</tr>
<tr>
<td>DONE_3</td>
<td>[1]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Measurement Done</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Measurement 3 not completed</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Measurement 3 completed</td>
</tr>
<tr>
<td>DONE_4</td>
<td>[0]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Measurement Done</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Measurement 4 not completed</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Measurement 4 completed</td>
</tr>
</tbody>
</table>

8.6.4 Offset Calibration Registers

These registers configure a digitized capacitance value in the range of -16 pF to 16 pF (max residual offset 250 aF) that can be added to each channel in order to remove parasitic capacitance due to external circuitry. In addition to the offset calibration capacitance which is a fine-tune offset capacitance, it is possible to support a larger offset by using the CAPDAC (for up to 100 pF). These 16-bit registers are formatted as a fixed point number, where the first 5 bits represents the integer portion of the capacitance in Two’s complement format, and the remaining 11 bits represent the fractional portion of the capacitance.

Table 6. Offset Calibration Registers Description (0x0D, 0x0E, 0x0F, 0x10)

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET_CALn(1)</td>
<td>[15:11]</td>
<td>Integer part</td>
</tr>
<tr>
<td></td>
<td>[10:0]</td>
<td>Decimal part</td>
</tr>
<tr>
<td>OFFSET_CALn(1)</td>
<td>[15:11]</td>
<td>Integer portion of the Offset Calibration of Channel CINn</td>
</tr>
<tr>
<td></td>
<td>[10:0]</td>
<td>Decimal portion of the Offset Calibration of Channel CINn</td>
</tr>
</tbody>
</table>

(1) OFFSET_CAL1 = register 0x0D, OFFSET_CAL2 = register 0x0E, OFFSET_CAL3 = register 0x0F, OFFSET_CAL4 = register 0x10

8.6.5 Gain Calibration Registers

These registers contain a gain factor correction in the range of 0 to 4 that can be applied to each channel in order to remove gain mismatch due to the external circuitry. This 16-bit register is formatted as a fixed point number, where the 2 MSBs of the GAIN_CALn register correspond to an integer portion of the gain correction, and the remaining 14 bits represent the fractional portion of the gain correction. The result of the conversion represents a number without dimensions.

The Gain can be set according to the following formula:

\[ \text{Gain} = \frac{\text{GAIN_CAL}[15:0]}{2^{14}} \]

Table 7. Gain Calibration Registers Description (0x11, 0x12, 0x13, 0x14)

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GAIN_CALn(1)</td>
<td>[15:14]</td>
<td>Integer part</td>
</tr>
<tr>
<td></td>
<td>[13:0]</td>
<td>Decimal part</td>
</tr>
<tr>
<td>GAIN_CALn(1)</td>
<td>[15:14]</td>
<td>Integer portion of the Gain Calibration of Channel CINn</td>
</tr>
<tr>
<td></td>
<td>[13:0]</td>
<td>Decimal portion of the Gain Calibration of Channel CINn</td>
</tr>
</tbody>
</table>

(1) GAIN_CAL1 = register 0x11, GAIN_CAL2 = register 0x12, GAIN_CAL3 = register 0x13, GAIN_CAL4 = register 0x14

8.6.6 Manufacturer ID Register

This register contains a factory-programmable identification value that identifies this device as being manufactured by Texas Instruments. This register distinguishes this device from other devices that are on the same I²C bus. The manufacturer ID reads 0x5449.
Table 8. Manufacturer ID Register Description (0xFE)

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MANUFACTURER ID</td>
<td>[15:0]</td>
<td>Manufacturer 0x5449h Texas instruments ID (read only)</td>
</tr>
</tbody>
</table>

8.6.7 Device ID Register

This register contains a factory-programmable identification value that identifies this device as a FDC1004. This register distinguishes this device from other devices that are on the same I2C bus. The Device ID for the FDC1004 is 0x1004.

Table 9. Device ID Register Description (0xFF)

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEVICE ID</td>
<td>[15:0]</td>
<td>Device ID 0x1004 FDC1004 Device ID (read only)</td>
</tr>
</tbody>
</table>
9 Applications and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Liquid Level Measurement

The FDC1004 can be used to measure liquid level in non-conductive containers. Capacitive sensors can be attached to the outside of the container or be located remotely from the container, allowing for contactless measurements. The working principle is based on a ratiometric measurement; Figure 14 shows a possible system implementation which uses three electrodes. The Level electrode provides a capacitance value proportional to the liquid level. The Reference Environmental electrode and the Reference Liquid electrode are used as references. The Reference Liquid electrode accounts for the liquid dielectric constant and its variation, while the Reference Environmental electrode is used to compensate for any other environmental variations that are not due to the liquid itself. Note that the Reference Environmental electrode and the Reference Liquid electrode are the same physical size (\(h_{\text{REF}}\)).

For this application, single-ended measurements on the appropriate channels are appropriate, as the tank is grounded.

Use the following formula to determine the liquid level from the measured capacitances:

\[
Level = h_{\text{ref}} \frac{C_{\text{Lev}} - C_{\text{Lev}}(0)}{C_{\text{RL}} - C_{\text{RE}}}
\]

where

- \(C_{\text{RE}}\) is the capacitance of the Reference Environmental electrode,
- \(C_{\text{RL}}\) is the capacitance of the Reference Liquid electrode,
- \(C_{\text{Lev}}\) is the current value of the capacitance measured at the Level electrode sensor,
- \(C_{\text{Lev}}(0)\) is the capacitance of the Level electrode when the container is empty, and
- \(h_{\text{REF}}\) is the height in the desired units of the Container or Liquid Reference electrodes.

The ratio between the capacitance of the level and the reference electrodes allows simple calculation of the liquid level inside the container itself. Very high sensitivity values (that is, many LSB/mm) can be obtained due to the high resolution of the FDC1004, even when the sensors are located remotely from the container.

9.2 Typical Application

![Figure 14. FDC1004 (Liquid Level Measurement)](image-url)
Typical Application (continued)

9.2.1 Design Requirements

The liquid level measurement should be independent of the liquid, which can be achieved using the 3-electrode design described above. Moreover, the sensor should be immune to environmental interferers such as a human body, other objects, or EMI. This can be achieved by shielding the side of the sensor which does not face the container.

9.2.2 Detailed Design Procedure

In capacitive sensing systems, the design of the sensor plays an important role in determining system performance and capabilities. In most cases the sensor is simply a metal plate that can be designed on the PCB. The sensor used in this example is implemented with a two-layer PCB. On the top layer, which faces the tank, there are the 3 electrodes (Reference Environmental, Reference Liquid, and Level) with a ground plane surrounding the electrodes. The bottom layer is covered with a shield plane in order to isolate the electrodes from any external interference sources.

Depending on the shape of the container, the FDC1004 can be located on the sensor PCB to minimize the length of the traces between the input channels and the sensors and increase the immunity from EMI sources. In case the shape of the container or other mechanical constraints do not allow having the sensors and the FDC1004 on the same PCB, the traces which connect the channels to the sensor need to be shielded with the appropriate shield. In this design example all of the channels are shielded with SHLD1. For this configuration, the FDC1004 measures the capacitance of the 3 channels versus ground; and so the SHLD1 and SHLD2 pins are internally shorted in the FDC1004 (see The Shield).

9.2.3 Application Performance Plot

The data shown below has been collected with the FDC1004EVM. A liquid level sensor with 3 electrodes like the one shown in the schematic was connected to the EVM. The plot shows the capacitance measured by the 3 electrodes at different levels of liquid in the tank. The capacitance of the Reference Liquid (the RF trace in the graph below) and Reference Environmental (the RE trace) sensors have a steady value when the liquid is above their height while the capacitance of the level sensor (Level) increases linearly with the height of the liquid in the tank.

![Figure 15. Electrodes' Capacitance vs. Liquid Level](image-url)
9.3 Do's and Don'ts
Avoid long traces to connect the sensor to the FDC1004. Short traces reduce parasitic capacitances between shield versus input channel and parasitic resistance between input channel versus GND and shield versus GND. Since the sensor in many cases is simply a metal surface on a PCB, it needs to be protected with solder resist to avoid short circuits and limit any corrosion. Any change in the sensor may result in a change in system performance.

9.4 Initialization Set Up
At power on the device is in stand-by. It stays in this mode until a measurement is triggered.

10 Power Supply Recommendations
The FDC1004 requires a voltage supply within 3 V and 3.6 V. Two multilayer ceramic bypass X7R capacitors of 0.1 μF and 1 μF, respectively between VDD and GND pin are recommended. The 0.1-μF capacitor should be closer to the VDD pin than the 1-μF capacitor.

11 Layout

11.1 Layout Guidelines
The FDC1004 measures the capacitances connected between the CINn (n=1..4) pins and GND. To get the best result, locate the FDC1004 as close as possible to the capacitive sensor. Minimize the connection length between the sensor and FDC1004 CINn pins and between the sensor ground and the FDC1004 GND pin. If a shielded cable is used for remote sensor connection, the shield should be connected to the SHLDm (m=1...2) pin according to the configured measurement.

11.2 Layout Example
Figure 16 below is optimized for applications where the sensor is not too far from the FDC1004. Each channel trace runs between 2 shield traces. This layout allows the measurements of 4 single ended capacitance or 2 differential capacitance. The ground plane needs to be far from the channel traces, it is mandatory around or below the I2C pin.

Figure 16. Layout
12 Device and Documentation Support

12.1 Trademarks
All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDC1004DGSR</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>3500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>ZBNX</td>
<td>Samples</td>
</tr>
<tr>
<td>FDC1004DGST</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>ZBNX</td>
<td>Samples</td>
</tr>
<tr>
<td>FDC1004DSCJ</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DSC</td>
<td>10</td>
<td>4500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>F1004</td>
<td>Samples</td>
</tr>
<tr>
<td>FDC1004DSCR</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DSC</td>
<td>10</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>F1004</td>
<td>Samples</td>
</tr>
<tr>
<td>FDC1004DSCT</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DSC</td>
<td>10</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>F1004</td>
<td>Samples</td>
</tr>
</tbody>
</table>

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1. The marketing status values are defined as follows:
   - **ACTIVE**: Product device recommended for new designs.
   - **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
   - **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
   - **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
   - **OBSOLETE**: TI has discontinued the production of the device.

2. **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
   - **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
   - **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

3. **MSL, Peak Temp. -** The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

4. There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

5. Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

6. **Lead/Ball Finish -** Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
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OTHER QUALIFIED VERSIONS OF FDC1004:

- Automotive: FDC1004-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDC1004DGSR</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>3500</td>
<td>330.0</td>
<td>12.4</td>
<td>5.3</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
<td></td>
</tr>
<tr>
<td>FDC1004DGST</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>250</td>
<td>178.0</td>
<td>12.4</td>
<td>5.3</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
<td></td>
</tr>
<tr>
<td>FDC1004DSCJ</td>
<td>WSON</td>
<td>DSC</td>
<td>10</td>
<td>4500</td>
<td>330.0</td>
<td>12.4</td>
<td>3.3</td>
<td>1.0</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
<td></td>
</tr>
<tr>
<td>FDC1004DSCR</td>
<td>WSON</td>
<td>DSC</td>
<td>10</td>
<td>1000</td>
<td>178.0</td>
<td>12.4</td>
<td>3.3</td>
<td>1.0</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
<td></td>
</tr>
<tr>
<td>FDC1004DSCT</td>
<td>WSON</td>
<td>DSC</td>
<td>10</td>
<td>250</td>
<td>178.0</td>
<td>12.4</td>
<td>3.3</td>
<td>1.0</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
<td></td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
**TAPE AND REEL BOX DIMENSIONS**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDC1004DGSR</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>3500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>FDC1004DGST</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>FDC1004DSCJ</td>
<td>WSON</td>
<td>DSC</td>
<td>10</td>
<td>4500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>FDC1004DSCR</td>
<td>WSON</td>
<td>DSC</td>
<td>10</td>
<td>1000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>FDC1004DSCT</td>
<td>WSON</td>
<td>DSC</td>
<td>10</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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