LM3525 Single Port USB Power Switch and Over-Current Protection

Check for Samples: LM3525

FEATURES

- **Compatible with USB1.1 and USB 2.0**
- **1 ms Fault Flag Delay During Hot-Plug Events**
- **Smooth Turn-On Eliminates Inrush Induced Voltage Drop**
- **UL Recognized Component: REF # 205202**
- **1A Nominal Short Circuit Output Current Protects Notebook PC Power Supplies**
- **Thermal Shutdown Protects Device in Direct Short Condition**
- **500mA Minimum Continuous Load Current**
- **Small SOIC-8 Package Minimizes Board Space**
- **2.7V to 5.5V Input Voltage Range**
- **Switch Resistance ≤ 120 mΩ Max. at V_{IN} = 5V**
- **1µA Max Standby Current**
- **100 µA Max Operating Current**
- **Undervoltage Lockout (UVLO)**

APPLICATIONS

- **Universal Serial Bus (USB) Root Hubs including Desktop and Notebook PC**
- **USB Monitor Hubs**
- **Other Self-Powered USB Hub Devices**
- **High Power USB Devices Requiring Inrush Limiting**
- **General Purpose High Side Switch Applications**

DESCRIPTION

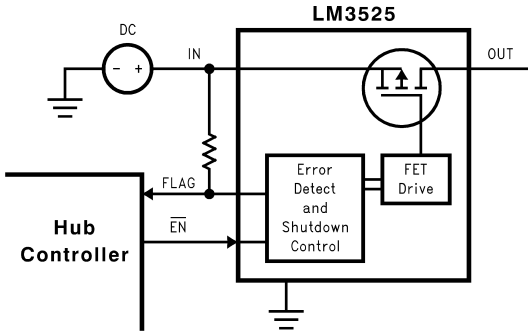
The LM3525 provides Universal Serial Bus standard power switch and over-current protection for all host port applications. The single port device is ideal for Notebook PC and Handheld PC applications that supply power to one port.

A 1 ms delay on fault flag output prevents erroneous overcurrent reporting caused by inrush currents during the hot-plug events.

The LM3525 accepts an input voltage between 2.7V and 5.5V allowing use as a device-based inrush current limiter for 3.3V USB peripherals, as well as Root and Self-Powered Hubs at 5.5V. The Enable input accepts both 3.3V and 5.0V logic thresholds.

The small size, low R_{ON}, and 1 ms fault flag delay make the LM3525 a good choice for root hubs as well as ganged power control in space-critical self-powered hubs.

Typical Operating Circuit and Connection Diagram



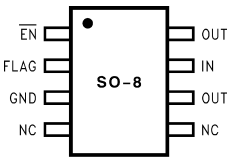


Figure 1. LM3525M-L

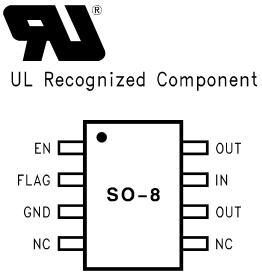


Figure 2. LM3525M-H

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage	−0.3V to 6.0V
Output Voltage	−0.3V to 6.0V
Voltage at All Other Pins	−0.3V to 5.5V
Power Dissipation (T_A = 25°C)(3)	700 mW
T_{JMAX}(3)	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions. Products are not tested under negative Absolute Maximum conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, which ever is lower. The thermal resistance θ_{JA} of the LM3525 in the SOIC-8 package is 150°C/W.

Operating Ratings

Supply Voltage Range	2.7 to 5.5V
Operating Ambient Range	−40°C to +85°C
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 5 seconds)	260°C
ESD Rating(1)	2 kV

(1) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

DC Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface** type apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 5.0V, $\overline{EN}$ = 0V (LM3525-L) or EN = V_{IN} (LM3525-H).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{ON}	On-Resistance	IN to Out pins V_{IN} = 5V V_{IN} = 2.7V		80 120	120 160	mΩ
I_{OUT}	OUT pins continuous output current		**0.5**			A
I_{SC}	Short Circuit Output Current	See (1)	0.5	1.0	1.5	A
I_{LEAK}	OUT pins Output Leakage Current	$\overline{EN}$ = V_{IN} (LM3525-L) or EN = GND (LM3525-H),		0.15	10	µA
OC_{THRESH}	Over-current Threshold			2.25	3.2	A
R_{FO}	FLAG Output Resistance	I_{FO} = 10 mA, V_{IN} = 5V		6	**25**	Ω
		I_{FO} = 10 mA, V_{IN} = 2.7V		8	**40**	
I_{EN}	$\overline{EN}$/EN Leakage Current	$\overline{EN}$/EN = 0V or $\overline{EN}$/EN = V_{IN}	−0.5		0.5	µA
V_{IH}	$\overline{EN}$/EN Input Voltage	See (2)	**2.4**	1.9		V
V_{IL}	$\overline{EN}$/EN Input Voltage	See (2)		1.7	**0.8**	V
V_{UVLO}	Under-Voltage Lockout	V_{IN} = Increasing V_{IN} = Decreasing		1.9 1.8		V
I_{DDOFF}	Supply Current	Switch OFF		0.05	1	µA
I_{DDON}	Supply Current	Switch ON		65	100	µA
Th_{SD}	Overtemperature Shutdown Threshold (1)	T_J Increasing T_J Decreasing		135 125		°C °C
I_{FH}	Error Flag Leakage Current	V_{FLAG}= 5V		0.1	1	µA

(1) Thermal shutdown will protect the device from permanent damage.
(2) For the LM3525-L, OFF is $\overline{EN}$ ≥ 2.4V and ON is $\overline{EN}$ ≤ 0.8V. For the LM3525-H, OFF is EN ≤ 0.8V and ON is EN ≥ 2.4V

AC Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface** type apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 5.0V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_r	OUT Rise Time	R_L = 10Ω		200		µs
t_f	OUT Fall Time	R_L = 10Ω		20		µs
t_{ON}	Turn on Delay, $\overline{EN}$ to OUT	R_L = 10Ω		200		µs
t_{OFF}	Turn off Delay, $\overline{EN}$ to OUT	R_L = 10Ω		20		µs
t_{OC}	Over Current Flag Delay	R_L = 0		1		ms

TYPICAL APPLICATION CIRCUIT

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1	$\overline{EN}$ (LM3525-L) EN (LM3525-H)	Enable (Input): Logic-compatible enable input.
2	FLG	Fault Flag (Output): Active-low, open-drain output. Indicates overcurrent, UVLO and thermal shutdown.
3	GND	Ground
4, 5	NC	Not internally connected.
7	IN	Supply Input: This pin is the input to the power switch and the supply voltage for the IC.
6, 8	OUT	Switch Output: This pin is the output of the high side switch. Pins 6 & 8 must be tied together.

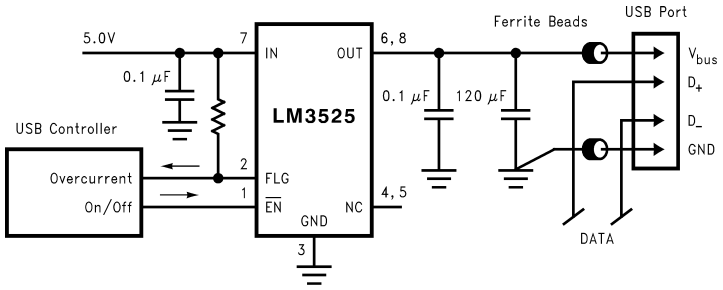


Figure 3. Typical Application Circuit

Typical Performance Characteristics

V_{IN} = 5.0V, I_L = 500 mA, T_A = 25°C unless otherwise specified.

RDS_{ON} vs V_{IN}

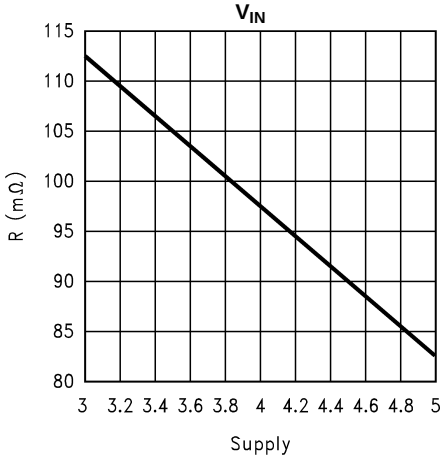


Figure 4.

RDS_{ON} vs Temperature

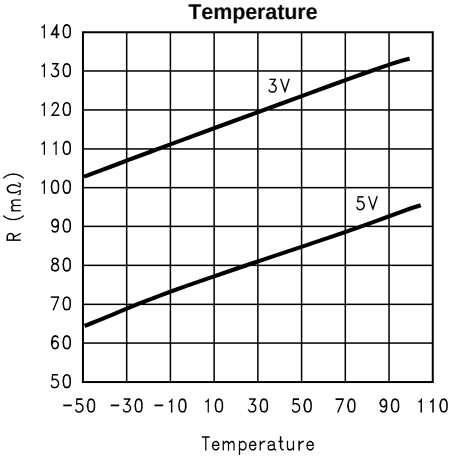


Figure 5.

Current Limit vs Temperature

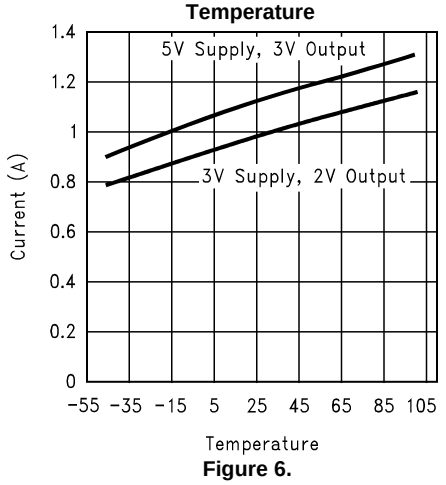


Figure 6.

Over Current Threshold vs Temperature

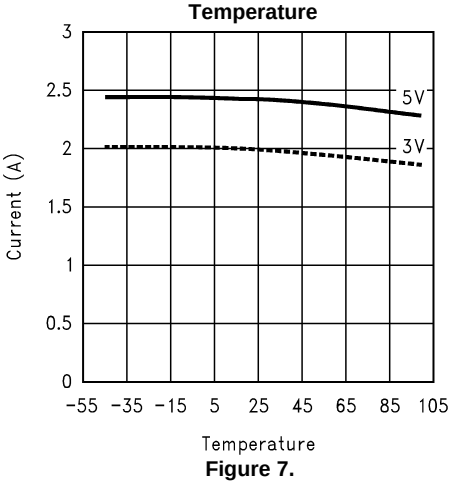


Figure 7.

Delay vs Temperature

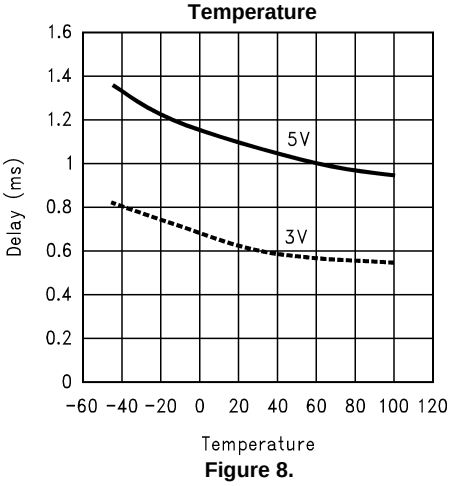


Figure 8.

UVLO Threshold

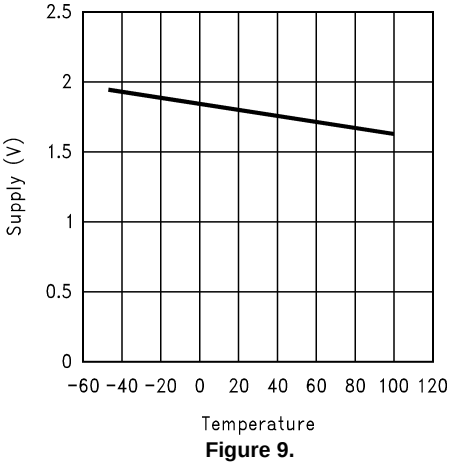


Figure 9.

Typical Performance Characteristics (continued)

V_{IN} = 5.0V, I_L = 500 mA, T_A = 25°C unless otherwise specified.

Short Circuit Response

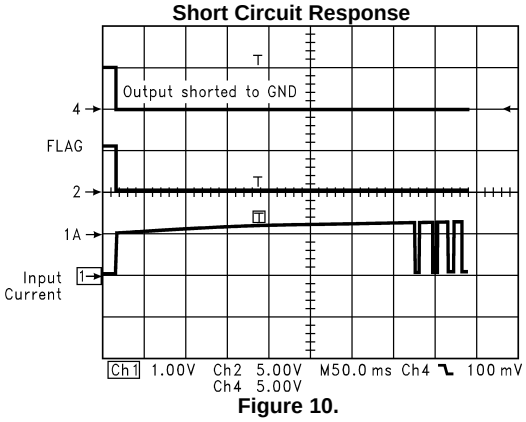


Figure 10.

Under Voltage Lock Out (UVLO)

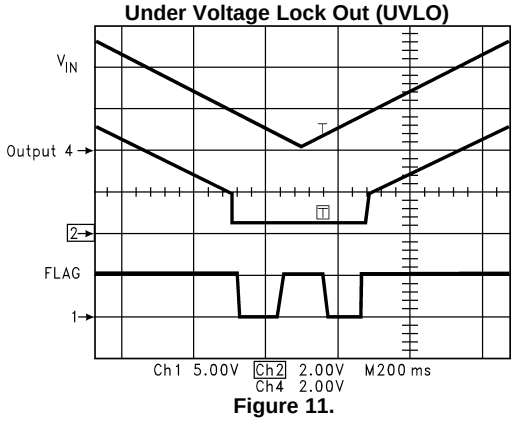


Figure 11.

Turn-ON/OFF Delay and Rise Time/Fall Time

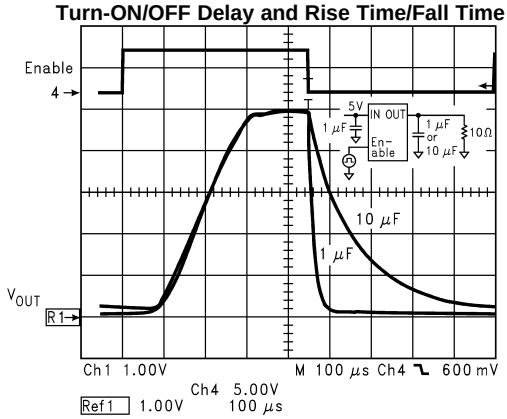


Figure 12.

Short Circuit Current

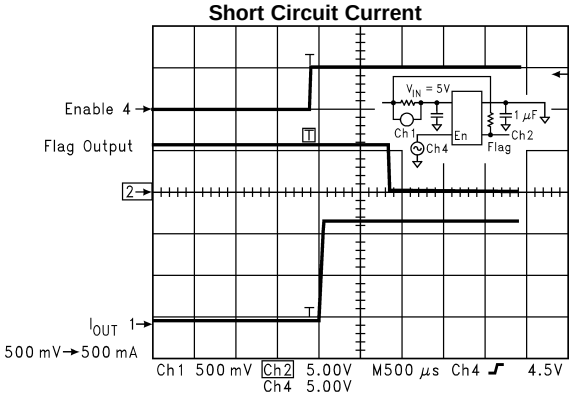


Figure 13.

FUNCTIONAL DESCRIPTION

The LM3525-H and LM3525-L are high side P-Channel switches with active-high and active-low enable inputs, respectively. Fault conditions turn off and inhibit turn-on of the output transistor and activate the open-drain error flag transistor sinking current to the ground.

INPUT AND OUTPUT

IN (Input) is the power supply connection to the control circuitry and the source of the output MOSFET.

OUT (Output) is the drain of the output MOSFET. In a typical application circuit, current flows through the switch from IN to OUT towards the load.

If V_{OUT} is greater than V_{IN} when the switch is enabled, current will flow from OUT to IN since the MOSFET is bidirectional.

THERMAL SHUTDOWN

LM3525 is internally protected against excessive power dissipation. In the event of a shorted output or heavy loads that could elevate the die temperature to above approximately 135°C, the thermal shutdown circuit of the LM3525 will be activated and the power switch turned off.

The switch is turned on after die temperature drops by 10°C. This built-in temperature hysteresis prevents undesirable oscillation of the thermal protection circuit and allows the device to reset itself after it is cooled down.

UNDERVOLTAGE LOCKOUT

UVLO prevents the MOSFET switch from turning on until input voltage exceeds 1.9V.

UVLO shuts off the MOSFET switch and signals the fault flag if input voltage drops below 1.8V. UVLO functions only when device is enabled.

CURRENT LIMIT

The current limit circuit is designed to protect the system supply, the MOSFET switches and the load from damage caused by excessive currents. The current limit threshold is set internally to allow a minimum of 500 mA through the MOSFET but limit the maximum current to 1.0A typical.

FAULT FLAG

The fault flag is an open-drain output capable of sinking 10 mA load current to typically 60 mV above ground.

The fault flag is active (pulled low) when any of the following conditions are present: undervoltage, current limit, or thermal shutdown.

A 1ms delay in reporting fault condition prevents erroneous fault flags and eliminates the need for external RC delay network.

Application Information

FILTERING

The USB specification indicates that “no less than 120 µF tantalum capacitors” must be used on the output of each downstream port. This bulk capacitance provides the short-term transient current needed during a hot plug-in. Current surges caused by the input capacitance of the down stream device could generate undesirable EMI signals. Ferrite beads in series with all power and ground lines are recommended to eliminate or significantly reduce EMI.

In selecting a ferrite bead, the DC resistance of the wire used must be kept to minimum to reduce the voltage drop.

A 0.01 µF ceramic capacitor is recommended on each port directly between the V_{bus} and ground pins to prevent EMI damage to other components during the hot - detachment.

Adequate capacitance must be connected to the input of the device to limit the input voltage drop during a hot-plug event to less than 330 mV. For a few tens of µs, the host must supply the inrush current to the peripheral, charging its bulk capacitance to V_{bus}. This current is initially supplied by the input capacitor. A 33 µF 16V tantalum capacitor is recommended.

In choosing the capacitors, special attention must be paid to the Effective Series Resistance, ESR, of the capacitors to minimize the IR drop across the capacitor's ESR.

SOFT START

To eliminate the upstream voltage droop caused by the high in-rush current drawn by the output capacitors, the inrush current is internally limited to 1.0A.

TRANSIENT OVER-CURRENT DELAY

In USB applications, it is required that output bulk capacitance is utilized to support hot-plug events. During hot-plug events, inrush currents may also cause the flag to go active. Since these conditions are not valid over-current faults, the USB controller must ignore the flag during these events.

High transient current is also generated when switch is enabled and large values of capacitance at the output have to be rapidly charged. The inrush currents created could exceed the short circuit current limit threshold of the device forcing it into the current limit mode. The capacitor is charged with the maximum available short circuit current set by the LM3525. The duration of the inrush current depends on the size of the output capacitance and load current. Since this is not a valid fault condition, the LM3525 delays the generation of the fault flag for 1 ms. If condition persists due to other causes such as a short, a fault flag is generated after a 1 ms delay has elapsed.

The LM3525's 1 ms delay in issuing the fault flag is adequate for most applications. If longer delays are required, an RC filter as shown in Figure 14 may be used.

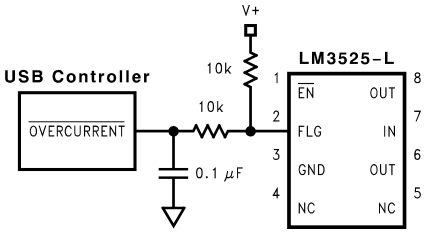


Figure 14. Transient Fitter

PCB LAYOUT CONSIDERATIONS

In order to meet the USB requirements for voltage drop, droop and EMI, each component used in this circuit must be evaluated for its contribution to the circuit performance as shown in Figure 15. The PCB layout rules and guidelines must be followed.

- Place the switch as close to the USB connector as possible. Keep all V_{bus} traces as short as possible and use at least 50-mil, 1 ounce copper for all V_{bus} traces. Solder plating the traces will reduce the trace resistance.
- Avoid vias as much as possible. If vias are used, use multiple vias in parallel and/or make them as large as possible.
- Place the output capacitor and ferrite beads as close to the USB connector as possible.
- If ferrite beads are used, use wires with minimum resistance and large solder pads to minimize connection resistance.

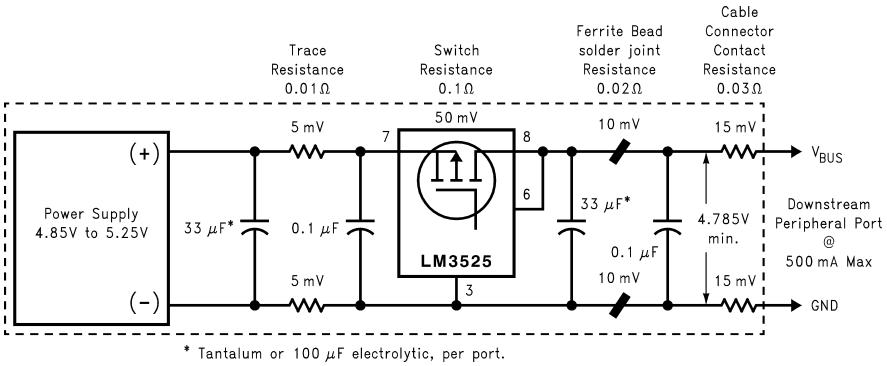


Figure 15. Self-Powered Hub Per-Port Voltage Drop

Typical Applications

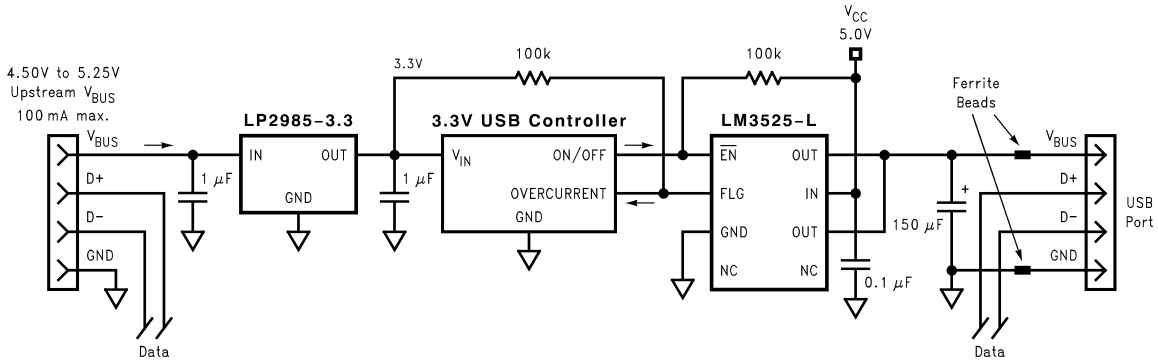


Figure 16. SIngle-Port USB Self-Powered Hub

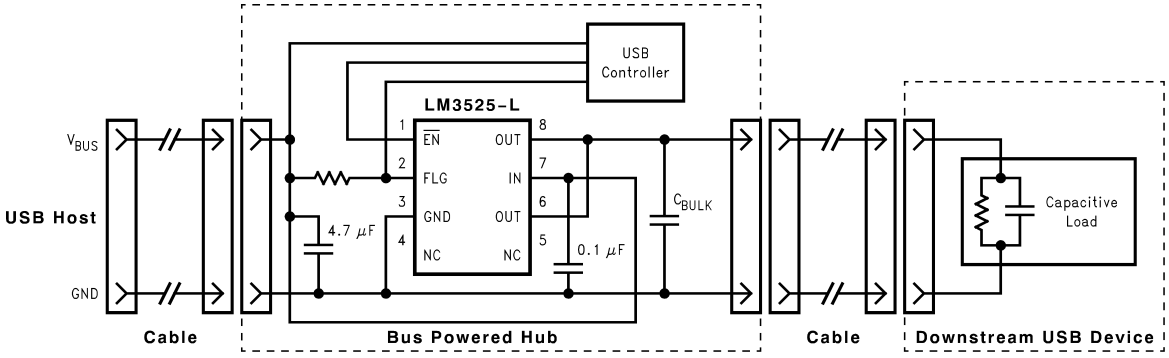


Figure 17. Soft-Start Application

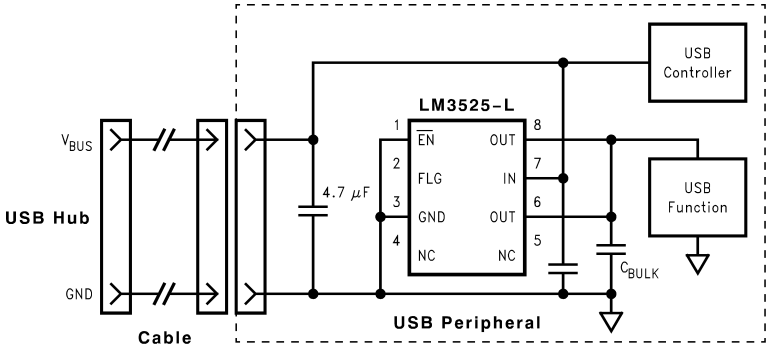


Figure 18. Inrush Current-limit Application

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3525M-H/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3525 M-H	Samples
LM3525M-L/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3525 M-L	Samples
LM3525MX-H/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3525 M-H	Samples
LM3525MX-L/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3525 M-L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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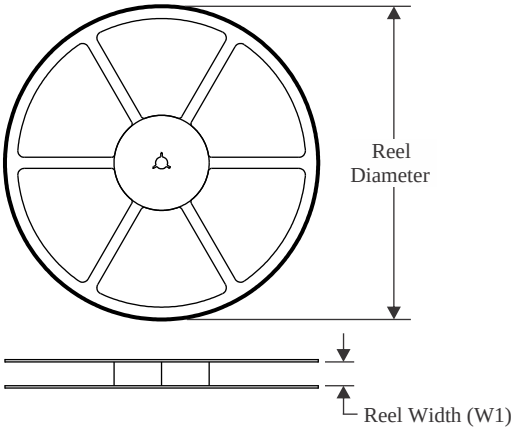
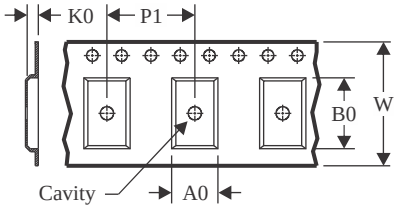
TAPE AND REEL INFORMATION

REEL DIMENSIONS

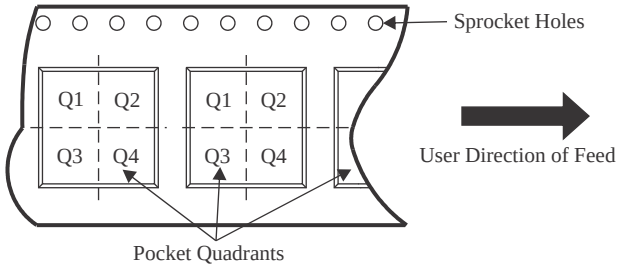


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

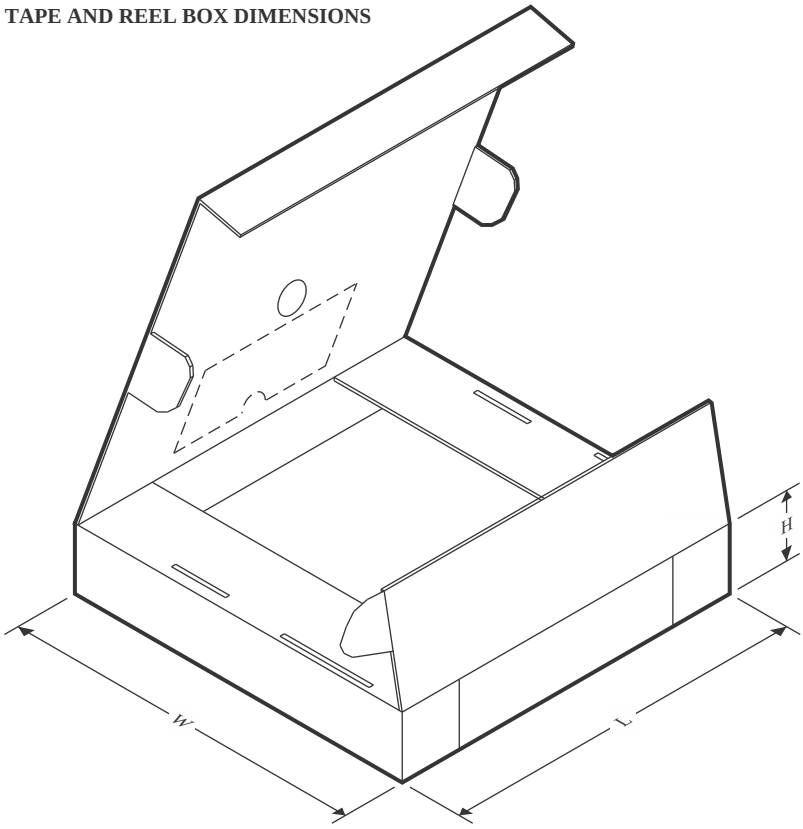
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3525MX-H/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM3525MX-L/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

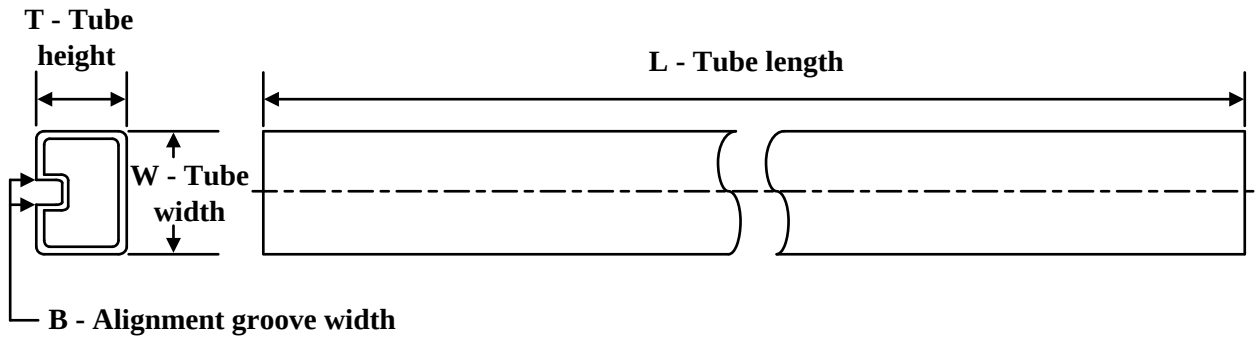
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

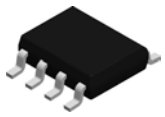
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3525MX-H/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM3525MX-L/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM3525M-H/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM3525M-L/NOPB	D	SOIC	8	95	495	8	4064	3.05

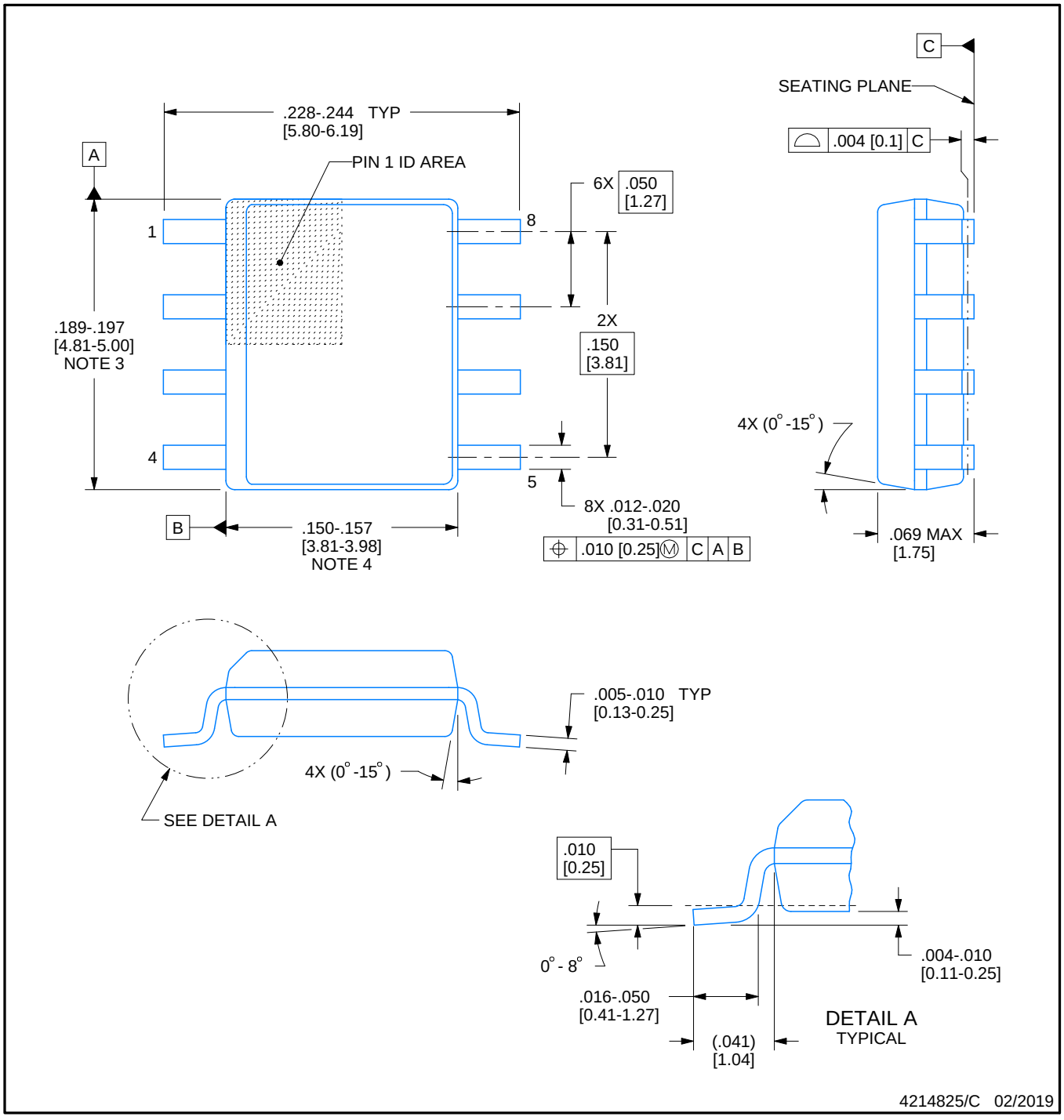


PACKAGE OUTLINE

D0008A

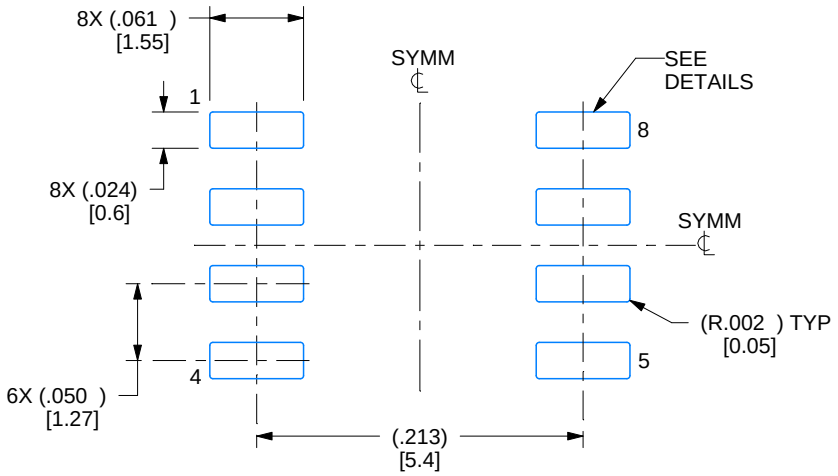
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

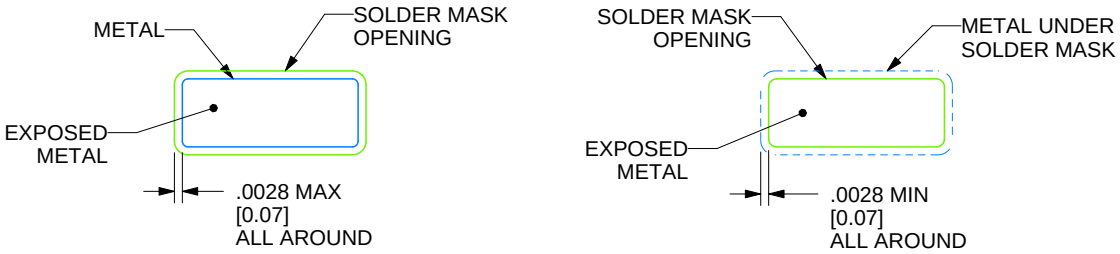


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

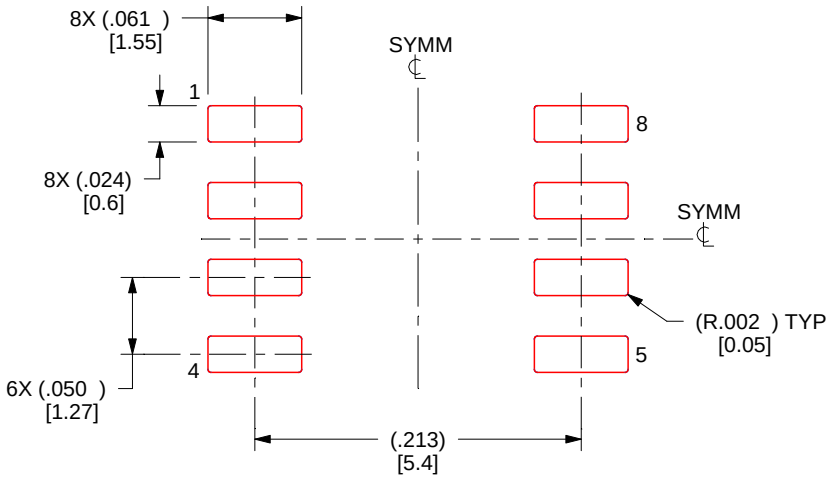
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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