LM2622 600kHz/1.3MHz Step-up PWM DC/DC Converter

FEATURES
- 1.6A, 0.2Ω, Internal Switch
- Operating Voltage as Low as 2.0V
- 600kHz/1.3MHz Pin Selectable Frequency Operation
- Over Temperature Protection
- 8-Lead VSSOP Package

APPLICATIONS
- TFT Bias Supplies
- Handheld Devices
- Portable Applications
- GSM/CDMA Phones
- Digital Cameras

DESCRIPTION
The LM2622 is a step-up DC/DC converter with a 1.6A, 0.2Ω internal switch and pin selectable operating frequency. With the ability to convert 3.3V to multiple outputs of 8V, -8V, and 23V, the LM2622 is an ideal part for biasing TFT displays. The LM2622 can be operated at switching frequencies of 600kHz and 1.3MHz allowing for easy filtering and low noise. An external compensation pin gives the user flexibility in setting frequency compensation, which makes possible the use of small, low ESR ceramic capacitors at the output. The LM2622 is available in a low profile 8-lead VSSOP package.

Typical Application Circuit

![Typical Application Circuit](image_url)

**Figure 1. 600 kHz Operation**
Connection Diagram

Figure 2. Top View
8-Lead Plastic VSSOP
See DGK Package

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V_C</td>
<td>Compensation network connection. Connected to the output of the voltage error amplifier.</td>
</tr>
<tr>
<td>2</td>
<td>FB</td>
<td>Output voltage feedback input.</td>
</tr>
<tr>
<td>3</td>
<td>SHDN</td>
<td>Shutdown control input, active low.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Analog and power ground.</td>
</tr>
<tr>
<td>5</td>
<td>SW</td>
<td>Power switch input. Switch connected between SW pin and GND pin.</td>
</tr>
<tr>
<td>6</td>
<td>V_IN</td>
<td>Analog power input.</td>
</tr>
<tr>
<td>7</td>
<td>FSLCT</td>
<td>Switching frequency select input. V_IN = 1.3MHz. Ground = 600kHz.</td>
</tr>
<tr>
<td>8</td>
<td>NC</td>
<td>Connect to ground or leave open. Connect to GND pin directly beneath the device if possible. If other traces are in the way or it is otherwise not possible to directly connect it to GND leave this pin open and shield it from sources of EMI.</td>
</tr>
</tbody>
</table>
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.
Absolute Maximum Ratings (1)(2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_IN</td>
<td>12V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SW Voltage</td>
<td>18V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB Voltage</td>
<td>7V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_C Voltage</td>
<td>7V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHDN Voltage</td>
<td>7V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSLCT</td>
<td>12V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Maximum Junction Temperature: 150 °C

Power Dissipation:<br>Internally Limited

Lead Temperature:<br>Vapor Phase (60 sec.): 215 °C<br>Infrared (15 sec.): 220 °C

ESD Susceptibility:<br>Human Body Model: 2kV<br>Machine Model: 200V

Operating Conditions

Operating Junction Temperature Range (1): −40 °C to +125 °C

Storage Temperature: −65 °C to +150 °C

Supply Voltage: 2V to 12V

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For ensured specifications and test conditions, see the Electrical Characteristics.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J$(MAX), the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. See the Electrical Characteristics table for the thermal resistance of various layouts. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_D$(MAX) = ($T_J$(MAX) − $T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

(4) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Electrical Characteristics

Specifications in standard type face are for $T_J$ = 25 °C and those with boldface type apply over the full Operating Temperature Range ($T_J$ = −40 °C to +125 °C). Unless otherwise specified, $V_{IN}$ = 2.0V and $I_L$ = 0A, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min (t)</th>
<th>Typ (t)</th>
<th>Max (t)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>IQ</td>
<td>Quiescent Current</td>
<td>$V_{SHDN} = 0V$ (Not Switching)</td>
<td>1.3</td>
<td>2.0</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>VF</td>
<td>Feedback Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>ISCL</td>
<td>Switch Current Limit</td>
<td>$V_{IN} = 2.7V$ (4)</td>
<td>1.0</td>
<td>1.65</td>
<td>2.3</td>
<td>A</td>
</tr>
<tr>
<td>$\Delta V_O/\Delta I_{LOAD}$</td>
<td>Load Regulation</td>
<td>$V_{IN} = 3.3V$</td>
<td>6.7</td>
<td></td>
<td></td>
<td>mV/A</td>
</tr>
<tr>
<td>$%V_F/B/\Delta V_{IN}$</td>
<td>Feedback Voltage Line Regulation</td>
<td>$2.0V \leq V_{IN} \leq 12.0V$</td>
<td>0.013</td>
<td>0.1</td>
<td></td>
<td>%/V</td>
</tr>
<tr>
<td>IB</td>
<td>FB Pin Bias Current</td>
<td></td>
<td>0.5</td>
<td>20</td>
<td></td>
<td>nA</td>
</tr>
</tbody>
</table>

(1) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

(2) Typical numbers are at 25 °C and represent the most likely norm.

(3) Duty cycle affects current limit due to ramp generator.

(4) Current limit at 0% duty cycle. See Typical Performance Characteristics section for Switch Current Limit vs. $V_{IN}$

(5) Bias current flows into FB pin.
Electrical Characteristics (continued)

Specifications in standard type face are for $T_J = 25^\circ C$ and those with **boldface type** apply over the full **Operating Temperature Range** ($T_J = -40^\circ C$ to $+125^\circ C$) unless otherwise specified. $V_{IN} = 2.0V$ and $I_{L} = 0A$, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min (1)</th>
<th>Typ (2)</th>
<th>Max (3)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input Voltage Range</td>
<td></td>
<td>2</td>
<td>12</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$g_m$</td>
<td>Error Amp Transconductance</td>
<td>$\Delta I = 5\mu A$</td>
<td>40</td>
<td>135</td>
<td>290</td>
<td>$\mu$mho</td>
</tr>
<tr>
<td>$A_V$</td>
<td>Error Amp Voltage Gain</td>
<td></td>
<td>135</td>
<td></td>
<td></td>
<td>V/V</td>
</tr>
<tr>
<td>$D_{MAX}$</td>
<td>Maximum Duty Cycle</td>
<td></td>
<td>78</td>
<td>85</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$f_S$</td>
<td>Switching Frequency</td>
<td>FSLCT = Ground</td>
<td>480</td>
<td>600</td>
<td>720</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FSLCT = $V_{IN}$</td>
<td>1</td>
<td>1.25</td>
<td>1.5</td>
<td>MHz</td>
</tr>
<tr>
<td>$I_{SHDN}$</td>
<td>Shutdown Pin Current</td>
<td>$V_{SHDN} = V_{IN}$</td>
<td>0.01</td>
<td>0.1</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{SHDN} = 0V$</td>
<td>-0.5</td>
<td>-1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_L$</td>
<td>Switch Leakage Current</td>
<td>$V_{SW} = 18V$</td>
<td>0.01</td>
<td>3</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$R_{DSON}$</td>
<td>Switch $R_{DSON}$</td>
<td>$V_{IN} = 2.7V$, $I_{SW} = 1A$</td>
<td>0.2</td>
<td>0.4</td>
<td></td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$T_{THSHDN}$</td>
<td>SHDN Threshold</td>
<td>Output High</td>
<td>0.9</td>
<td>0.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output Low</td>
<td>0.6</td>
<td>0.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>UVP</td>
<td>On Threshold</td>
<td></td>
<td>1.8</td>
<td>1.92</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Off Threshold</td>
<td></td>
<td>1.7</td>
<td>1.82</td>
<td>1.9</td>
<td>V</td>
</tr>
<tr>
<td>$\theta_{JA}$</td>
<td>Thermal Resistance</td>
<td>Junction to Ambient$^{(6)}$</td>
<td>235</td>
<td></td>
<td></td>
<td>$^\circ$C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Junction to Ambient$^{(7)}$</td>
<td>225</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Junction to Ambient$^{(8)}$</td>
<td>220</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Junction to Ambient$^{(9)}$</td>
<td>200</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Junction to Ambient$^{(10)}$</td>
<td>195</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(6) Junction to ambient thermal resistance (no external heat sink) for the VSSOP package with minimal trace widths (0.010 inches) from the pins to the circuit. See “Scenario ‘A’” in the Power Dissipation section.

(7) Junction to ambient thermal resistance for the VSSOP package with minimal trace widths (0.010 inches) from the pins to the circuit and approximately 0.0191 sq. in. of copper heat sinking. See “Scenario ‘B’” in the Power Dissipation section.

(8) Junction to ambient thermal resistance for the VSSOP package with minimal trace widths (0.010 inches) from the pins to the circuit and approximately 0.0465 sq. in. of copper heat sinking. See “Scenario ‘C’” in the Power Dissipation section.

(9) Junction to ambient thermal resistance for the VSSOP package with minimal trace widths (0.010 inches) from the pins to the circuit and approximately 0.2523 sq. in. of copper heat sinking. See “Scenario ‘D’” in the Power Dissipation section.

(10) Junction to ambient thermal resistance for the VSSOP package with minimal trace widths (0.010 inches) from the pins to the circuit and approximately 0.0098 sq. in. of copper heat sinking on the top layer and 0.0760 sq. in. of copper heat sinking on the bottom layer, with three 0.020 in. vias connecting the planes. See “Scenario ‘E’” in the Power Dissipation section.
Typical Performance Characteristics

Efficiency vs. Load Current
\(V_{\text{OUT}} = 8\text{V}, f_s = 600\text{ kHz}\)

Figure 3.

Efficiency vs. Load Current
\(V_{\text{OUT}} = 8\text{V}, f_s = 1.3\text{ MHz}\)

Figure 4.

Switch Current Limit vs. Temperature
\(V_{\text{IN}} = 3.3\text{V}, V_{\text{OUT}} = 8\text{V}\)

Figure 5.

Switch Current Limit vs. \(V_{\text{IN}}\)
\(V_{\text{OUT}} = 8\text{V}, V_{\text{OUT}} = 12\text{V}\)

Figure 6.

\(R_{\text{DS(ON)}}\) vs. \(V_{\text{IN}}\)
\(I_{\text{SW}} = 1\text{A}\)

Figure 7.

\(I_{Q}\) vs. \(V_{\text{IN}}\)
\(600\text{ kHz}, \text{not switching}\)

Figure 8.
Typical Performance Characteristics (continued)

Figure 9. \( I_Q \) vs. \( V_{IN} \) (600 kHz, switching)

Figure 10. \( I_Q \) vs. \( V_{IN} \) (1.3 MHz, not switching)

Figure 11. \( I_Q \) vs. \( V_{IN} \) (1.3 MHz, switching) (In shutdown)

Figure 12. \( I_Q \) vs. \( V_{IN} \)

Figure 13. Frequency vs. \( V_{IN} \) (600 kHz)

Figure 14. Frequency vs. \( V_{IN} \) (1.3 MHz)
Typical Performance Characteristics (continued)

Load Transient Response
(600 kHz operation)

Test circuit is shown in Figure 20.

Figure 15.

Load Transient Response
(1.3 MHz operation)

Test circuit is shown in Figure 21.

Figure 16.
OPERATION

CONTINUOUS CONDUCTION MODE

The LM2622 is a current-mode, PWM boost regulator. A boost regulator steps the input voltage up to a higher output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles.

In the first cycle of operation, shown in Figure 17 (a), the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by $C_{OUT}$.

The second cycle is shown in Figure 17 (b). During this cycle, the transistor is open and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:

$$V_{OUT} = \frac{V_{IN}}{1-D}, D' = (1-D) = \frac{V_{IN}}{V_{OUT}}$$

where

- $D$ is the duty cycle of the switch
- $D$ and $D'$ will be required for design calculations

(1)

SETTING THE OUTPUT VOLTAGE

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown in the typical operating circuit. The feedback pin voltage is 1.26V, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} \cdot 1.26}{1.26} \Omega$$

(2)
The LM2622 is a current mode PWM boost converter. The signal flow of this control scheme has two feedback loops, one that senses switch current and one that senses output voltage.

To keep a current programmed control converter stable above duty cycles of 50%, the inductor must meet certain criteria. The inductor, along with input and output voltage, will determine the slope of the current through the inductor (see Figure 18 (a)). If the slope of the inductor current is too great, the circuit will be unstable above duty cycles of 50%. A 10 µH inductor is recommended for most 600 kHz applications, while a 4.7 µH inductor may be used for most 1.25 MHz applications. If the duty cycle is approaching the maximum of 85%, it may be necessary to increase the inductance by as much as 2X. See INDUCTOR AND DIODE SELECTION for more detailed inductor sizing.

The LM2622 provides a compensation pin (V_C) to customize the voltage loop feedback. It is recommended that a series combination of R_C and C_C be used for the compensation network, as shown in the typical application circuit. For any given application, there exists a unique combination of R_C and C_C that will optimize the performance of the LM2622 circuit in terms of its transient response. The series combination of R_C and C_C introduces a pole-zero pair according to the following equations:

(a) Inductor current
(b) Diode current

Figure 18.
\[ f_{zc} = \frac{1}{2\pi R C c} \text{ Hz} \]  
\[ f_{zc} = \frac{1}{2\pi (R_c + R_o) C c} \text{ Hz} \]

where
- \( R_o \) is the output impedance of the error amplifier, approximately 1\,\text{Meg}Ω

For most applications, performance can be optimized by choosing values within the range 5\,\Omega \leq R_c \leq 20\,\Omega (R_c can be up to 200\,\Omega if \( C_{C2} \) is used, see HIGH OUTPUT CAPACITOR ESR COMPENSATION) and 680\,\text{pF} \leq C_c \leq 4.7\,\text{nF}. Refer to the Application Information section for recommended values for specific circuits and conditions. Refer to the COMPENSATION section for other design requirements.

**COMPENSATION**

This section will present a general design procedure to help insure a stable and operational circuit. The designs in this datasheet are optimized for particular requirements. If different conversions are required, some of the components may need to be changed to ensure stability. Below is a set of general guidelines in designing a stable circuit for continuous conduction operation (loads greater than approximately 75mA), in most all cases this will provide for stability during discontinuous operation as well. The power components and their effects will be determined first, then the compensation components will be chosen to produce stability.

**INDUCTOR AND DIODE SELECTION**

Although the inductor sizes mentioned earlier are fine for most applications, a more exact value can be calculated. To ensure stability at duty cycles above 50\%, the inductor must have some minimum value determined by the minimum input voltage and the maximum output voltage. This equation is:

\[ L > \frac{V_{IN} R_{DSON}}{0.144 \, f_s} \left( \frac{D}{D'} \right)^2 \left( 1 + \frac{D}{D'} \right) \text{ (in H)} \]

where
- \( f_s \) is the switching frequency
- \( D \) is the duty cycle
- \( R_{DSON} \) is the ON resistance of the internal switch taken from the graph "\( R_{DSON} \) vs. \( V_{IN} \)" in the Typical Performance Characteristics section

This equation is only good for duty cycles greater than 50\% (\( D > 0.5 \)), for duty cycles less than 50\% the recommended values may be used. The corresponding inductor current ripple as shown in Figure 18 (a) is given by:

\[ \Delta i_l = \frac{V_{IN} D}{2 L f_s} \text{ (in Amps)} \]

The inductor ripple current is important for a few reasons. One reason is because the peak switch current will be the average inductor current (input current or \( I_{LOAD}/D' \)) plus \( \Delta i_l \). As a side note, discontinuous operation occurs when the inductor current falls to zero during a switching cycle, or \( \Delta i_l \) is greater than the average inductor current. Therefore, continuous conduction mode occurs when \( \Delta i_l \) is less than the average inductor current. Care must be taken to make sure that the switch will not reach its current limit during normal operation. The inductor must also be sized accordingly. It should have a saturation current rating higher than the peak inductor current expected. The output voltage ripple is also affected by the total ripple current.

The output diode for a boost regulator must be chosen correctly depending on the output voltage and the output current. The typical current waveform for the diode in continuous conduction mode is shown in Figure 18 (b). The diode must be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. During short circuit testing, or if short circuit conditions are possible in the application, the diode current rating must exceed the switch current limit. Using Schottky diodes with lower forward voltage drop will decrease power dissipation and increase efficiency.
DC GAIN AND OPEN-LOOP GAIN

Since the control stage of the converter forms a complete feedback loop with the power components, it forms a closed-loop system that must be stabilized to avoid positive feedback and instability. A value for open-loop DC gain will be required, from which you can calculate, or place, poles and zeros to determine the crossover frequency and the phase margin. A high phase margin (greater than 45°) is desired for the best stability and transient response. For the purpose of stabilizing the LM2622, choosing a crossover point well below where the right half plane zero is located will ensure sufficient phase margin. A discussion of the right half plane zero and checking the crossover using the DC gain will follow.

INPUT AND OUTPUT CAPACITOR SELECTION

The switching action of a boost regulator causes a triangular voltage waveform at the input. A capacitor is required to reduce the input ripple and noise for proper operation of the regulator. The size used is dependant on the application and board layout. If the regulator will be loaded uniformly, with very little load changes, and at lower current outputs, the input capacitor size can often be reduced. The size can also be reduced if the input of the regulator is very close to the source output. The size will generally need to be larger for applications where the regulator is supplying nearly the maximum rated output or if large load steps are expected. A minimum value of 10µF should be used for the less stressful conditions while a 22µF to 47µF capacitor may be required for higher power and dynamic loads. Larger values and/or lower ESR may be needed if the application requires very low ripple on the input source voltage.

The choice of output capacitors is also somewhat arbitrary and depends on the design requirements for output voltage ripple. It is recommended that low ESR (Equivalent Series Resistance, denoted R_{ESR}) capacitors be used such as ceramic, polymer electrolytic, or low ESR tantalum. Higher ESR capacitors may be used but will require more compensation which will be explained later on in the section. The ESR is also important because it determines the peak to peak output voltage ripple according to the approximate equation:

\[ \Delta V_{OUT} \approx 2\Delta i_L R_{ESR} \text{ (in Volts)} \]  \hspace{1cm} (7)

A minimum value of 10µF is recommended and may be increased to a larger value. After choosing the output capacitor you can determine a pole-zero pair introduced into the control loop by the following equations:

\[ f_{P1} = \frac{1}{2\pi R_L C_{OUT}} \text{ (in Hz)} \]  \hspace{1cm} (8)

where

\[ f_{Z1} = \frac{1}{2\pi R_{ESR} C_{OUT}} \text{ (in Hz)} \]  \hspace{1cm} (9)

The zero created by the ESR of the output capacitor is generally very high frequency if the ESR is small. If low ESR capacitors are used it can be neglected. If higher ESR capacitors are used see the HIGH OUTPUT CAPACITOR ESR COMPENSATION section.

RIGHT HALF PLANE ZERO

A current mode control boost regulator has an inherent right half plane zero (RHP zero). This zero has the effect of a zero in the gain plot, causing an imposed +20dB/decade on the rolloff, but has the effect of a pole in the phase, subtracting another 90° in the phase plot. This can cause undesirable effects if the control loop is influenced by this zero. To ensure the RHP zero does not cause instability issues, the control loop should be designed to have a bandwidth of less than ½ the frequency of the RHP zero. This zero occurs at a frequency of:

\[ f_{RHP} = \frac{V_{OUT}(D)^3}{2\pi I_{LOAD} L} \text{ (in Hz)} \]  \hspace{1cm} (10)

where

\[ I_{LOAD} \] is the maximum load current
SELECTING THE COMPENSATION COMPONENTS

The first step in selecting the compensation components \( R_C \) and \( C_C \) is to set a dominant low frequency pole in the control loop. Simply choose values for \( R_C \) and \( C_C \) within the ranges given in the INTRODUCTION TO COMPENSATION section to set this pole in the area of 10Hz to 500Hz. The frequency of the pole created is determined by the equation:

\[
f_{PC} = \frac{1}{2\pi(R_C + R_O)C_C} \text{ (in Hz)}
\]

where

- \( R_O \) is the output impedance of the error amplifier, approximately 1\( \text{M} \Omega \) \( (11) \)

Since \( R_C \) is generally much less than \( R_O \), it does not have much effect on the above equation and can be neglected until a value is chosen to set the zero \( f_{ZC} \). \( f_{ZC} \) is created to cancel out the pole created by the output capacitor, \( f_{P1} \). The output capacitor pole will shift with different load currents as shown by the equation, so setting the zero is not exact. Determine the range of \( f_{P1} \) over the expected loads and then set the zero \( f_{ZC} \) to a point approximately in the middle. The frequency of this zero is determined by:

\[
f_{ZC} = \frac{1}{2\pi C_C R_C} \text{ (in Hz)}
\]

Now \( R_C \) can be chosen with the selected value for \( C_C \). Check to make sure that the pole \( f_{PC} \) is still in the 10Hz to 500Hz range, change each value slightly if needed to ensure both component values are in the recommended range. After checking the design at the end of this section, these values can be changed a little more to optimize performance if desired. This is best done in the lab on a bench, checking the load step response with different values until the ringing and overshoot on the output voltage at the edge of the load steps is minimal. This should produce a stable, high performance circuit. For improved transient response, higher values of \( R_C \) should be chosen. This will improve the overall bandwidth which makes the regulator respond more quickly to transients. If more detail is required, or the most optimal performance is desired, refer to a more in depth discussion of compensating current mode DC/DC switching regulators.

HIGH OUTPUT CAPACITOR ESR COMPENSATION

When using an output capacitor with a high ESR value, or just to improve the overall phase margin of the control loop, another pole may be introduced to cancel the zero created by the ESR. This is accomplished by adding another capacitor, \( C_{C2} \), directly from the compensation pin \( V_C \) to ground, in parallel with the series combination of \( R_C \) and \( C_C \). The pole should be placed at the same frequency as \( f_{Z1} \), the ESR zero. The equation for this pole follows:

\[
f_{PC2} = \frac{1}{2\pi C_{C2}(R_C + R_O)} \text{ (in Hz)}
\]

To ensure this equation is valid, and that \( C_{C2} \) can be used without negatively impacting the effects of \( R_C \) and \( C_C \), \( f_{PC2} \) must be greater than \( 10f_{ZC} \).

CHECKING THE DESIGN

The final step is to check the design. This is to ensure a bandwidth of \( \frac{1}{2} \) or less of the frequency of the RHP zero. This is done by calculating the open-loop DC gain, \( A_{DC} \). After this value is known, you can calculate the crossover visually by placing a \(-20\text{dB/decade}\) slope at each pole, and a \(+20\text{dB/decade}\) slope for each zero. The point at which the gain plot crosses unity gain, or 0dB, is the crossover frequency. If the crossover frequency is less than \( \frac{1}{2} \) the RHP zero, the phase margin should be high enough for stability. The phase margin can also be improved by adding \( C_{C2} \) as discussed earlier in the section. The equation for \( A_{DC} \) is given below with additional equations required for the calculation:

\[
A_{DC(\text{dB})} = 20\log_{10}\left(\frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right) g_m R_O D' \left\{\frac{I_o(0\text{Cleft})/R_L}{I_o/R_L}\right\} \text{ (in dB)}
\]

where

- \( R_L \) is the minimum load resistance
- \( g_m \) is the error amplifier transconductance found in the Electrical Characteristics table \( (14) \)
- \( o_C \approx \frac{2f_s}{nD'} \text{ (in rad/s)} \) \( (15) \)
\[ L_{\text{eff}} = \frac{L}{(D')^2} \]  

\[ n = 1 + \frac{2mc}{m_1} \text{ (no unit)} \]  

\[ m_1 \geq \frac{V_{\text{IN}}R_{\text{DSON}}}{L} \text{ (in V/s)} \]  

where

- \( V_{\text{IN}} \) is the minimum input voltage
- \( R_{\text{DSON}} \) is the value chosen from the graph "\( R_{\text{DSON}} \) vs. \( V_{\text{IN}} \)" in the Typical Performance Characteristics section  

LAYOUT CONSIDERATIONS

The input bypass capacitor \( C_{\text{IN}} \), as shown in the typical operating circuit, must be placed close to the IC. This will reduce copper trace resistance which affects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with \( C_{\text{IN}} \) close to the \( V_{\text{IN}} \) pin, to shunt any high frequency noise to ground. The output capacitor, \( C_{\text{OUT}} \), should also be placed close to the IC. Any copper trace connections for the \( C_{\text{OUT}} \) capacitor can increase the series resistance, which directly affects output voltage ripple. The feedback network, resistors \( R_{\text{FB1}} \) and \( R_{\text{FB2}} \), should be kept close to the FB pin, and away from the inductor, to minimize copper trace connections that can inject noise into the system. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. For more detail on switching power supply layout considerations see Application Note AN-1149: Layout Guidelines for Switching Power Supplies (SNVA021).
TRIPLE OUTPUT TFT BIAS

The circuit in Figure 19 shows how the LM2622 can be configured to provide outputs of 8V, −8V, and 23V, convenient for biasing TFT displays. The 8V output is regulated, while the −8V and 23V outputs are unregulated.

The 8V output is generated by a typical boost topology. The basic operation of the boost converter is described in the OPERATION section. The output voltage is set with $R_{FB1}$ and $R_{FB2}$ by:

$$R_{FB1} = R_{FB2} \frac{V_{OUT} - 1.26}{1.26} \Omega$$  \hspace{1cm} (20)

$C_{FB}$ is placed across $R_{FB1}$ to act as a pseudo soft-start. The compensation network of $R_C$ and $C_C$ are chosen to optimally stabilize the converter. The inductor also affects the stability. When operating at 600 kHz, a 10uH inductor is recommended to insure the converter is stable at duty cycles greater than 50%. Refer to the COMPENSATION section for more information.

The −8V output is derived from a diode inverter. During the second cycle, when the transistor is open, D2 conducts and C1 charges to 8V minus a diode drop ($\approx 0.4V$ if using a Schottky). When the transistor opens in the first cycle, D3 conducts and C1’s polarity is reversed with respect to the output at C2, producing -8V.

The 23V output is realized with a series of capacitor charge pumps. It consists of four stages: the first stage includes C4, D4, and the LM2622 switch; the second stage uses C5, D5, and D1; the third stage includes C6, D6, and the LM2622 switch; the final stage is C7 and D7. In the first stage, C4 charges to 8V when the LM2622 switch is closed, which causes D5 to conduct when the switch is open. In the second stage, the voltage across C5 is $V_{C4} + V_{D1} - V_{D5} = V_{C4} = 8V$ when the switch is open. However, because C5 is referenced to the 8V
output, the voltage at C5 is 16V when referenced to ground. In the third stage, the 16V at C5 appears across C6 when the switch is closed. When the switch opens, C6 is referenced to the 8V output minus a diode drop, which raises the voltage at C6 with respect to ground to about 24V. Hence, in the fourth stage, C7 is charged to 24V when the switch is open. From the first stage to the last, there are three diode drops that make the output voltage closer to 24 - 3xVDIODE (about 22.8V if a 0.4V forward drop is assumed).

Table 1. Components For Circuits in Figure 19

<table>
<thead>
<tr>
<th>Component</th>
<th>600 kHz</th>
<th>1.3 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>10µH</td>
<td>4.7µH</td>
</tr>
<tr>
<td>COUT1</td>
<td>10µF</td>
<td>22µF</td>
</tr>
<tr>
<td>COUT2</td>
<td>10µF</td>
<td>NOT USED</td>
</tr>
<tr>
<td>CC</td>
<td>3.9nF</td>
<td>1.5nF</td>
</tr>
<tr>
<td>CFB1</td>
<td>0.1µF</td>
<td>15nF</td>
</tr>
<tr>
<td>CFB2</td>
<td>NOT USED</td>
<td>560pF</td>
</tr>
<tr>
<td>CIN</td>
<td>10µF</td>
<td>22µF</td>
</tr>
<tr>
<td>C1</td>
<td>4.7µF</td>
<td>4.7µF</td>
</tr>
<tr>
<td>C2</td>
<td>0.1µF</td>
<td>0.1µF</td>
</tr>
<tr>
<td>C4</td>
<td>1µF</td>
<td>1µF</td>
</tr>
<tr>
<td>C5</td>
<td>1µF</td>
<td>1µF</td>
</tr>
<tr>
<td>C6</td>
<td>1µF</td>
<td>1µF</td>
</tr>
<tr>
<td>C7</td>
<td>1µF</td>
<td>1µF</td>
</tr>
<tr>
<td>RFB1</td>
<td>40.2kΩ</td>
<td>91kΩ</td>
</tr>
<tr>
<td>RFB2</td>
<td>7.5kΩ</td>
<td>18kΩ</td>
</tr>
<tr>
<td>RC</td>
<td>5.1kΩ</td>
<td>10kΩ</td>
</tr>
<tr>
<td>D1</td>
<td>MBRM140T3</td>
<td>MBRM140T3</td>
</tr>
<tr>
<td>D2</td>
<td>BAT54S</td>
<td>BAT54S</td>
</tr>
<tr>
<td>D3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td>BAT54S</td>
<td>BAT54S</td>
</tr>
<tr>
<td>D5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D6</td>
<td>BAT54S</td>
<td>BAT54S</td>
</tr>
<tr>
<td>D7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
600 KHZ OPERATION

![Diagram of 600 kHz operation](image)

Figure 20. 600 kHz operation

1.3 MHZ OPERATION

![Diagram of 1.3 MHz operation](image)

Figure 21. 1.3 MHz operation
POWER DISSIPATION

The output power of the LM2622 is limited by its maximum power dissipation. The maximum power dissipation is determined by the formula

\[ P_D = \frac{(T_{j\text{max}} - T_A)}{\theta_{JA}} \]

where

- \( T_{j\text{max}} \) is the maximum specified junction temperature (125°C)
- \( T_A \) is the ambient temperature
- \( \theta_{JA} \) is the thermal resistance of the package

\( \theta_{JA} \) is dependant on the layout of the board as shown below.
SCENARIO 'C'
(0.0465 sq. in. Copper)

SCENARIO 'D'
(0.2523 sq. in. Copper)
SCENARIO 'E'
(0.0098 sq. in. Copper [TOP])
(0.0760 sq. in. Copper [BOTTOM])

$\theta_{ja} = 195^\circ C/W$
## REVISION HISTORY

**Changes from Revision D (March 2013) to Revision E**

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changed layout of National Data Sheet to TI format</td>
<td>20</td>
</tr>
</tbody>
</table>
## Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2622MM-ADJ/NOPB</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>S18B</td>
<td>Samples</td>
</tr>
<tr>
<td>LM2622MMX-ADJ/NOPB</td>
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<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>3500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>S18B</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

- **K0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **A0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width (W1)**

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Sprocket Holes**
- **User Direction of Feed**
- **Pocket Quadrants**

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
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<tr>
<td>LM2622MM-ADJ/NOPB</td>
<td>VSSOP</td>
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<td>178.0</td>
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<td>5.3</td>
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<td>12.0</td>
<td>Q1</td>
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<tr>
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<td>DGK</td>
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<td>3500</td>
<td>330.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
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<tr>
<th>Device</th>
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<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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<tr>
<td>LM2622MMX-ADJ/NOPB</td>
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<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.
NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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