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# LP38851 800 mA Fast-Response High-Accuracy Adjustable LDO Linear Regulator with Enable and Soft-Start

Check for Samples: LP38851

## **FEATURES**

- Adjustable V<sub>OUT</sub> Range of 0.80V to 1.8V
- Wide V<sub>BIAS</sub> Supply Operating Range of 3.0V to 5.5V
- Stable with 10µF Ceramic Capacitors
- Dropout Voltage of 115 mV (Typical) at 800 mA Load Current
- Precision V<sub>ADJ</sub> across All Line and Load Conditions:
  - ±1.5%  $V_{ADJ}$  for  $T_J = 25$ °C
  - ±2.0% V<sub>ADJ</sub> for 0°C ≤ T<sub>J</sub> ≤ +125°C
  - $\pm 3.0\%$  V<sub>ADJ</sub> for -40°C ≤ T<sub>J</sub> ≤ +125°C
- Over-Temperature and Over-Current Protection
- Available in 8-Lead SO PowerPad,
   7-Lead SFM and 7-Lead PFM Packages
- -40°C to +125°C Operating Junction Temperature Range

# **APPLICATIONS**

- ASIC Power Supplies in:
  - Desktops, Notebooks, and Graphics Cards, Servers
  - Gaming Set Top Boxes, Printers and Copiers
- Server Core and I/O Supplies
- DSP and FPGA Power Supplies
- SMPS Post-Regulator

#### DESCRIPTION

The LP38851-ADJ is a high current, fast response regulator which can maintain output voltage regulation with extremely low input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages:  $V_{BIAS}$  provides voltage to drive the gate of the N-MOS power transistor, while  $V_{IN}$  is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low  $V_{IN}$  voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of this device makes it suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The part is available in PSOP 8-pin, SFM 7-pin, and TO-263 7-pin packages.

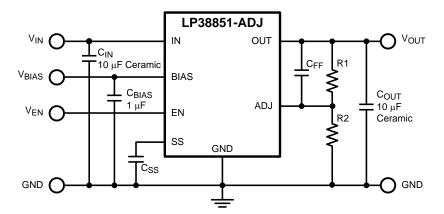
- Dropout Voltage: 115 mV (typical) at 800 mA load current
- Low Ground Pin Current: 10 mA (typical) at 800 mA load current
- Soft-Start: Programmable Soft-Start time
- Precision ADJ Voltage: ±1.5% for T<sub>J</sub> = 25°C, and ±2.0% for 0°C ≤ T<sub>J</sub> ≤ +125°C, across all line and load conditions

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## TYPICAL APPLICATION CIRCUIT



# **Connection Diagram**

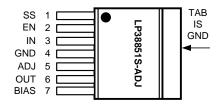


Figure 1. 7-Lead PFM - Top View See KTW0007B Package

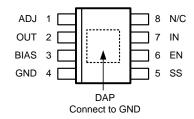


Figure 3. 8-Lead SO PowerPad - Top View See DDA Package

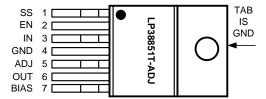


Figure 2. 7-Lead SFM - Top View See NDZ0007B Package

# **PIN DESCRIPTIONS**

SFM Pin #	PFM Pin #	SO PowerPad Pin #	Pin Symbol	Pin Description
1	1	5	SS	Soft-Start capacitor connection. Used to control the rise time of $V_{\text{OUT}}$ at turn-on.
2	2	6	EN	Device Enable, High = On, Low = Off.
3	3	7	IN	The unregulated voltage input
4	4	4	GND	Ground
5	5	1	ADJ	The feedback connection to set the output voltage
6	6	2	OUT	The regulated output voltage
7	7	3	BIAS	The supply for the internal control and reference circuitry.
-	-	8	N/C	No internal connection
TAB	TAB	-	TAB	The SFM and PFM TAB is a thermal and electrical connection that is physically attached to the backside of the die, and used as a thermal heat-sink connection. See APPLICATION INFORMATION for details.



#### PIN DESCRIPTIONS (continued)

SFM	PFM	SO PowerPad	Pin	Pin Description
Pin #	Pin #	Pin #	Symbol	
-	-	DAP	DAP	The SO PowerPad DAP is a thermal connection only that is physically attached to the backside of the die, and used as a thermal heat-sink connection. See APPLICATION INFORMATION for details.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

# ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature Range		−65°C to +150°C
Lead Temperature	Soldering, 5 seconds	260°C
ESD Rating	Human Body Model (2)	±2 kV
Power Dissipation (3)		Internally Limited
V <sub>IN</sub> Supply Voltage (Survival)		-0.3V to +6.0V
V <sub>BIAS</sub> Supply Voltage (Surviva	ıl)	-0.3V to +6.0V
V <sub>SS</sub> SoftStart Voltage (Surviva	al)	-0.3V to +6.0V
V <sub>OUT</sub> Voltage (Survival)		-0.3V to +6.0V
I <sub>OUT</sub> Current (Survival)		Internally Limited
Junction Temperature		-40°C to +150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For specifications and conditions, see the Electrical Characteristics.
- (2) The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin. Test method is per JESD22-A114.
- (3) Device power dissipation must be de-rated based on device power dissipation (P<sub>D</sub>), ambient temperature (T<sub>A</sub>), and package junction to ambient thermal resistance (θ<sub>JA</sub>). Additional heat-sinking may be required to ensure that the device junction temperature (T<sub>J</sub>) does not exceed the maximum operating rating. See APPLICATION INFORMATION for details.

## OPERATING RATINGS (1)

V <sub>IN</sub> Supply Voltage		(V <sub>OUT</sub> + V <sub>DO</sub> ) to V <sub>BIAS</sub>
V Cupply Voltage	tage $\frac{0.8 \text{V} \leq \text{V}_{\text{OUT}} \leq 1.2 \text{V}}{1.2 \text{V} < \text{V}_{\text{OUT}} \leq 1.8 \text{V}}$	3.0V to 5.5V
V <sub>BIAS</sub> Supply Voltage	1.2V < V <sub>OUT</sub> ≤ 1.8V	4.5V to 5.5V
V <sub>EN</sub> Voltage		0.0V to V <sub>BIAS</sub>
l <sub>OUT</sub>		0 mA to 800 mA
Junction Temperature Range (2)		-40°C to +125°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For specifications and conditions, see the Electrical Characteristics.
- (2) Device power dissipation must be de-rated based on device power dissipation (P<sub>D</sub>), ambient temperature (T<sub>A</sub>), and package junction to ambient thermal resistance (θ<sub>JA</sub>). Additional heat-sinking may be required to ensure that the device junction temperature (T<sub>J</sub>) does not exceed the maximum operating rating. See APPLICATION INFORMATION for details.



# **ELECTRICAL CHARACTERISTICS**

Unless otherwise specified:  $V_{OUT} = 0.80V$ ,  $V_{IN} = V_{OUT(NOM)} + 1V$ ,  $V_{BIAS} = 3.0V$ ,  $V_{EN} = V_{BIAS}$ ,  $I_{OUT} = 10$  mA,  $C_{IN} = C_{OUT} = 10$   $\mu$ F,  $C_{BIAS} = 1$   $\mu$ F,  $C_{SS} = open$ . Limits in standard type are for  $T_J = 25^{\circ}$ C only; limits in **boldface type** apply over the junction temperature  $(T_J)$  range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^{\circ}$ C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
		$V_{OUT(NOM)}$ +1V $\leq$ $V_{IN} \leq$ $V_{BIAS} \leq$ 4.5V <sup>(1)</sup> 3.0V $\leq$ $V_{BIAS} \leq$ 5.5V, 10 mA $\leq$ $I_{OUT} \leq$ 800 mA	492.5 <b>485.0</b>	500.	507.5 <b>515.0</b>	
$V_{ADJ}$	V <sub>ADJ</sub> Accuracy	$\begin{split} &V_{OUT(NOM)} \! \! + \! 1 V \leq V_{IN} \leq V_{BIAS} \leq 4.5 V^{~(1)} \\ &3.0 V \leq V_{BIAS} \leq 5.5 V, \\ &10 \text{ mA} \leq I_{OUT} \leq 800 \text{ mA}, \\ &0^{\circ} C \leq T_{J} \leq + 125^{\circ} C \end{split}$	490.0	500.	510.0	mV
V <sub>OUT</sub>	V <sub>OUT</sub> Range	$3.0V \le V_{BIAS} \le 5.5V$	0.80		1.20	V
VOU1		4.5V ≤ V <sub>BIAS</sub> ≤ 5.5V	0.80		1.80	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation, V <sub>IN</sub> <sup>(2)</sup>	$V_{OUT(NOM)} + 1V \le V_{IN} \le V_{BIAS}$	-	0.04	-	%/V
$\Delta V_{OUT}/\Delta V_{BIAS}$	Line Regulation, V <sub>BIAS</sub> <sup>(2)</sup>	3.0V ≤ V <sub>BIAS</sub> ≤ 5.5V	-	0.10	-	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output Voltage Load Regulation (3)	10 mA ≤ I <sub>OUT</sub> ≤ 800 mA	-	0.2	-	%/A
$V_{DO}$	Dropout Voltage (4)	I <sub>OUT</sub> = 800 mA	-	115	150 <b>200</b>	mV
I <sub>GND(IN)</sub>	Quiescent Current Drawn from V <sub>IN</sub>	$V_{OUT} = 0.80V$ $V_{BIAS} = 3.0V$ 10 mA $\leq I_{OUT} \leq 800$ mA	-	7.0	8.5 <b>9.0</b>	mA
( <i>y</i>	Supply	V <sub>EN</sub> ≤ 0.5V		1	100 <b>300</b>	μΑ
	Quiescent Current Drawn from	10 mA ≤ I <sub>OUT</sub> ≤ 800 mA	-	3.0	3.8 <b>4.5</b>	mA
I <sub>GND</sub> (BIAS)	V <sub>BIAS</sub> Supply	V <sub>EN</sub> ≤ 0.5V		100	170 <b>200</b>	μΑ
UVLO	Under-Voltage Lock-Out Threshold	V <sub>BIAS</sub> rising until device is functional	2.20 <b>2.00</b>	2.45	2.70 <b>2.90</b>	V
UVLO <sub>(HYS)</sub>	Under-Voltage Lock-Out Hysteresis	V <sub>BIAS</sub> falling from UVLO threshold until device is non-functional	60 <b>50</b>	150	300 <b>350</b>	mV
I <sub>SC</sub>	Output Short-Circuit Current	$\begin{aligned} V_{\text{IN}} &= V_{\text{OUT(NOM)}} + 1V, \\ V_{\text{BIAS}} &= 3.0V, V_{\text{OUT}} = 0.0V \end{aligned}$	-	2.3	-	Α
Soft-Start						
r <sub>SS</sub>	Soft-Start internal resistance		11.0	14.0	17.0	kΩ
t <sub>SS</sub>	Soft-Start time $t_{SS} = C_{SS} \times r_{SS} \times 5$	C <sub>SS</sub> = 10 nF	-	700	-	μs
Enable						
		$V_{EN} = V_{BIAS}$	-	0.01	-	
I <sub>EN</sub>	ENABLE pin Current	$V_{EN} = 0.0V, V_{BIAS} = 5.5V$	-24 <b>-21</b>	-35	-43 <b>-50</b>	μA
V <sub>EN(ON)</sub>	Enable Voltage Threshold	V <sub>EN</sub> rising until Output = ON	1.00 <b>0.90</b>	1.25	1.50 <b>1.55</b>	V
V <sub>EN(HYS)</sub>	Enable Voltage Hysteresis	$V_{EN}$ falling from $V_{EN(ON)}$ until Output = OFF	50 <b>30</b>	100	150 <b>200</b>	mV
t <sub>OFF</sub>	Turn-OFF Delay Time	R <sub>LOAD</sub> x C <sub>OUT</sub> << t <sub>OFF</sub>	-	20	-	
t <sub>ON</sub>	Turn-ON Delay Time	R <sub>LOAD</sub> x C <sub>OUT</sub> << t <sub>ON</sub>	-	15	-	μs
AC Parameters			-		<del></del>	

<sup>1)</sup>  $V_{IN}$  cannot exceed either  $V_{BIAS}$  or 4.5V, whichever value is lower.

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<sup>(2)</sup> Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.

<sup>(3)</sup> Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.

<sup>(4)</sup> Dropout voltage is defined as the input to output voltage differential (V<sub>IN</sub> - V<sub>OUT</sub>) where the input voltage is low enough to cause the output voltage to drop 2% from the nominal value.



# **ELECTRICAL CHARACTERISTICS (continued)**

Unless otherwise specified:  $V_{OUT} = 0.80V$ ,  $V_{IN} = V_{OUT(NOM)} + 1V$ ,  $V_{BIAS} = 3.0V$ ,  $V_{EN} = V_{BIAS}$ ,  $I_{OUT} = 10$  mA,  $C_{IN} = C_{OUT} = 10$   $\mu$ F,  $C_{BIAS} = 1$   $\mu$ F,  $C_{SS} = open$ . Limits in standard type are for  $T_J = 25^{\circ}$ C only; limits in **boldface type** apply over the junction temperature  $(T_J)$  range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^{\circ}$ C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
PSRR	Ripple Rejection for V <sub>IN</sub> Input	V <sub>IN</sub> = V <sub>OUT(NOM)</sub> + 1V, f = 120 Hz	-	72	-		
(V <sub>IN</sub> )	Voltage	$V_{IN} = V_{OUT(NOM)} + 1V,$ f = 1 kHz	-	61	-	40	
PSRR	Dinale Dejection for V Voltage	$V_{BIAS} = V_{OUT(NOM)} + 3V,$ f = 120 Hz	-	54	-	dB	
(V <sub>BIAS</sub> )	Ripple Rejection for V <sub>BIAS</sub> Voltage	$V_{BIAS} = V_{OUT(NOM)} + 3V,$ f = 1 kHz	-	53	-		
	Output Noise Density	f = 120 Hz	-	1	-	μV/√ <del>Hz</del>	
$e_n$	Output Nision Walters	BW = 10 Hz - 100 kHz	-	150	-		
	Output Noise Voltage	BW = 300 Hz - 300 kHz	-	90	-	μV <sub>RMS</sub>	
Thermal Para	meters						
T <sub>SD</sub>	Thermal Shutdown Junction Temperature		-	160	-	°C	
T <sub>SD(HYS)</sub>	Thermal Shutdown Hysteresis		-	10	-		
		SFM	-	60	-		
$\theta_{J\text{-}A}$	Thermal Resistance, Junction to Ambient <sup>(5)</sup>	PFM	-	60	-		
	7 41121311	SO PowerPad	-	168	-	°C/\/	
		SFM	-	3	-	°C/W	
$\theta_{\text{J-C}}$	Thermal Resistance, Junction to Case <sup>(5)(6)</sup>	PFM	-	3	-		
		SO PowerPad	-	11	-		

<sup>(5)</sup> Device power dissipation must be de-rated based on device power dissipation (P<sub>D</sub>), ambient temperature (T<sub>A</sub>), and package junction to ambient thermal resistance (θ<sub>JA</sub>). Additional heat-sinking may be required to ensure that the device junction temperature (T<sub>J</sub>) does not exceed the maximum operating rating. See APPLICATION INFORMATION for details.

<sup>(6)</sup> For SFM and PFM: θ<sub>J-C</sub> refers to the BOTTOM surface of the package, under the epoxy body, as the 'CASE'. For SO PowerPad: θ<sub>J-C</sub> refers to the DAP (aka: Exposed Pad) on BOTTOM surface of the package as the 'CASE'.



## TYPICAL PERFORMANCE CHARACTERISTICS

Refer to the TYPICAL APPLICATION CIRCUIT. Unless otherwise specified:  $T_J = 25$ °C,  $R1 = 1.40 \text{ k}\Omega$ ,  $R2 = 1.00 \text{ k}\Omega$ ,  $C_{FF}$ = 180 pF,  $V_{IN} = V_{OUT(NOM)} + 1V$ ,  $V_{BIAS} = 3.0V$ ,  $I_{OUT} = 10$  mA,  $C_{IN} = 10$   $\mu$ F Ceramic,  $C_{OUT} = 10$   $\mu$ F Ceramic,  $C_{\text{BIAS}}$  = 1  $\mu F$  Ceramic, ,  $C_{\text{SS}}$  = Open.

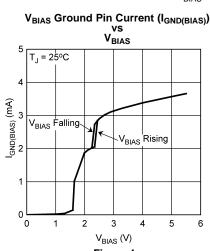


Figure 4.

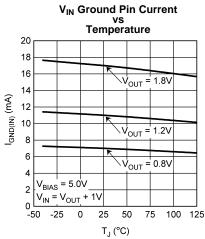
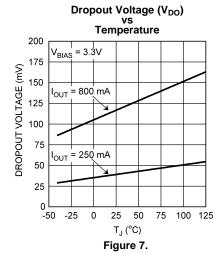
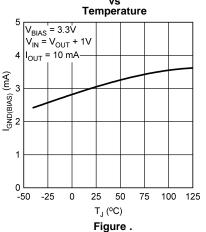


Figure 5.



V<sub>BIAS</sub> Ground Pin Current (I<sub>GND(BIAS)</sub>)



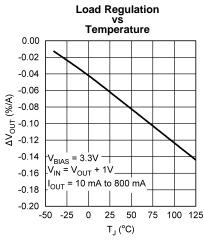


Figure 6.

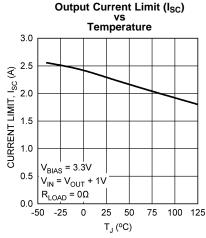
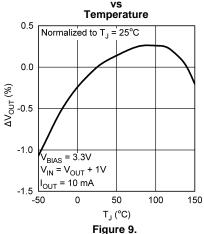


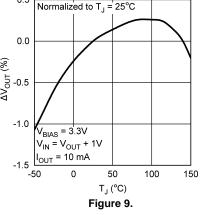
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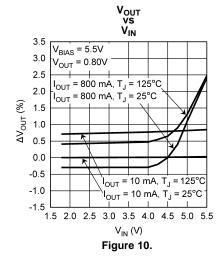


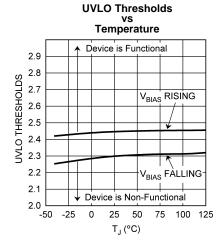
Refer to the TYPICAL APPLICATION CIRCUIT. Unless otherwise specified:  $T_J$  = 25°C, R1 = 1.40 k $\Omega$ , R2 = 1.00 k $\Omega$ ,

 $C_{FF} = 180 \text{ pF}, \ V_{IN} = V_{OUT(NOM)} + 1V, \ V_{BIAS} = 3.0V, \ I_{OUT} = 10 \text{ mA}, \ C_{IN} = 10 \text{ } \mu\text{F} \ Ceramic, \ C_{OUT} = 10 \text{ } \mu\text{F} \$ 









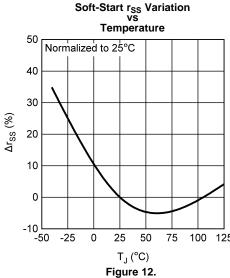
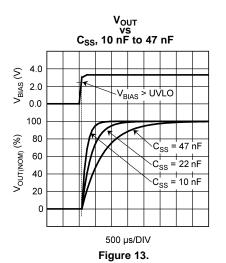


Figure 11.





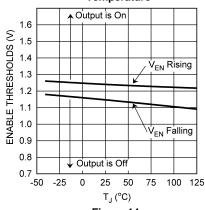
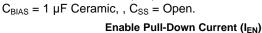


Figure 14.



Refer to the TYPICAL APPLICATION CIRCUIT. Unless otherwise specified:  $T_J = 25^{\circ}C$ ,  $R1 = 1.40 \text{ k}\Omega$ ,  $R2 = 1.00 \text{ k}\Omega$ ,  $C_{FF} = 180 \text{ pF}$ ,  $V_{IN} = V_{OUT(NOM)} + 1V$ ,  $V_{BIAS} = 3.0V$ ,  $I_{OUT} = 10 \text{ mA}$ ,  $C_{IN} = 10 \text{ }\mu\text{F}$  Ceramic,  $C_{OUT} = 10 \text{ }\mu\text{F}$  Ceramic,



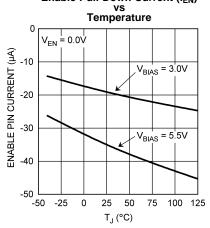


Figure 15.

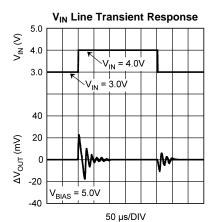
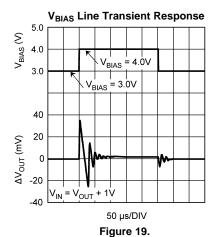


Figure 17.



Enable Pull-Up Resistor (r<sub>EN</sub>) vs Temperature

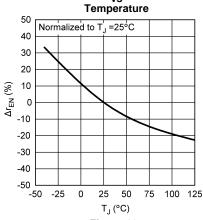


Figure 16.

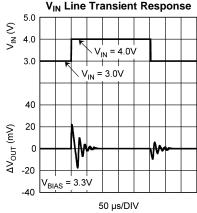


Figure 18.

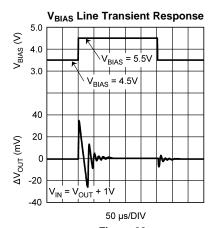


Figure 20.



Refer to the TYPICAL APPLICATION CIRCUIT. Unless otherwise specified:  $T_J$  = 25°C, R1 = 1.40 k $\Omega$ , R2 = 1.00 k $\Omega$ ,

 $C_{FF} = 180 \text{ pF}, \ V_{IN} = V_{OUT(NOM)} + 1V, \ V_{BIAS} = 3.0V, \ I_{OUT} = 10 \text{ mA}, \ C_{IN} = 10 \text{ } \mu\text{F} \text{ Ceramic}, \ C_{OUT} = 10 \text{ } \mu\text{F} \text{ Ceramic}, \$ 

 $C_{\rm BIAS}$  = 1  $\mu F$  Ceramic, ,  $C_{\rm SS}$  = Open. Load Transient Response,  $C_{\rm OUT}$  = 10  $\mu F$  Ceramic

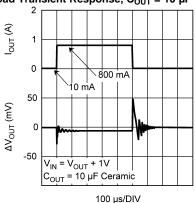


Figure 21.

# Load Transient Response, C<sub>OUT</sub> = 47 µF Ceramic

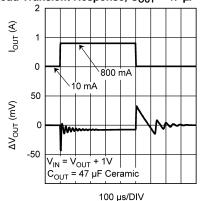


Figure 23.

# Load Transient Response, C<sub>OUT</sub> = 68 μF Tantalum

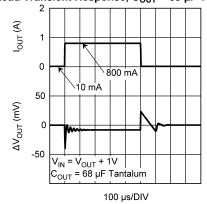
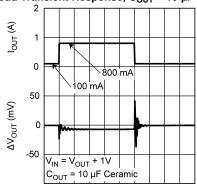


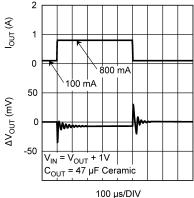
Figure 25.

## Load Transient Response, $C_{OUT} = 10 \mu F$ Ceramic



100 μs/DIV Figure 22.

## Load Transient Response, C<sub>OUT</sub> = 47 μF Ceramic



Load Transient Response, C<sub>OUT</sub> = 68 μF Tantalum

Figure 24.

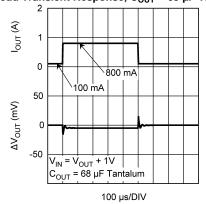


Figure 26.

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Refer to the TYPICAL APPLICATION CIRCUIT. Unless otherwise specified:  $T_J$  = 25°C, R1 = 1.40 k $\Omega$ , R2 = 1.00 k $\Omega$ ,

 $C_{FF}\text{= }180\text{ pF},\text{ }V_{\text{IN}}\text{= }V_{\text{OUT(NOM)}}\text{+ }1\text{V},\text{ }V_{\text{BIAS}}\text{= }3.0\text{V},\text{ }I_{\text{OUT}}\text{= }10\text{ mA},\text{ }C_{\text{IN}}\text{= }10\text{ }\mu\text{F}\text{ Ceramic},\text{ }C_{\text{OUT}}\text{= }10\text{ }\mu\text{F}\text{ Ceramic},\text{ }I_{\text{OUT}}\text{= }10\text{ }\mu\text{F}\text{Ceramic},\text{ }I_{\text{OUT}}\text{= }10\text{ }\mu\text{F}\text{ Ceramic},\text{ }I_{\text{OUT}}\text{= }10\text{ }\mu\text{F}\text{ Ceramic},\text{ }I_{\text{OUT}}\text{= }10\text{ }\mu\text{F}\text{Cer$ 

 $C_{\text{BIAS}}$  = 1  $\mu\text{F}$  Ceramic, ,  $C_{\text{SS}}$  = Open.  $V_{\text{BIAS}}$  PSRR

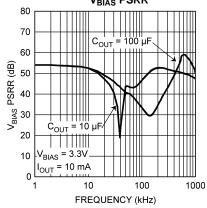


Figure 27.

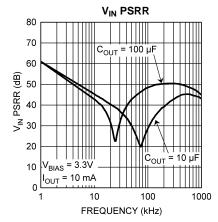
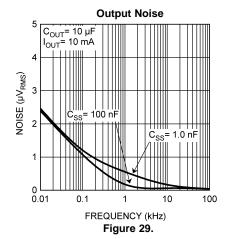
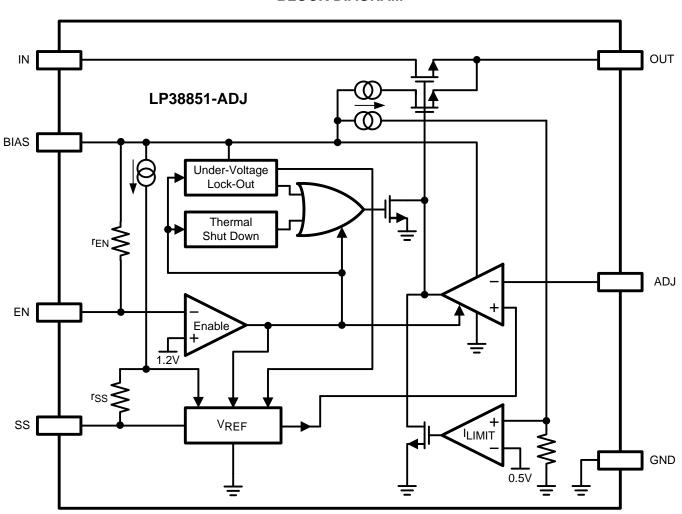


Figure 28.





# **BLOCK DIAGRAM**





#### **APPLICATION INFORMATION**

## **EXTERNAL CAPACITORS**

To assure regulator stability, input and output capacitors are required as shown in TYPICAL APPLICATION CIRCUIT.

#### **Output Capacitor**

A minimum output capacitance of 10  $\mu$ F, ceramic, is required for stability. The amount of output capacitance can be increased without limit. The output capacitor must be located less than 1 cm from the output pin of the IC and returned to the device ground pin with a clean analog ground.

Only high quality ceramic types such as X5R or X7R should be used, as the Z5U and Y5F types do not provide sufficient capacitance over temperature.

Tantalum capacitors will also provide stable operation across the entire operating temperature range. However, the effects of ESR may provide variations in the output voltage during fast load transients. Using the minimum recommended 10 µF ceramic capacitor at the output will allow unlimited capacitance, Tantalum and/or Aluminum, to be added in parallel.

# **Input Capacitor**

The input capacitor must be at least 10  $\mu$ F, but can be increased without limit. It's purpose is to provide a low source impedance for the regulator input. A ceramic capacitor, X5R or X7R, is recommended.

Tantalum capacitors may also be used at the input pin. There is no specific ESR limitation on the input capacitor (the lower, the better).

Aluminum electrolytic capacitors can be used, but are not recommended as their ESR increases very quickly at cold temperatures. They are not recommended for any application where the ambient temperature falls below 0°C.

#### **Bias Capacitor**

The capacitor on the bias pin must be at least 1  $\mu$ F, and can be any good quality capacitor (ceramic is recommended).

# Feed Forward Capacitor, C<sub>FF</sub> (Refer to TYPICAL APPLICATION CIRCUIT)

When using a ceramic capacitor for  $C_{OUT}$ , the typical ESR value will be too small to provide any meaningful positive phase compensation,  $F_Z$ , to offset the internal negative phase shifts in the gain loop.

$$F_Z = 1 / (2 \times \pi \times C_{OUT} \times ESR)$$
 (1)

A capacitor placed across the gain resistor R1 will provide additional phase margin to improve load transient response of the device. This capacitor,  $C_{FF}$ , in parallel with R1, will form a zero in the loop response given by the formula:

$$F_Z = 1 / (2 \times \pi \times C_{FF} \times R1)$$
 (2)

For optimum load transient response select C<sub>FF</sub> so the zero frequency, F<sub>Z</sub>, falls between 500 kHz and 750 kHz.

$$C_{FF} = 1 / (2 \times \pi \times R1 \times F_z)$$
 (3)

The phase lead provided by  $C_{FF}$  diminishes as the DC gain approaches unity, or  $V_{OUT}$  approaches  $V_{ADJ}$ . This is because  $C_{FF}$  also forms a pole with a frequency of:

$$F_{p} = 1 / (2 \times \pi \times C_{FF} \times (R1 || R2))$$
 (4)

It's important to note that at higher output voltages, where R1 is much larger than R2, the pole and zero are far apart in frequency. At lower output voltages the frequency of the pole and the zero mover closer together. The phase lead provided from  $C_{FF}$  diminishes quickly as the output voltage is reduced, and has no effect when  $V_{OUT} = V_{ADJ}$ . For this reason, relying on this compensation technique alone is adequate only for higher output voltages. For the LP38851, the practical minimum  $V_{OUT}$  is 0.8V when a ceramic capacitor is used for  $C_{OUT}$ .



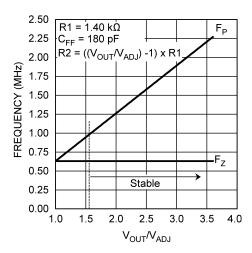


Figure 30.  $F_{ZERO}$  and  $F_{POLE}$  vs Gain

# SETTING THE OUTPUT VOLTAGE (Refer to TYPICAL APPLICATION CIRCUIT)

The output voltage is set using the external resistive divider R1 and R2. The output voltage is given by the formula:

$$V_{OUT} = V_{ADJ} \times \left(1 + \left(\frac{R1}{R2}\right)\right)$$
 (5)

The resistors used for R1 and R2 should be high quality, tight tolerance, and with matching temperature coefficients. It is important to remember that, although the value of  $V_{ADJ}$  is specified, the use of low quality resistors for R1 and R2 can easily produce a  $V_{OUT}$  value that is unacceptable.

It is recommended that the values selected for R1 and R2 are such that the parallel value is less than 10 k $\Omega$ . This is to prevent internal parasitic capacitances on the ADJ pin from interfering with the F<sub>Z</sub> pole set by R1 and C<sub>FF</sub>.

$$((R1 \times R2) / (R1 + R2)) \le 10 k\Omega$$
 (6)

Table 1 lists some suggested, best fit, standard  $\pm 1\%$  resistor values for R1 and R2, and a standard  $\pm 10\%$  capacitor values for C<sub>FF</sub>, for a range of V<sub>OUT</sub> values. Other values of R1, R2, and C<sub>FF</sub> are available that will give similar results.

Table 1.

$V_{OUT}$	R1	R2	C <sub>FF</sub>	F <sub>Z</sub>
0.8V	1.07 kΩ	1.78 kΩ	220 pF	676 kHz
0.9V	1.50 kΩ	1.87 kΩ	180 pF	589 kHz
1.00V	1.00 kΩ	1.00 kΩ	270 pF	589 kHz
1.1V	1.65 kΩ	1.37 kΩ	150 pF	643 kHz
1.2V	1.40 kΩ	1.00 kΩ	180 pF	631 kHz
1.3V	1.15 kΩ	715 Ω	220 pF	629 kHz
1.4V	1.07 kΩ	590 Ω	220 pF	676 kHz
1.5V	2.00 kΩ	1.00 kΩ	120pF	663 kHz
1.6V	1.65 kΩ	750 Ω	150 pF	643 kHz
1.7V	2.55 kΩ	1.07 kΩ	100 pF	624 kHz
1.8V	2.94 kΩ	1.13 kΩ	82 pF	660 kHz



Please refer to Application Note AN-1378 (SNVA112) for additional information on how resistor tolerances affect the calculated  $V_{OUT}$  value.

#### INPUT VOLTAGE

The input voltage ( $V_{IN}$ ) is the high current external voltage rail that will be regulated down to a lower voltage, which is applied to the load. The input voltage must be at least  $V_{OUT} + V_{DO}$ , and no higher than whatever value is used for  $V_{BIAS}$ .

For applications where  $V_{BIAS}$  is higher than 4.5V,  $V_{IN}$  must be no greater than 4.5V, otherwise output voltage accuracy may be affected.

## **BIAS VOLTAGE**

The bias voltage ( $V_{BIAS}$ ) is a low current external voltage rail required to bias the control circuitry and provide gate drive for the N-FET pass transistor. When  $V_{OUT}$  is set to 1.20V, or less,  $V_{BIAS}$  may be anywhere in the operating range of 3.0V to 5.5V. If  $V_{OUT}$  is set higher than 1.20V ,  $V_{BIAS}$  must be between 4.5V and 5.5V to ensure proper operation of the device.

## UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the device from functioning when the bias voltage is below the Under-Voltage Lock-Out (UVLO) threshold of approximately 2.45V.

As the bias voltage rises above the UVLO threshold the device control circuitry becomes active. There is approximately 150 mV of hysteresis built into the UVLO threshold to provide noise immunity.

When the bias voltage is between the UVLO threshold and the Minimum Operating Rating value of 3.0V the device will be functional, but the operating parameters will not be within the specified limits.

#### SUPPLY SEQUENCING

There is no requirement for the order that V<sub>IN</sub> or V<sub>BIAS</sub> are applied or removed.

One practical limitation is that the Soft-Start circuit starts charging  $C_{SS}$  when both  $V_{BIAS}$  rises above the UVLO threshold and the Enable pin is above the  $V_{EN(ON)}$  threshold. If the application of  $V_{IN}$  is delayed beyond this point the benefits of Soft-Start will be compromised.

In any case, the output voltage cannot be specified until both  $V_{IN}$  and  $V_{BIAS}$  are within the range of specified operating values.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommended for this diode clamp.

## **REVERSE VOLTAGE**

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when  $V_{IN}$  is abruptly taken low and  $C_{OUT}$  continues to hold a sufficient charge such that the input to output voltage becomes reversed.

The NMOS pass element, by design, contains no body diode. This means that, as long as the gate of the pass element is not driven, there will not be any reverse current flow through the pass element during a reverse voltage event. The gate of the pass element is not driven when  $V_{BIAS}$  is below the UVLO threshold, or when the Enable pin is held low.

When  $V_{BIAS}$  is above the UVLO threshold, and the Enable pin is above the  $V_{EN(ON)}$  threshold, the control circuitry is active and will attempt to regulate the output voltage. Since the input voltage is less than the output voltage the control circuit will drive the gate of the pass element to the full  $V_{BIAS}$  potential when the output voltage begins to fall. In this condition, reverse current will flow from the output pin to the input pin , limited only by the  $R_{DS(ON)}$  of the pass element and the output to input voltage differential. Discharging an output capacitor up 1000  $\mu F$  in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided.



#### **SOFT-START**

The LP38851 incorporates a Soft-Start function that reduces the start-up current surge into the output capacitor  $(C_{OUT})$  by allowing  $V_{OUT}$  to rise slowly to the final value. This is accomplished by controlling  $V_{REF}$  at the SS pin. The soft-start timing capacitor  $(C_{SS})$  is internally held to ground until both  $V_{BIAS}$  rises above the Under-Voltage Lock-Out threshold (ULVO) and the Enable pin is higher than the  $V_{EN(ON)}$  threshold.

 $V_{REF}$  will rise at an RC rate defined by the internal resistance of the SS pin ( $r_{SS}$ ), and the external capacitor connected to the SS pin. This allows the output voltage to rise in a controlled manner until steady-state regulation is achieved. Typically, five time constants are recommended to assure that the output voltage is sufficiently close to the final steady-state value. During the soft-start time the output current can rise to the built-in current limit.

Soft-Start Time = 
$$C_{SS} \times r_{SS} \times 5$$
 (7)

Since the  $V_{OUT}$  rise will be exponential, not linear, the in-rush current will peak during the first time constant ( $\tau$ ), and  $V_{OUT}$  will require four additional time constants ( $4\tau$ ) to reach the final value ( $5\tau$ ).

After achieving normal operation, should either  $V_{BIAS}$  fall below the ULVO threshold, or the Enable pin fall below the  $V_{EN(OFF)}$  threshold, the device output will be disabled and the Soft-Start capacitor ( $C_{SS}$ ) discharge circuit will become active. The  $C_{SS}$  discharge circuit will remain active until  $V_{BIAS}$  falls to 500 mV (typical). When  $V_{BIAS}$  falls below 500 mV (typical), the  $C_{SS}$  discharge circuit will cease to function due to a lack of sufficient biasing to the control circuitry.

Since  $V_{REF}$  appears on the SS pin, any leakage through  $C_{SS}$  will cause  $V_{REF}$  to fall, and thus affect  $V_{OUT}$ . A leakage of 50 nA (about 10 M $\Omega$ ) through  $C_{SS}$  will cause  $V_{OUT}$  to be approximately 0.1% lower than nominal, while a leakage of 500 nA (about 1 M $\Omega$ ) will cause  $V_{OUT}$  to be approximately 1% lower than nominal. Typical ceramic capacitors will have a factor of 10X difference in leakage between 25°C and 85°C, so the maximum ambient temperature must be included in the capacitor selection process.

Typical  $C_{SS}$  values will be in the range of 1 nF to 100 nF, providing typical Soft-Start times in the range of 70  $\mu$ s to 7 ms (5 $\tau$ ). Values less than 1 nF can be used, but the Soft-Start effect will be minimal. Values larger than 100 nF will provide soft-start, but may not be fully discharged if  $V_{BIAS}$  falls from the UVLVO threshold to less than 500 mV in less than 100  $\mu$ s.

Figure 31 shows the relationship between the C<sub>OUT</sub> value and a typical C<sub>SS</sub> value.

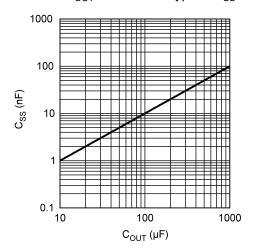


Figure 31. Typical C<sub>SS</sub> vs C<sub>OUT</sub> Values

The  $C_{SS}$  capacitor must be connected to a clean ground path back to the device ground pin. No components, other than  $C_{SS}$ , should be connected to the SS pin, as there could be adverse effects to  $V_{OUT}$ .

If the Soft-Start function is not needed the SS pin should be left open, although some minimal capacitance value is always recommended.



#### **ENABLE OPERATION**

The Enable pin (EN) provides a mechanism to enable, or disable, the regulator output stage. The Enable pin has an internal pull-up, through a typical 160 k $\Omega$  resistor, to  $V_{BIAS}$ .

If the Enable pin is actively driven, pulling the Enable pin above the V<sub>EN</sub> threshold of 1.25V (typical) will turn the regulator output on, while pulling the Enable pin below the V<sub>EN</sub> threshold will turn the regulator output off. There is approximately 100 mV of hysteresis built into the Enable threshold provide noise immunity.

If the Enable function is not needed this pin should be left open, or connected directly to V<sub>BIAS</sub>. If the Enable pin is left open, stray capacitance on this pin must be minimized, otherwise the output turn-on will be delayed while the stray capacitance is charged through the internal resistance (r<sub>EN</sub>).

## POWER DISSIPATION AND HEAT-SINKING

Additional copper area for heat-sinking may be required depending on the maximum device dissipation (P<sub>D</sub>) and the maximum anticipated ambient temperature (T<sub>A</sub>) for the device. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

The total power dissipation of the device is the sum of three different points of dissipation in the device.

The first part is the power that is dissipated in the NMOS pass element, and can be determined with the formula:

$$P_{D(PASS)} = (V_{IN} - V_{OUT}) \times I_{OUT}$$
(8)

The second part is the power that is dissipated in the bias and control circuitry, and can be determined with the formula:

 $P_{D(BIAS)} = V_{BIAS} \times I_{GND(BIAS)}$ 

where

 $I_{GND(BIAS)}$  is the portion of the operating ground current of the device that is related to  $V_{BIAS}$ (9)

The third part is the power that is dissipated in portions of the output stage circuitry, and can be determined with the formula:

$$P_{D(IN)} = V_{IN} \times I_{GND(IN)}$$

where

$$I_{\text{GND(IN)}}$$
 is the portion of the operating ground current of the device that is related to  $V_{\text{IN}}$  (10)

The total power dissipation is then:

$$P_{D} = P_{D(PASS)} + P_{D(BIAS)} + P_{D(IN)}$$
 (11)

The maximum allowable junction temperature rise  $(\Delta T_i)$  depends on the maximum anticipated ambient temperature  $(T_A)$  for the application, and the maximum allowable operating junction temperature  $(T_{J(MAX)})$ .

$$\Delta_{J} = T_{J(MAX)} - T_{A(MAX)} \tag{12}$$

The maximum allowable value for junction to ambient Thermal Resistance,  $\theta_{JA}$ , can be calculated using the formula:

$$\theta_{JA} \le \frac{\Delta T_J}{P_D}$$
 (13)

# **Heat-Sinking The SFM Package**

The SFM package has a  $\theta_{JA}$  rating of 60°C/W and a  $\theta_{JC}$  rating of 3°C/W. These ratings are for the package only, no additional heat-sinking, and with no airflow. If the needed  $\theta_{JA}$ , as calculated above, is greater than or equal to 60°C/W then no additional heat-sinking is required since the package can safely dissipate the heat and not exceed the operating  $T_{J(MAX)}$ . If the needed  $\theta_{JA}$  is less than 60°C/W then additional heat-sinking is needed.

The thermal resistance of a SFM package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of  $\theta_{JA}$  will be same as shown in next section for PFM package.

The heat-sink to be used in the application should have a heat-sink to ambient thermal resistance,  $\theta_{HA}$ :

$$\theta_{\mathsf{HA}} \leq \theta_{\mathsf{JA}} - (\theta_{\mathsf{CH}} + \theta_{\mathsf{JC}})$$

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$$\theta \stackrel{\mathsf{H}}{\mathsf{A}} \leq \theta \stackrel{\mathsf{J}}{\mathsf{A}} - \left(\theta \stackrel{\mathsf{C}}{\mathsf{B}} + \theta \stackrel{\mathsf{J}}{\mathsf{C}}\right)$$

#### where

- θ<sub>JA</sub> is the required total thermal resistance from the junction to the ambient air, θ<sub>CH</sub> is the thermal resistance from the case to the surface of the heart-sink
- $\theta_{JC}$  is the thermal resistance from the junction to the surface of the case

(14)

For this equation,  $\theta_{JC}$  is about 3°C/W for a SFM package. The value for  $\theta_{CH}$  depends on method of attachment, insulator, etc.  $\theta_{CH}$  varies between 1.5°C/W to 2.5°C/W. Consult the heat-sink manufacturer datasheet for details and recommendations.

## **Heat-Sinking The PFM Package**

The PFM package has a  $\theta_{JA}$  rating of 60°C/W, and a  $\theta_{JC}$  rating of 3°C/W. These ratings are for the package only, no additional heat-sinking, and with no airflow.

The PFM package uses the copper plane on the PCB as a heat-sink. The tab of this package is soldered to the copper plane for heat sinking. Figure 32 shows a curve for the  $\theta_{JA}$  of PFM package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat-sinking.

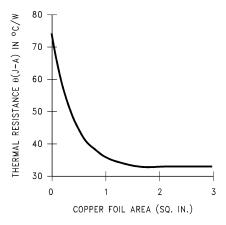


Figure 32.  $\theta_{JA}$  vs Copper (1 Ounce) Area for the PFM package

Figure 32 shows that increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for  $\theta_{JA}$  for the PFM package mounted to a PCB is 32°C/W.

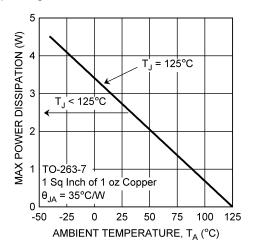


Figure 33. Maximum Power Dissipation vs Ambient Temperature for the PFM Package

Figure 33 shows the maximum allowable power dissipation for PFM packages for different ambient temperatures, assuming  $\theta_{JA}$  is 35°C/W and the maximum junction temperature is 125°C.



# Heat-Sinking The SO PowerPad Package

The LP38851MR package has a  $\theta_{JA}$  rating of 168°C/W, and a  $\theta_{JC}$  rating of 11°C/W. The  $\theta_{JA}$  rating of 168°C/W includes the device DAP soldered to an area of 0.008 square inches (0.09 in x 0.09 in) of 1 ounce copper, with no airflow.

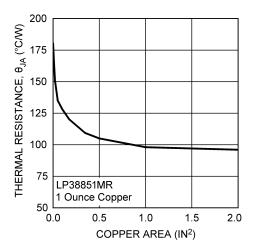


Figure 34.  $\theta_{JA}$  vs Copper (1 Ounce) Area for the SO PowerPad Package

Increasing the copper area soldered to the DAP to 1 square inch of 1 ounce copper, using a dog-bone type layout, will improve the  $\theta_{JA}$  rating to 98°C/W. Figure 34 shows that increasing the copper area beyond 1 square inch produces very little improvement.

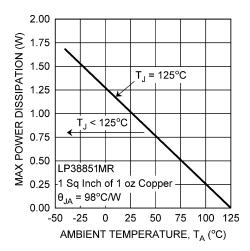


Figure 35. Maximum Power Dissipation vs Ambient Temperature for the SO PowerPad Package

Figure 35 shows the maximum allowable power dissipation for the SO PowerPad package for a range of ambient temperatures, assuming  $\theta_{JA}$  is 98°C/W and the maximum junction temperature is 125°C.



# **REVISION HISTORY**

Cł	hanges from Revision B (April 2013) to Revision C	Pag	ge
•	Changed layout of National Data Sheet to TI format		18

11-Nov-2025

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#### PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package   Pins	Package qty   Carrier	<b>RoHS</b> (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
LP38851MR-ADJ/NOPB	Active	Production	SO PowerPAD (DDA)   8	95   TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	L38851 MRADJ
LP38851MR-ADJ/NOPB.A	Active	Production	SO PowerPAD (DDA)   8	95   TUBE	Yes	SN	Level-3-260C-168 HR	-40 to 125	L38851 MRADJ
LP38851MRX-ADJ/NO.A	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L38851 MRADJ
LP38851MRX-ADJ/NOPB	Active	Production	SO PowerPAD (DDA)   8	2500   LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L38851 MRADJ
LP38851S-ADJ/NOPB	Active	Production	DDPAK/TO-263 (KTW)   7	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38851S -ADJ
LP38851S-ADJ/NOPB.A	Active	Production	DDPAK/TO-263 (KTW)   7	45   TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38851S -ADJ
LP38851SX-ADJ/NOPB	Active	Production	DDPAK/TO-263 (KTW)   7	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38851S -ADJ
LP38851SX-ADJ/NOPB.A	Active	Production	DDPAK/TO-263 (KTW)   7	500   LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38851S -ADJ
LP38851T-ADJ/NOPB	Active	Production	TO-220 (NDZ)   7	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP38851T -ADJ
LP38851T-ADJ/NOPB.A	Active	Production	TO-220 (NDZ)   7	45   TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP38851T -ADJ

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



# **PACKAGE OPTION ADDENDUM**

www.ti.com 11-Nov-2025

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

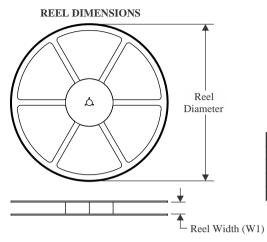
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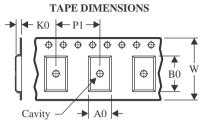
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# **PACKAGE MATERIALS INFORMATION**

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# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38851MRX-ADJ/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP38851SX-ADJ/NOPB	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

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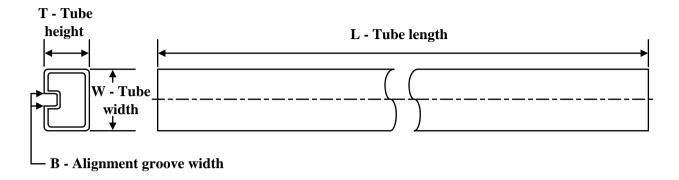
# \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38851MRX-ADJ/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	36.0
LP38851SX-ADJ/NOPB	DDPAK/TO-263	KTW	7	500	356.0	356.0	45.0

# **PACKAGE MATERIALS INFORMATION**

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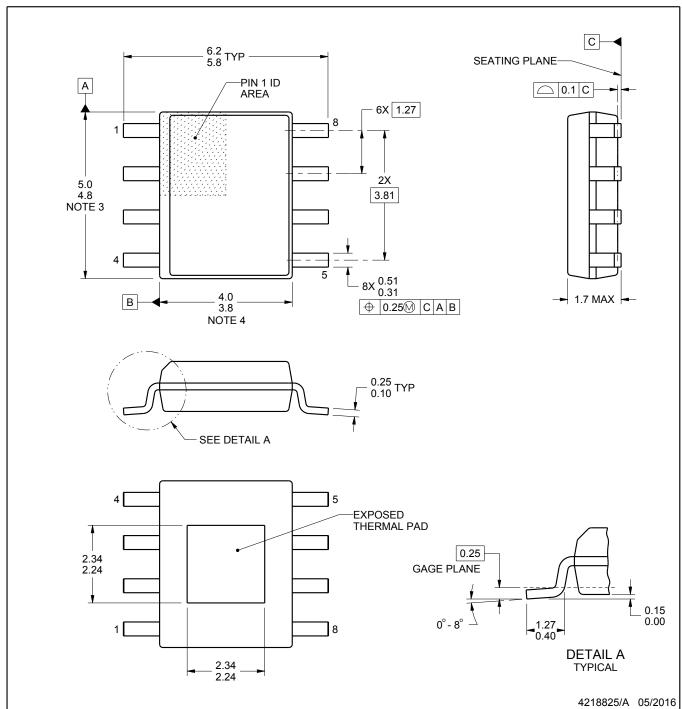
# **TUBE**



# \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP38851MR-ADJ/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05
LP38851MR-ADJ/NOPB.A	DDA	HSOIC	8	95	495	8	4064	3.05
LP38851S-ADJ/NOPB	KTW	TO-263	7	45	502	25	8204.2	9.19
LP38851S-ADJ/NOPB.A	KTW	TO-263	7	45	502	25	8204.2	9.19
LP38851T-ADJ/NOPB	NDZ	TO-220	7	45	502	30	30048.2	10.74
LP38851T-ADJ/NOPB.A	NDZ	TO-220	7	45	502	30	30048.2	10.74



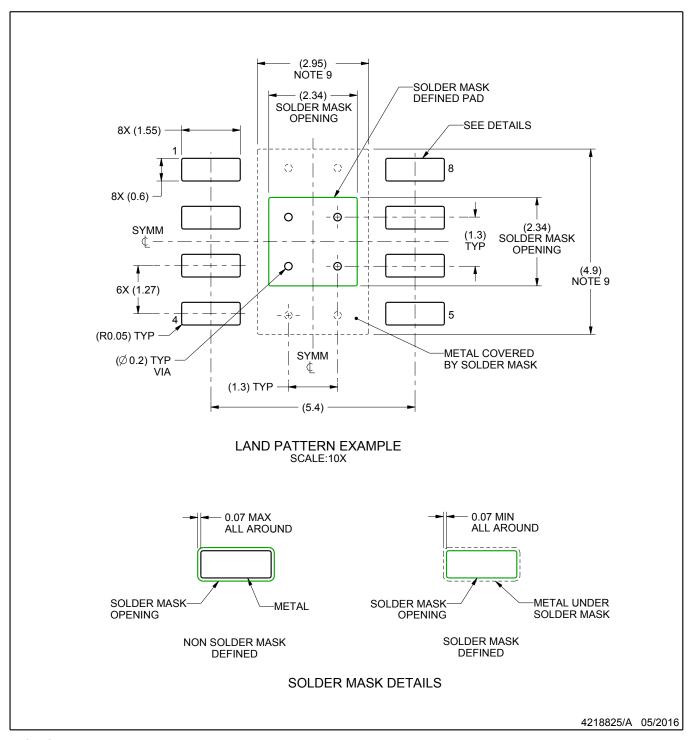


PowerPAD is a trademark of Texas Instruments.

# NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MS-012.

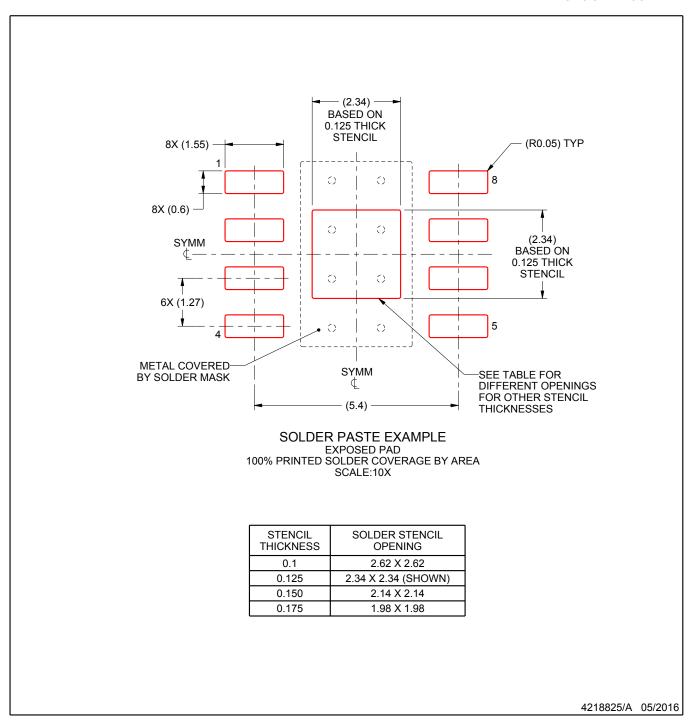




# NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
- Size of metal pad may vary due to creepage requirement.
   Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



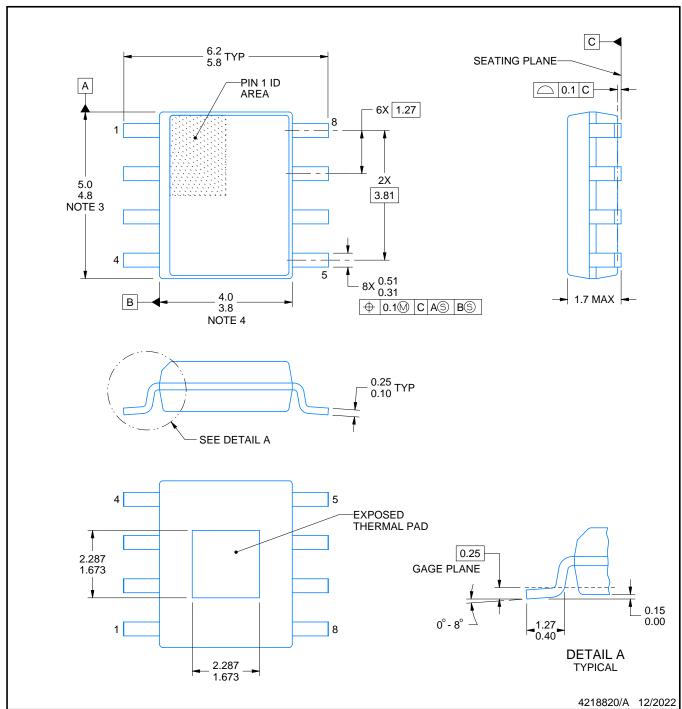


#### NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.





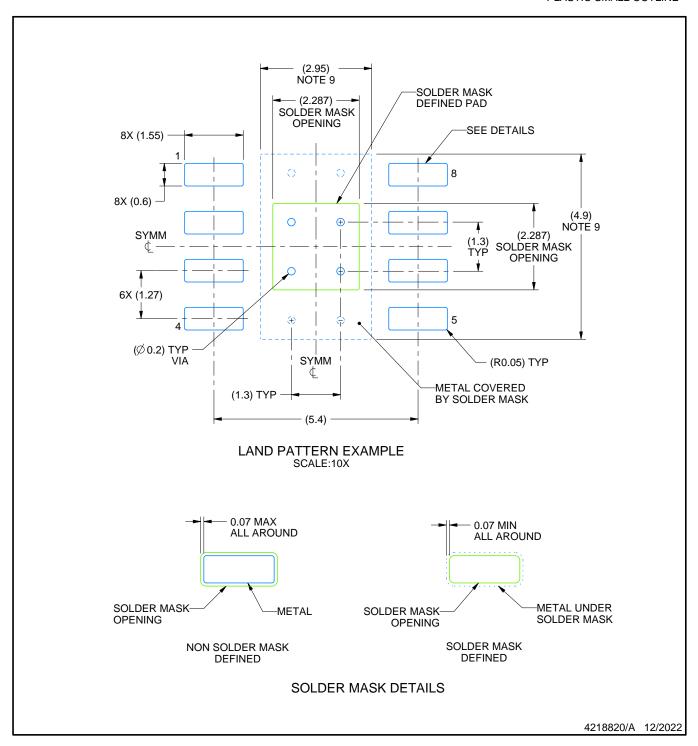


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# NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MS-012, variation BA.

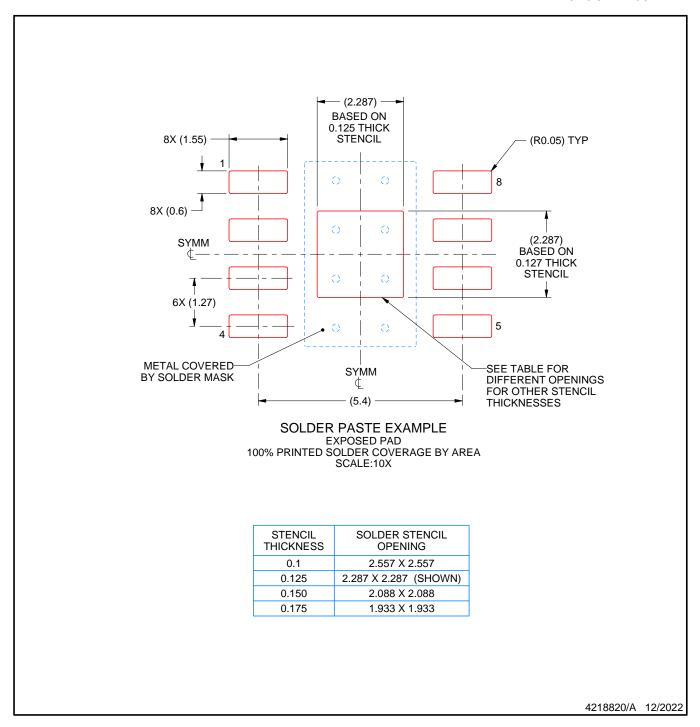




## NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
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- 9. Size of metal pad may vary due to creepage requirement.

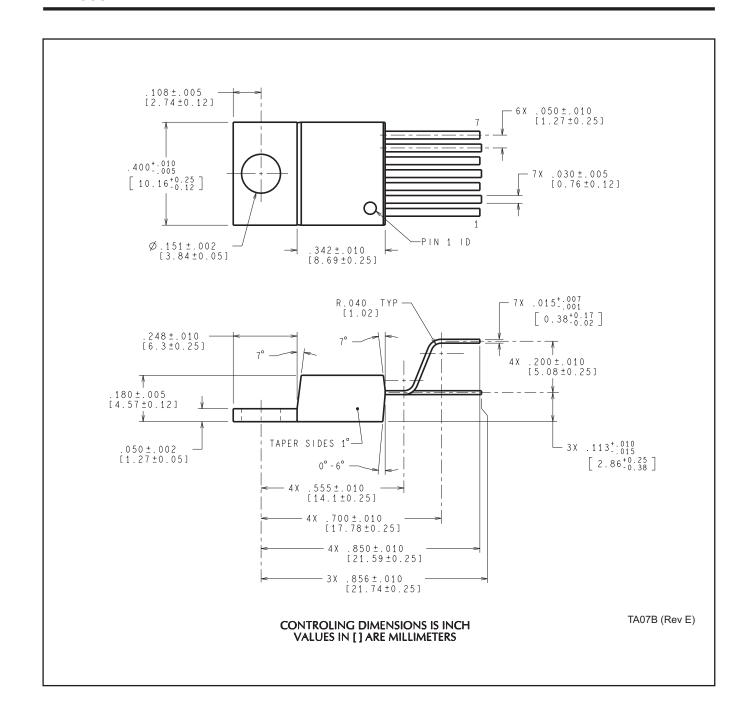




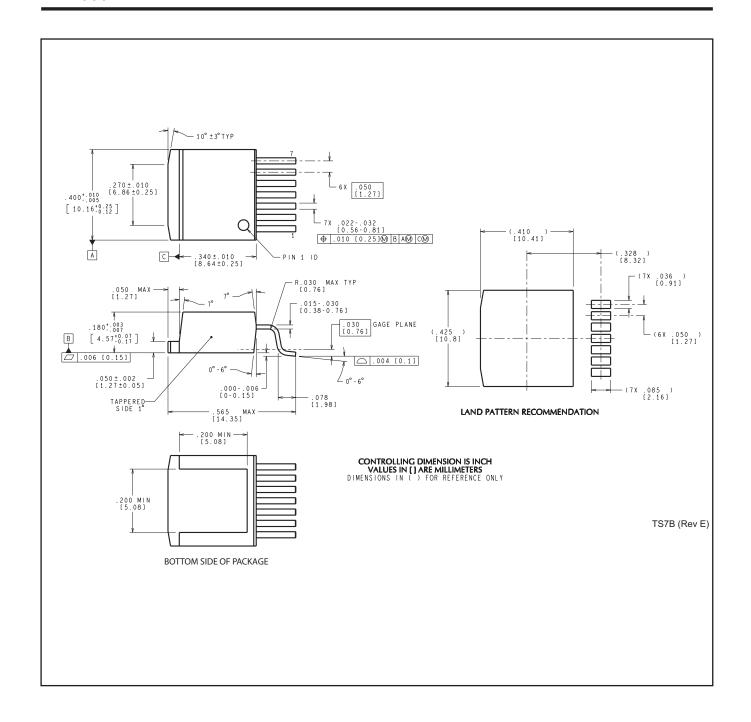
NOTES: (continued)

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- 11. Board assembly site may have different recommendations for stencil design.









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