LM3444 AC-DC Offline LED Driver

1 Features
- Application Voltage Range: 80 V\(_{\text{AC}}\) to 277 V\(_{\text{AC}}\)
- Capable of Controlling LED Currents
- Greater than 1 A
- Adjustable Switching Frequency
- Low Quiescent Current
- Adaptive Programmable Off-Time Allows for Constant Ripple Current
- Thermal Shutdown
- No Flicker at 120 Hz
- Low-Profile 10-Pin VSSOP Package or 8-Lead SOIC Package
- Patented Drive Architecture

2 Applications
- Solid State Lighting
- Industrial and Commercial Lighting
- Residential Lighting

3 Description
The LM3444 is an adaptive constant off-time AC/DC buck (step-down) constant current controller that provides a constant current for illuminating high power LEDs. The high-frequency capable architecture allows the use of small external passive components. A passive PFC circuit ensures good power factor by drawing current directly from the line for most of the cycle, and provides a constant positive voltage to the buck regulator. Additional features include thermal shutdown, current limit and V\(_{\text{CC}}\) undervoltage lockout. The LM3444 is available in a low profile 10-pin VSSOP package or an 8-lead SOIC package.

Device Information\(^{(1)}\)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3444</td>
<td>VSSOP (10)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
<tr>
<td></td>
<td>SOIC (8)</td>
<td>3.91 mm × 4.90 mm</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency vs Line Voltage

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2013) to Revision D Page

- Added ESD Ratings table, Feature Description section, Device Functional Modes section, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................. 1

Changes from Revision B (May 2013) to Revision C Page

- Changed layout of National Data Sheet to TI format ................................................................................................................................. 23
## 5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>COFF</td>
<td>4</td>
<td>VSSOP</td>
</tr>
<tr>
<td>FILTER</td>
<td>5</td>
<td>SOIC</td>
</tr>
<tr>
<td>GATE</td>
<td>8</td>
<td>SOIC</td>
</tr>
<tr>
<td>GND</td>
<td>6</td>
<td>SOIC</td>
</tr>
<tr>
<td>ISNS</td>
<td>7</td>
<td>SOIC</td>
</tr>
<tr>
<td>NC</td>
<td>1, 2, 3, 10</td>
<td>VSSOP</td>
</tr>
<tr>
<td>VCC</td>
<td>9</td>
<td>SOIC</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1),(2)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC}) and GATE to GND</td>
<td>–0.3</td>
<td>14</td>
<td>V</td>
</tr>
<tr>
<td>ISNS to GND</td>
<td>–0.3</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>FILTER and COFF to GND</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>COFF input current</td>
<td>60</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Continuous power dissipation(^{(3)})</td>
<td>Internally limited</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_J) Junction temperature</td>
<td>150</td>
<td></td>
<td>(^{\circ})C</td>
</tr>
<tr>
<td>Maximum lead temperature (soldering)</td>
<td>260</td>
<td></td>
<td>(^{\circ})C</td>
</tr>
</tbody>
</table>

\(1\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(2\) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.

\(3\) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at \(T_J = 165^{\circ}\)C (typical) and disengages at \(T_J = 145^{\circ}\)C (typical).

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)}) Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±1250</td>
<td></td>
</tr>
</tbody>
</table>

\(1\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(2\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC})</td>
<td>8</td>
<td>13</td>
<td>V</td>
</tr>
<tr>
<td>(T_J) Junction temperature</td>
<td>–40</td>
<td>125</td>
<td>(^{\circ})C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>LM3444</th>
<th>DGS (VSSOP)</th>
<th>D (SOIC)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>10 PINS</td>
<td>8 PINS</td>
<td></td>
</tr>
<tr>
<td>(R_{JUA}) Junction-to-ambient thermal resistance</td>
<td>163.8</td>
<td>111.3</td>
<td>(^{\circ})C/W</td>
<td></td>
</tr>
<tr>
<td>(R_{JUC(top)}) Junction-to-case (top) thermal resistance</td>
<td>58.4</td>
<td>58.0</td>
<td>(^{\circ})C/W</td>
<td></td>
</tr>
<tr>
<td>(R_{JUB}) Junction-to-board thermal resistance</td>
<td>83.6</td>
<td>51.1</td>
<td>(^{\circ})C/W</td>
<td></td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>6.1</td>
<td>11.9</td>
<td>(^{\circ})C/W</td>
<td></td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>82.3</td>
<td>51.0</td>
<td>(^{\circ})C/W</td>
<td></td>
</tr>
</tbody>
</table>

\(1\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
6.5 Electrical Characteristics

All typical limits are for $T_J = 25^\circ C$ and all maximum and minimum limits apply over the full operating temperature range ($T_J = -40^\circ C$ to 125$^\circ C$). Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ C$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{CC} = 12$ V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$ SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{VCC}$ Operating supply current</td>
<td>1.58</td>
<td>2.25</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$-UVLO Rising threshold</td>
<td>7.4</td>
<td>7.7</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$-UVLO Falling threshold</td>
<td>6</td>
<td>6.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$-UVLO Hysteresis</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>COFF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{COFF}$ Time-out threshold</td>
<td>1.225</td>
<td>1.276</td>
<td>1.327</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$R_{COFF}$ Off timer sinking impedance</td>
<td>33</td>
<td>60</td>
<td>Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{COFF}$ Restart timer</td>
<td>180</td>
<td></td>
<td>μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CURRENT LIMIT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{ISNS}$ ISNS limit threshold</td>
<td>1.174</td>
<td>1.269</td>
<td>1.364</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{ISNS}$ Leading edge blanking time</td>
<td>125</td>
<td></td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{ISNS}$ Current limit reset delay</td>
<td>180</td>
<td></td>
<td>μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{ISNS}$ ISNS limit to GATE delay</td>
<td>ISNS = 0 to 1.75-V step</td>
<td>33</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CURRENT SENSE COMPARATOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{FILTER}$ FILTER open circuit voltage</td>
<td>720</td>
<td>750</td>
<td>780</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$R_{FILTER}$ FILTER impedance</td>
<td>1.12</td>
<td></td>
<td>MΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OS}$ Current sense comparator offset voltage</td>
<td>−4</td>
<td>0.1</td>
<td>4</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>GATE DRIVE OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DRVH}$ GATE high saturation</td>
<td>$I_{GATE} = 50$ mA</td>
<td>0.24</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{DRVL}$ GATE low saturation</td>
<td>$I_{GATE} = 100$ mA</td>
<td>0.22</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{DRV}$ Peak souce current</td>
<td>GATE = $V_{CC}$/2</td>
<td>−0.77</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>$I_{DRV}$ Peak sink current</td>
<td>GATE = $V_{CC}$/2</td>
<td>0.88</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DRV}$ Rise time</td>
<td>$C_{load} = 1$ nF</td>
<td>15</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$I_{DRV}$ Fall time</td>
<td>$C_{load} = 1$ nF</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>THERMAL SHUTDOWN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{SD}$ Thermal shutdown temperature</td>
<td>See (1)</td>
<td>165</td>
<td></td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_{SD}$ Thermal shutdown hysteresis</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A-MAX}$) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ C$), the maximum power dissipation of the device in the application ($P_{D-MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{thJA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{thJA} \times P_{D-MAX})$. 
6.6 Typical Characteristics

Figure 1. fSW vs Input Line Voltage

Figure 2. Efficiency vs Input Line Voltage

Figure 3. VCC UVLO vs Temperature

Figure 4. Minimum On-Time (tON) vs Temperature

Figure 5. Off Threshold (C11) vs Temperature

Figure 6. Normalized Variation in fSW Over VBUCK Voltage
Typical Characteristics (continued)

Figure 7. Leading Edge Blanking Variation Over Temperature
7 Detailed Description

7.1 Overview
The LM3444 device contains all the necessary circuitry to build a line-powered (mains powered) constant current LED driver.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Theory of Operation
For an image of the LM3444 along with basic external circuitry, see Figure 8.
7.3.2 Valley-Fill Circuit

$V_{BUCK}$ supplies the power which drives the LED string. Diode D3 allows $V_{BUCK}$ to remain high while $V+$ cycles on and off. $V_{BUCK}$ has a relatively small hold capacitor C10 which reduces the voltage ripple when the valley fill capacitors are being charged. However, the network of diodes and capacitors shown between D3 and C10 make up a valley-fill circuit. The valley-fill circuit can be configured with two or three stages. The most common configuration is two stages. Figure 9 illustrates a two- and three-stage valley-fill circuit.
Feature Description (continued)

Figure 9. Two and Three Stage Valley Fill Circuit

The valley-fill circuit allows the buck regulator to draw power throughout a larger portion of the AC line. This allows the capacitance needed at $V_{BUCK}$ to be lower than if there were no valley-fill circuit, and adds passive power factor correction (PFC) to the application.

7.3.3 Valley-Fill Operation

When the input line is high, power is derived directly through D3. The term *input line is high* is explained as follows. The valley-fill circuit charges capacitors C7 and C9 in series (Figure 10) when the input line is high.

Figure 10. Two Stage Valley-Fill Circuit When AC Line is High

The peak voltage of a two-stage valley-fill capacitor is given by Equation 1.

$$V_{VF,CAP} = \frac{V_{AC-RMS} \sqrt{2}}{2}$$

As the AC line decreases from its peak value every cycle, there is a point where the voltage magnitude of the AC line is equal to the voltage that each capacitor is charged. At this point, diode D3 becomes reversed biased, and the capacitors are placed in parallel to each other (Figure 11), and $V_{BUCK}$ equals the capacitor voltage.
Feature Description (continued)

A three stage valley-fill circuit performs exactly the same as two-stage valley-fill circuit, except now three capacitors are charged in series when the line voltage decreases, as shown in Equation 2:

\[ V_{VF\text{-}CAP} = \frac{V_{AC\text{-}RMS} \sqrt{2}}{3} \]  

Figure 11. Two Stage Valley-Fill Circuit when AC Line is Low

Diode D3 is reverse-biased and three capacitors are in parallel to each other.

The valley-fill circuit can be optimized for power factor, voltage hold-up, and overall application size and cost. The LM3444 operates with a single-stage or a three-stage valley-fill circuit as well. Resistor R8 functions as a current limiting resistor during start-up, and during the transition from series to parallel connection. Resistors R6 and R7 are 1-MΩ bleeder resistors, and may or may not be necessary for each application.

7.3.4 Buck Converter

The LM3444 is a buck controller that uses a proprietary constant off-time method to maintain constant current through a string of LEDs. While transistor Q2 is on, current ramps up through the inductor and LED string. A resistor R3 senses this current and this voltage is compared to the reference voltage at FILTER. When this sensed voltage is equal to the reference voltage, transistor Q2 is turned off and diode D10 conducts the current through the inductor and LEDs. Capacitor C12 eliminates most of the ripple current seen in the inductor. Resistor R4, capacitor C11, and transistor Q3 provide a linear current ramp that sets the constant off-time for a given output voltage.
7.3.5 Overview Of Constant Off-Time Control

The conversion ratio of a buck converter is defined as given by Equation 3.

\[
\frac{V_O}{V_{IN}} = D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times f_{SW}
\]  

(3)

Constant off-time control architecture operates by simply defining the off-time and allowing the on-time, and therefore the switching frequency, to vary as either \(V_{IN}\) or \(V_O\) changes. The output voltage is equal to the LED string voltage \(V_{LED}\), and should not change significantly for a given application. The input voltage or \(V_{BUCK}\) in this analysis varies as the input line varies. The length of the on-time is determined by the sensed inductor current through a resistor to a voltage reference at a comparator. During the on-time, denoted by \(t_{ON}\), MOSFET switch Q2 is on causing the inductor current to increase. During the on-time, current flows from \(V_{BUCK}\), through the LEDs, through L2, Q2, and finally through R3 to ground. At some point in time, the inductor current reaches a maximum \(I_{L2-PK}\) determined by the voltage sensed at R3 and the ISNS pin. This sensed voltage across R3 is compared against the voltage of FILTER, at which point Q2 is turned off by the controller.
Feature Description (continued)

During the off-period denoted by $t_{OFF}$, the current through L2 continues to flow through the LEDs through D10.

7.3.6 Thermal Shutdown
Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch does not turn on until the junction temperature drops to approximately 145°C.

7.4 Device Functional Modes
This device does not have any additional functional modes.

![Figure 13. Inductor Current Waveform in CCM](image-url)
8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Determining Duty-Cycle (D)

Equation 4 shows the duty-cycle (D).

\[
\frac{V_{\text{LED}}}{V_{\text{BUCK}}} = D = \frac{t_{\text{ON}}}{t_{\text{ON}} + t_{\text{OFF}}} = t_{\text{ON}} x f_{\text{SW}}
\]  

(4)

Equation 5 shows the duty-cycle with efficiency considered.

\[
\frac{1}{\eta} \times \frac{V_{\text{LED}}}{V_{\text{BUCK}}} = D
\]

(5)

For simplicity, choose efficiency from 75% to 85%.

8.1.2 Calculating Off-Time

The off-time of the LM3444 is set by the user and remains fairly constant as long as the voltage of the LED stack remains constant. Calculating the off-time is the first step in determining the switching frequency of the converter, which is integral in determining some external component values.

PNP transistor Q3, resistor R4, and the LED string voltage define a charging current into capacitor C11. A constant current into a capacitor creates a linear charging characteristic.

\[
i = C \frac{dv}{dt}
\]

(6)

Resistor R4, capacitor C11 and the current through resistor R4 (i_{COLL}), which is approximately equal to \(V_{\text{LED}}/R4\), are all fixed. Therefore, \(dv\) is fixed and linear, and \(dt\) (t_{OFF}) can now be calculated as shown in Equation 7.

\[
t_{\text{OFF}} = C11 \times 1.276V \times \left(\frac{R4}{V_{\text{LED}}}\right)
\]

(7)

Common equations for determining duty-cycle and switching frequency in any buck converter are shown in Equation 8.

\[
f_{\text{SW}} = \frac{1}{t_{\text{OFF}} + t_{\text{ON}}}
\]

\[
D = \frac{t_{\text{ON}}}{t_{\text{ON}} + t_{\text{OFF}}} = \frac{V_{\text{LED}}}{V_{\text{BUCK}}}
\]

\[
D' = \frac{t_{\text{OFF}}}{t_{\text{ON}} + t_{\text{OFF}}}
\]

(8)

Therefore, Equation 9 shows:

\[
f_{\text{SW}} = \frac{D}{t_{\text{ON}}}, \text{ and } f_{\text{SW}} = \frac{1 - D}{t_{\text{OFF}}}
\]

(9)
Application Information (continued)

With efficiency of the buck converter in mind, Equation 10 shows:

\[
\frac{V_{LED}}{V_{BUCK}} = \eta \times D
\]  \hspace{1cm} (10)

Substituting and rearranging the equations, Equation 11 shows:

\[
f_{SW} = \frac{1 - \frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}}}{t_{OFF}}
\]  \hspace{1cm} (11)

Off-time and switching frequency can now be calculated using the previous equations.

8.1.3 Setting the Switching Frequency

Selecting the switching frequency for nominal operating conditions is based on tradeoffs between efficiency (better at low frequency) and solution size and cost (smaller at high frequency).

The input voltage to the buck converter \(V_{BUCK}\) changes with both line variations and over the course of each half-cycle of the input line voltage. The voltage across the LED string, however, remains constant, and therefore the off-time remains constant.

The on-time, and therefore the switching frequency, varies as the \(V_{BUCK}\) voltage changes with line voltage. A good design practice is to choose a desired nominal switching frequency knowing that the switching frequency decreases as the line voltage drops, and increases as the line voltage increases (Figure 14).

![Graphical Illustration of Switching Frequency vs V_{BUCK}](image)

**Figure 14.** Graphical Illustration of Switching Frequency vs \(V_{BUCK}\)

The off-time of the LM3444 can be programmed for switching frequencies ranging from 30 kHz to over 1 MHz. A trade-off between efficiency and solution size must be considered when designing the LM3444 application.

The maximum switching frequency attainable is limited only by the minimum on-time requirement (200 ns).

Worst case scenario for minimum on time is when \(V_{BUCK}\) is at its maximum voltage (AC high line) and the LED string voltage \(V_{LED}\) is at its minimum value, as shown in Equation 12.

\[
t_{ON(MIN)} = \left( \frac{1}{\eta} \times \frac{V_{LED(MIN)}}{V_{BUCK(MAX)}} \right) \times \frac{1}{f_{SW}}
\]  \hspace{1cm} (12)
Application Information (continued)

The maximum voltage seen by the Buck Converter is given by Equation 13.

\[ V_{\text{BUCK(MAX)}} = V_{\text{AC-RMS(MAX)}} \times \sqrt{2} \]  

(13)

8.1.4 Inductor Selection

The controlled off-time architecture of the LM3444 regulates the average current through the inductor (L2), and therefore the LED string current. The input voltage to the buck converter \( V_{\text{BUCK}} \) changes with line variations and over the course of each half-cycle of the input line voltage. The voltage across the LED string is relatively constant, and therefore the current through R4 is constant. This current sets the off-time of the converter and therefore the output volt-second product \( (V_{\text{LED}} \times \text{off-time}) \) remains constant. A constant volt-second product makes it possible to keep the ripple through the inductor constant as the voltage at \( V_{\text{BUCK}} \) varies.

![Figure 15. LM3444 External Components of the Buck Converter](image)

Use Equation 14 to calculate an ideal inductor.

\[ v = L \frac{di}{dt} \]  

(14)

Given a fixed inductor value, \( L \), Equation 14 states that the change in the inductor current over time is proportional to the voltage applied across the inductor.

During the on-time, the voltage applied across the inductor is given in Equation 15.

\[ V_{\text{L(ON-TIME)}} = V_{\text{BUCK}} - (V_{\text{LED}} + V_{\text{DS(Q2)}} + I_{L2} \times R3) \]  

(15)

Because the voltage across the MOSFET switch (Q2) is relatively small, as is the voltage across sense resistor R3, we can approximately simplify this as shown in Equation 16,

\[ V_{\text{L(ON-TIME)}} = V_{\text{BUCK}} - V_{\text{LED}} \]  

(16)

During the off-time, the voltage seen by the inductor is given by Equation 17.

\[ V_{\text{L(OFF-TIME)}} = V_{\text{LED}} \]  

(17)
Application Information (continued)

The value of $V_{L\text{(OFF-TIME)}}$ is relatively constant, because the LED stack voltage remains constant. If we rewrite the equation for an inductor inserting what we know about the circuit during the off-time, Equation 18 shows that we get:

$$V_{L\text{(OFF-TIME)}} = V_{\text{LED}} = L \times \frac{\Delta i}{\Delta t}$$

$$V_{L\text{(OFF-TIME)}} = V_{\text{LED}} = L \times \frac{(I_{\text{MAX}}) - (I_{\text{MIN}})}{\Delta t}$$

Rearranging this gives Equation 19.

$$\Delta i \approx t_{\text{OFF}} \times \frac{V_{\text{LED}}}{L2}$$

From this, we can see that the ripple current ($\Delta i$) is proportional to off-time ($t_{\text{OFF}}$) multiplied by a voltage, which is dominated by $V_{\text{LED}}$ divided by a constant ($L2$).

These equations can be rearranged to calculate the desired value for inductor $L2$, as shown in Equation 20.

$$L2 \approx t_{\text{OFF}} \times \frac{V_{\text{LED}}}{\Delta i}$$

The off time can be calculated using Equation 21:

$$t_{\text{OFF}} = \left(1 - \frac{1}{\eta} \times \frac{V_{\text{LED}}}{V_{\text{BUCK}}}\right)$$

Substituting $t_{\text{off}}$ in Equation 21 results in Equation 22:

$$L2 = \frac{V_{\text{LED}} \left(1 - \frac{1}{\eta} \times \frac{V_{\text{LED}}}{V_{\text{BUCK}}}\right)}{f_{\text{SW}} \times \Delta i}$$

See Typical Application to better understand the design process.

8.1.5 Setting the LED Current

The LM3444 constant off-time control loop regulates the peak inductor current ($I_{L2}$). The average inductor current equals the average LED current ($I_{\text{AVE}}$). Therefore the average LED current is regulated by regulating the peak inductor current.

![Figure 16. Inductor Current Waveform in CCM](image-url)
Application Information (continued)

Knowing the desired average LED current, \(I_{\text{AVE}}\), and the nominal inductor current ripple, \(\Delta i_L\), the peak current for an application running in continuous conduction mode (CCM) is defined in Equation 23.

\[
I_{L2-PK} = I_{\text{AVE}} + \frac{\Delta i_L}{2}
\]  

(23)

The LED current would then be calculated using Equation 24.

\[
I_{\text{AVE(UNDIM)}} = I_{L2-PK(UNDIM)} - \frac{\Delta i_L}{2}
\]  

(24)

This is important to calculate because this peak current multiplied by the sense resistor R3 determines when the internal comparator is tripped. The internal comparator turns the control MOSFET off once the peak sensed voltage reaches 750 mV.

\[
I_{L-PK(UNDIM)} = \frac{750 \text{ mV}}{R3}
\]  

(25)

**Current Limit**: The trip voltage on the PWM comparator is 750 mV. However, if there is a short circuit or an excessive load on the output, higher than normal switch currents cause a voltage greater than 1.27 V on the ISNS pin which trip the I-LIM comparator. The I-LIM comparator resets the RS latch, turning off Q2. It also inhibits the Start Pulse Generator and the COFF comparator by holding the COFF pin low. A delay circuit prevents the start of another cycle for 180 \(\mu\)s.

### 8.1.6 Valley Fill Capacitors

Determining voltage rating and capacitance value of the valley-fill capacitors:

The maximum voltage seen by the valley-fill capacitors is calculated by Equation 26.

\[
V_{\text{VF-CAP}} = \frac{V_{\text{AC(MAX)}} \sqrt{2}}{\#\text{stages}}
\]  

(26)

This is, of course, if the capacitors chosen have identical capacitance values and split the line voltage equally. Often a 20% difference in capacitance could be observed between like capacitors. Therefore a voltage rating margin of 25% to 50% should be considered.

### 8.1.7 Determining the Capacitance Value of the Valley-Fill Capacitors

The valley-fill capacitors must be sized to supply energy to the buck converter \(V_{\text{BUCK}}\) when the input line is less than its peak divided by the number of stages used in the valley fill \(t_X\). The capacitance value must be calculated for the maximum LED current.

![Figure 17. Two Stage Valley-Fill \(V_{\text{BUCK}}\) Voltage](image-url)
Application Information (continued)

From Figure 17 and the equation for current in a capacitor, \( i = C \times \frac{dV}{dt} \), the amount of capacitance needed at \( V_{\text{BUCK}} \) is calculated as follows.

At 60 Hz, and a valley-fill circuit of two stages, the hold-up time \( (t_X) \) required at \( V_{\text{BUCK}} \) is calculated as follows. The total angle of an AC half cycle is 180° and the total time of a half AC line cycle is 8.33 ms. When the angle of the AC waveform is at 30° and 150°, the voltage of the AC line is exactly \( \frac{1}{2} \) of its peak. With a two-stage valley-fill circuit, this is the point where the LED string switches from power being derived from AC line to power being derived from the hold up capacitors (C7 and C9). 60° out of 180° of the cycle or 1/3 of the cycle the power is derived from the hold up capacitors \( (1/3 \times 8.33 \text{ ms} = 2.78 \text{ ms}) \). This is equal to the hold up time \( (dt) \) from the previous equation, and \( dv \) is the amount of voltage the circuit is allowed to droop. From Determining Maximum Number of Series Connected LEDs Allowed, we know the minimum \( V_{\text{BUCK}} \) voltage is about 45 V for a 90-V\(_{\text{AC}}\) to 135-V\(_{\text{AC}}\) line. At 90-V\(_{\text{AC}}\) low-line operating condition input, \( \frac{1}{2} \) of the peak voltage is 64 V. Thus, with some margin, the voltage at \( V_{\text{BUCK}} \) can not drop more than about 15 V \((dv)\). \( (i) \) is equal to \((P_{\text{OUT}}/V_{\text{BUCK}})\), where \( P_{\text{OUT}} \) is equal to \((V_{\text{LED}} \times I_{\text{LED}})\). Total capacitance \( (C7 \text{ in parallel with C9}) \) can now be calculated. See Typical Application for further calculations of the valley-fill capacitors.

8.1.8 Determining Maximum Number of Series Connected LEDs Allowed

The LM3444 is an off-line buck topology LED driver. A buck converter topology requires that the input voltage \( (V_{\text{BUCK}}) \) of the output circuit must be greater than the voltage of the LED stack \( (V_{\text{LED}}) \) for proper regulation. One must determine what the minimum voltage observed by the buck converter is before the maximum number of LEDs allowed can be determined. The following two variables must be determined to accomplish this:

1. AC line operating voltage. This is usually 90 V\(_{\text{AC}}\) to 135 V\(_{\text{AC}}\) for North America. Although the LM3444 can operate at much lower and higher input voltages, a range is needed to illustrate the design process.
2. The number of stages implemented in the valley-fill circuit (1, 2, or 3).

In this example, the most common valley-fill circuit is used (two stages).

Figure 18 shows the AC waveform. One can easily see that the peak voltage \( (V_{\text{PEAK}}) \) is always given by Equation 27.

\[
V_{\text{AC-RMS-PK}} \sqrt{2}
\]

The voltage at \( V_{\text{BUCK}} \) with a valley-fill stage of two looks similar to the waveforms in Figure 17.

The purpose of the valley-fill circuit is to allow the buck converter to pull power directly off of the AC line when the line voltage is greater than its peak voltage divided by two (two-stage valley-fill circuit). During this time, the capacitors within the valley fill circuit (C7 and C8) are charged up to the peak of the AC line voltage. Once the line drops below its peak divided by two, the two capacitors are placed in parallel and deliver power to the buck converter. One can now see that if the peak of the AC line voltage is lowered due to variations in the line voltage, the DC offset \( (V_{\text{DC}}) \) lowers. \( V_{\text{DC}} \) is the lowest value that voltage \( V_{\text{BUCK}} \) encounters.
Application Information (continued)

\[ V_{\text{BUCK(MIN)}} = \frac{V_{\text{AC-RMS(MIN)}}}{\sqrt{2}} \times \sin(\theta) \times \text{#stages} \]  

(28)

Example:

Line voltage = 90 V\text{AC} to 135 V\text{AC}

Valley-fill = two stage

\[ V_{\text{BUCK(MIN)}} = \frac{90 \times \sqrt{2} \times \sin(135^\circ)}{2} = 45\text{V} \]  

(29)

Depending on what type and value of capacitors are used, some derating should be used for voltage droop when the capacitors are delivering power to the buck converter. With this derating, the lowest voltage the buck converter sees is about 42.5 V in this example.

To determine how many LEDs can be driven, take the minimum voltage the buck converter sees (42.5 V) and divide it by the worst-case forward voltage drop of a single LED.

Example: 42.5 V / 3.7 V = 11.5 LEDs (11 LEDs with margin)

8.1.9 Output Capacitor

A capacitor placed in parallel with the LED or array of LEDs can be used to reduce the LED current ripple while keeping the same average current through both the inductor and the LED array. With a buck topology, the output inductance (L2) can now be lowered, making the magnets smaller and less expensive. With a well designed converter, you can assume that all of the ripple is seen by the capacitor, and not the LEDs. One must ensure that the capacitor you choose can handle the RMS current of the inductor. See the manufacturer data sheets to ensure compliance. Usually an X5R or X7R capacitor from 1 µF and 10 µF of the proper voltage rating is sufficient.

8.1.10 Switching MOSFET

The main switching MOSFET should be chosen with efficiency and robustness in mind. As shown in Equation 30, the maximum voltage across the switching MOSFET equals:

\[ V_{\text{DS(MAX)}} = V_{\text{AC-RMS(MAX)}} \times \sqrt{2} \]  

(30)

The average current rating should be greater than what is given in Equation 31.

\[ I_{\text{DS-MAX}} = I_{\text{LED(AVE)}}(D_{\text{MAX}}) \]  

(31)

8.1.11 Recirculating Diode

The LM3444 buck converter requires a recirculating diode D10 (see Figure 8) to carry the inductor current during the MOSFET Q2 off-time. The most efficient choice for D10 is a diode with a low forward drop and near-zero reverse recovery time that can withstand a reverse voltage of the maximum voltage seen at V\text{BUCK}. For a common 110 V\text{AC} ± 20% line, the reverse voltage could be as high as 190 V, as shown in Equation 32.

\[ V_{\text{D}} \geq V_{\text{AC-RMS(MAX)}} \times \sqrt{2} \]  

(32)

As shown in Equation 33, the current rating must be at least:

\[ I_{\text{D}} = (1 - D_{\text{MIN}}) \times I_{\text{LED(AVE)}} \]  

(33)

Or as shown in Equation 34:

\[ I_{\text{D}} = \left(1 - \frac{V_{\text{LED(MIN)}}}{V_{\text{BUCK(MAX)}}}\right) \times I_{\text{LED(AVE)}} \]  

(34)

8.2 Typical Application

The following design example illustrates the process of calculating external component values.
Typical Application (continued)

Figure 19. LM3444 Design Example 1 Input = 90 V\textsubscript{AC} to 135 V\textsubscript{AC}

\[ V_{LED} = 7 \times \text{HB LED String Application at 400 mA} \]
Typical Application (continued)

8.2.1 Design Requirements

Known:
1. Input voltage range (90 $V_{AC}$ to 135 $V_{AC}$)
2. Number of LEDs in series = 7
3. Forward voltage drop of a single LED = 3.6 V
4. LED stack voltage = ($7 \times 3.6$ V) = 25.2 V

Choose:
1. Nominal switching frequency, $f_{SW-TARGET}$ = 350 kHz
2. $I_{LED(AVE)}$ = 400 mA
3. $\Delta i$ (usually 15% to 30% of $I_{LED(AVE)}$) = ($0.30 \times 400$ mA) = 120 mA
4. Valley-fill stages (1, 2, or 3) = 2
5. Assumed minimum efficiency = 80%

8.2.2 Detailed Design Procedure

Calculate:
1. Calculate minimum voltage $V_{BUCK}$, as shown in Equation 35, which yields:

   \[
   V_{BUCK(MIN)} = \frac{90 \sqrt{2} \times \text{SIN}(135^\circ)}{2} = 45 \text{V} \tag{35}
   \]

2. Calculate maximum voltage $V_{BUCK}$, as shown in Equation 36, which yields:

   \[
   V_{BUCK(MAX)} = 135 \sqrt{2} = 190 \text{V} \tag{36}
   \]

3. Calculate $t_{OFF}$ at $V_{BUCK}$ nominal line voltage, as given by Equation 37.

   \[
   t_{OFF} = \frac{1 - \frac{1}{0.8} \times \frac{25.2V}{115 \sqrt{2}}}{(250 \text{kHz})} = 3.23 \mu\text{s} \tag{37}
   \]

4. Calculate $t_{ON(MIN)}$ at high line to ensure that $t_{ON(MIN)} > 200$ ns, as given by Equation 38.

   \[
   t_{ON(MIN)} = \left(1 - \frac{1}{0.8} \times \frac{25.2V}{135 \sqrt{2}}\right) \times 3.23 \mu\text{s} = 638 \text{ ns} \tag{38}
   \]

5. Calculate C11 and R4 in steps 6 through 9.
6. Choose current through R4 (from 50 µA to 100 µA): 70 µA as given by Equation 39.

   \[
   R4 = \frac{V_{LED}}{I_{COLL}} = 360 \text{k}\Omega \tag{39}
   \]

7. Use a standard value of 365 kΩ.
8. Calculate C11 as given by Equation 40.

   \[
   C11 = \left(\frac{V_{LED}}{R4}\right) \left(\frac{t_{OFF}}{1.276}\right) = 175 \text{pF} \tag{40}
   \]

9. Use standard value of 120 pF.
10. Calculate ripple current: 400 mA $\times$ 0.30 = 120 mA
11. Calculate inductor value at $t_{OFF} = 3 \mu\text{s}$ as given by Equation 41.
Typical Application (continued)

\[
L2 = \frac{25.2V \left(1 - \frac{1}{0.8} \times \frac{25.2V}{115\sqrt{2}}\right)}{(350 kHz \times 0.1A)} = 580 \mu F
\]

12. Choose C10: 1 \mu F, 200 V

13. Calculate valley-fill capacitor values:

\[ V_{AC \ low \ line} = 90 V_{AC}, \ V_{Buck \ minimum} = 60 V. \ Set \ droop \ for \ 20-V \ maximum \ at \ full \ load \ and \ low \ line \ as \ shown \ in \ Equation \ 42. \]

\[ i = C \frac{dv}{dt} \]

where

- \( i \) equals \( P_{OUT}/V_{Buck} \) (270 mA)
- \( dv \) equals 20 V
- \( dt \) equals 2.77 ms
- \( C_{TOTAL} \) equals 37 \mu F

Thus, \( C7 = C9 = 22 \mu F \)

8.2.3 Application Curve

![Efficiency vs Input Voltage](image)

**Figure 20. Efficiency vs Input Voltage**

<table>
<thead>
<tr>
<th>QTY</th>
<th>DESIGNATOR</th>
<th>DESCRIPTION</th>
<th>MANUFACTURER</th>
<th>MANUFACTURER PART NUMBER</th>
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<tr>
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<td>IC, CTRLR, DRVR-LED, VSSOP</td>
<td>TI</td>
<td>LM3444MM</td>
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<td>BR1</td>
<td>Bridge Rectifier, SMT, 400 V, 800 mA</td>
<td>DiodesInc</td>
<td>HD04-T</td>
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<td>1</td>
<td>L1</td>
<td>Common mode filter DIP4NS, 900 mA, 700 \mu H</td>
<td>Panasonic</td>
<td>ELF-11090E</td>
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<td>1</td>
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<td>Coilcraft</td>
<td>MSS1260-474-KLB</td>
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<td>2</td>
<td>L3, L4</td>
<td>Diff mode inductor, 500 mA, 1 mH</td>
<td>Coilcraft</td>
<td>MSS1260-105KL-KLB</td>
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<td>1</td>
<td>L5</td>
<td>Bead Inductor, 160 \Omega, 6 A</td>
<td>Steward</td>
<td>HI1206T161R-10</td>
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<tr>
<td>3</td>
<td>C1, C2, C15</td>
<td>Cap, Film, X2Y2, 12.5 MM, 250 V_{AC}, 20%, 10 nF</td>
<td>Panasonic</td>
<td>ECQ-U2A103ML</td>
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<td>1</td>
<td>C4</td>
<td>Cap, X7R, 0603, 16 V, 10%, 100 nF</td>
<td>Murata</td>
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<td>C5, C6</td>
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Typical Application (continued)

Table 1. Bill of Materials (continued)

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<th>QTY</th>
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<th>MANUFACTURER PART NUMBER</th>
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<td>ERJ-8ENF1003V</td>
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<td>ERJ-14RQJ1R8U</td>
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<td>RC1206JR-070RL</td>
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<td>CL-140</td>
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<td>SSQ 1.25</td>
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</table>
9 Power Supply Recommendations

Use any AC power supply capable of the maximum application requirements for voltage and total power.

10 Layout

10.1 Layout Guidelines

Keep the low power components for FILTER and COFF close to the LM3444 with short traces. The ISNS trace should also be as short and direct as possible. Keep the high current switching paths generated by R3, Q2, L2, and D10 as short as possible to minimize generated switching noise and improve EMI.

10.2 Layout Example

![Layout Recommendation Diagram](image-url)
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam
during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most
current data available for the designated devices. This data is subject to change without notice and revision of
this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
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<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>95</td>
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<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>L3444MA</td>
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<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAUAG</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>SZTB</td>
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<td>LM3444MMX/NOPB</td>
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<td>DGS</td>
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<td>3500</td>
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<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>SZTB</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
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TAPE AND REEL INFORMATION

<table>
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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W   (mm)</th>
<th>Pin1 Quadrant</th>
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<tbody>
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<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

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Pack Materials-Page 1
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
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<th>SPQ</th>
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<th>Width (mm)</th>
<th>Height (mm)</th>
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<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
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</tbody>
</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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