LMR10520 5.5-V_{IN}, 2-A Step-Down Voltage Regulator in WSON

1 Features

- Input Voltage Range of 3 V to 5.5 V
- Output Voltage Range of 0.6 V to 4.5 V
- Output Current up to 2 A
- 1.6-MHz (LMR10520X) and 3-MHz (LMR10520Y) Switching Frequencies
- Low Shutdown I_Q, 30 nA Typical
- Internal Soft Start
- Internally Compensated
- Current-Mode PWM Operation
- Thermal Shutdown
- Tiny Overall Solution Reduces System Cost
- WSON (3 × 3 × 0.8 mm) Packaging
- Create a custom design using the LMR10520 with the WEBENCH® Power Designer

2 Applications

- Point-of-Load Conversions from 3.3-V and 5-V Rails
- Space-Constrained Applications
- Battery-Powered Equipment
- Industrial Distributed Power Applications
- Power Meters
- Portable Hand-Held Instruments

3 Description

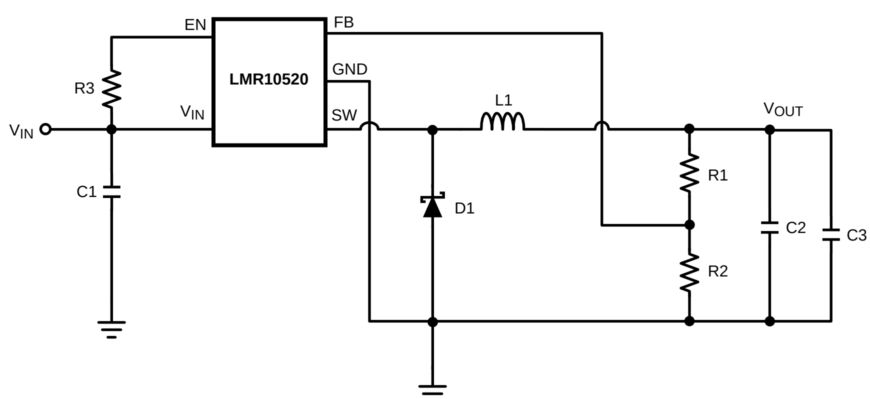
The LMR10520 regulator is a monolithic, high frequency, PWM step-down DC/DC converter in a 6-pin WSON package. It provides all the active functions to provide local DC/DC conversion with fast transient response and accurate regulation in the smallest possible PCB area. With a minimum of external components, the LMR10520 is easy to use. The ability to drive 2-A loads with an internal 150-mΩ PMOS switch results in the best power density available. The world-class control circuitry allows on-times as low as 30 ns, thus supporting exceptionally high frequency conversion over the entire 3-V to 5.5-V input operating range down to the minimum output voltage of 0.6 V. The LMR10520 is internally compensated, so it is simple to use and requires few external components. Even though the operating frequency is high, efficiencies up to 93% are easy to achieve. External shutdown is included, featuring an ultra-low stand-by current of 30 nA. The LMR10520 uses current-mode control and internal compensation to provide high-performance regulation over a wide range of operating conditions. Additional features include internal soft-start circuitry to reduce inrush current, pulse-by-pulse current limit, thermal shutdown, and output overvoltage protection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMR10520	WSON (6)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

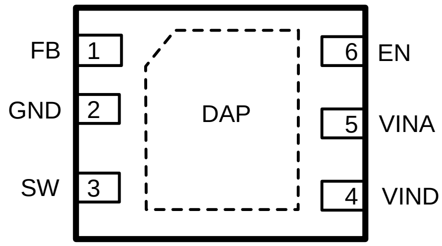
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2013) to Revision C	Page
• Editorial changes only; add WEBENCH links	1

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Semiconductor data sheet to TI format	1

5 Pin Configuration and Functions

NGG Package
6-Pin WSON
Top View



Pin Descriptions

PIN		DESCRIPTION
NO.	NAME	
1	FB	Feedback pin. Connect to external resistor divider to set output voltage.
2	GND	Signal and power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin.
3	SW	Switch node. Connect to the inductor and catch diode.
4	VIND	Power input supply.
5	VINA	Control circuitry supply voltage. Connect VINA to VIND on PC board.
6	EN	Enable control input. Logic high enables operation. Do not allow this pin to float or be greater than VINA + 0.3 V.
DAP	Die Attach Pad	Connect to system ground for low thermal impedance, but it cannot be used as a primary GND connection.

6 Specifications

6.1 Absolute Maximum Ratings

See [1][2].

VIN	-0.5V to 7V
FB Voltage	-0.5V to 3V
EN Voltage	-0.5V to 7V
SW Voltage	-0.5V to 7V
ESD Susceptibility	2kV
Junction Temperature[3]	150°C
Storage Temperature	−65°C to +150°C
Soldering Information	
For soldering specifications: http://www.ti.com/lit/SNOA549	

(1) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see *Electrical Characteristics*.
(3) Thermal shutdown occurs if the junction temperature exceeds the maximum junction temperature of the device.

6.2 Recommended Operating Ratings

VIN	3V to 5.5V
Junction Temperature	−40°C to +125°C

6.3 Electrical Characteristics

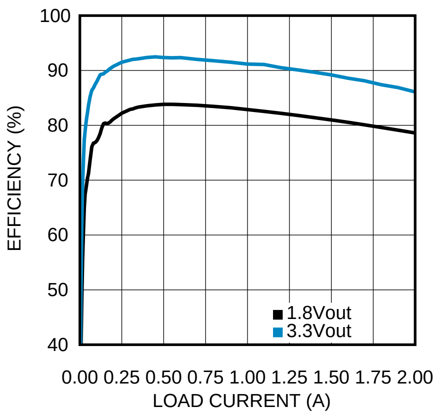
V_{IN} = 5 V unless otherwise indicated under the **TEST CONDITIONS** column. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of –40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback Voltage		**0.588**	0.600	**0.612**	V
$\Delta V_{FB}/V_{IN}$	Feedback Voltage Line Regulation	V_{IN} = 3V to 5V		0.02		%/V
I_B	Feedback Input Bias Current			0.1	**100**	nA
UVLO	Undervoltage Lockout	V_{IN} Rising		2.73	**2.90**	V
		V_{IN} Falling	**1.85**	2.3		
	UVLO Hysteresis			0.43		V
F_{SW}	Switching Frequency	LMR10520-X	**1.2**	1.6	**1.95**	MHz
		LMR10520-Y	**2.25**	3.0	**3.75**	
D_{MAX}	Maximum Duty Cycle	LMR10520-X	**86%**	94%		
		LMR10520-Y	**82%**	90%		
D_{MIN}	Minimum Duty Cycle	LMR10520-X		5%		
		LMR10520-Y		7%		
$R_{DS(ON)}$	Switch On Resistance			150		mΩ
I_{CL}	Switch Current Limit	V_{IN} = 3.3V	**2.4**	3.25		A
V_{EN_TH}	Shutdown Threshold Voltage				**0.4**	V
	Enable Threshold Voltage		**1.8**			
I_{SW}	Switch Leakage			100		nA
I_{EN}	Enable Pin Current	Sink/Source		100		nA
I_Q	Quiescent Current (switching)	LMR10520X V_{FB} = 0.55		3.3	**5**	mA
		LMR10520Y V_{FB} = 0.55		4.3	**6.5**	
	Quiescent Current (shutdown)	All Options V_{EN} = 0V		30		nA
θ_{JA}	Junction to Ambient 0 LFPM Air Flow(3)			80		°C/W
θ_{JC}	Junction to Case			18		°C/W
T_{SD}	Thermal Shutdown Temperature			165		°C

(1) Minimum and Maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) Applies for packages soldered directly onto a 3” × 3” PC board with 2 oz. copper on 4 layers in still air.

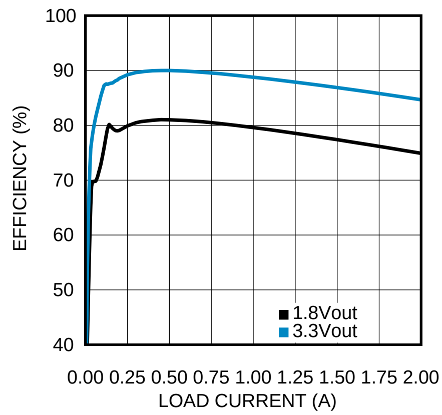
6.4 Typical Characteristics

Unless stated otherwise, all curves taken at V_{IN} = 5 V with configuration in typical application circuit shown in Figure 14. T_J = 25°C, unless otherwise specified.



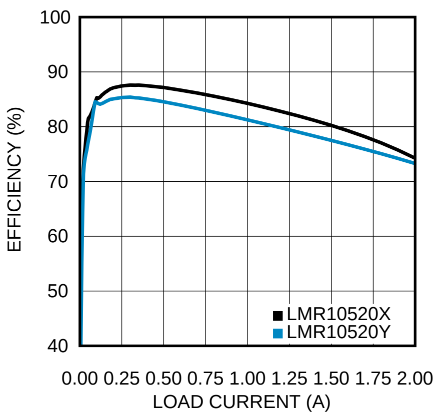
V_{IN} = 5 V V_{OUT} = 1.8 V and 3.3 V

Figure 1. Efficiency vs Load "X"



V_{IN} = 5 V V_{OUT} = 1.8 V and 3.3 V

Figure 2. Efficiency vs Load "Y"



V_{IN} = 3.3 V V_{OUT} = 1.8 V

Figure 3. Efficiency vs Load "X" and "Y"

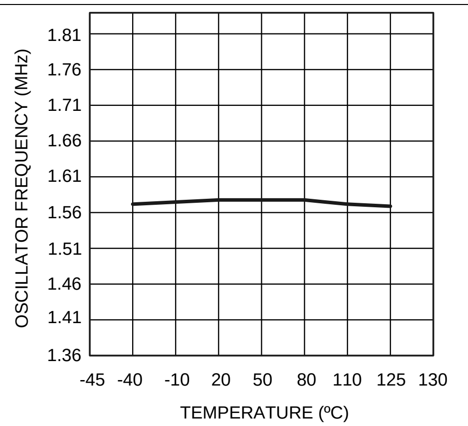


Figure 4. Oscillator Frequency vs Temperature - "X"

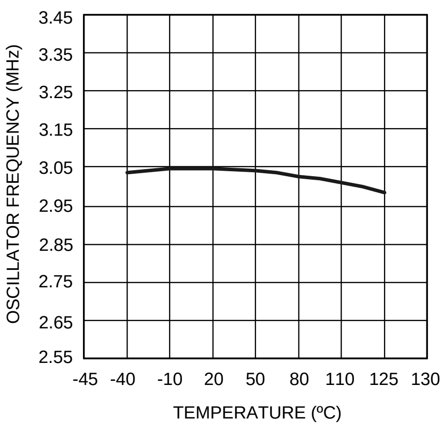
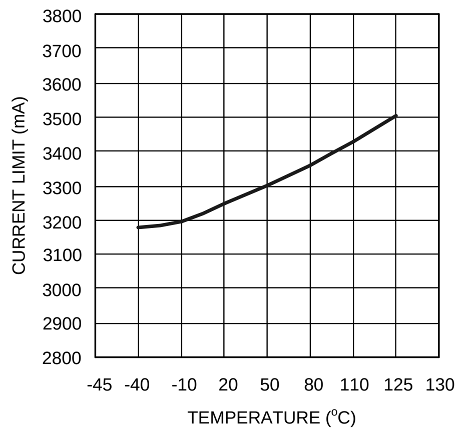


Figure 5. Oscillator Frequency vs Temperature - "Y"



V_{IN} = 3.3 V

Figure 6. Current Limit vs Temperature

Typical Characteristics (continued)

Unless stated otherwise, all curves taken at V_{IN} = 5 V with configuration in typical application circuit shown in Figure 14. T_J = 25°C, unless otherwise specified.

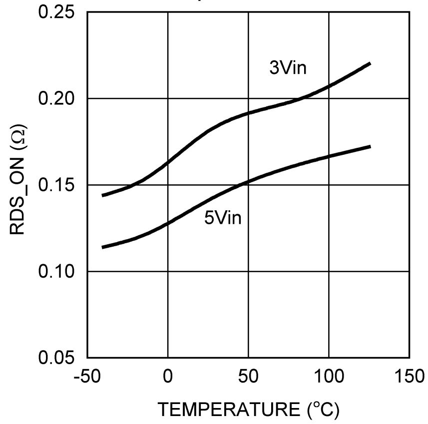


Figure 7. RD_{SON} vs Temperature

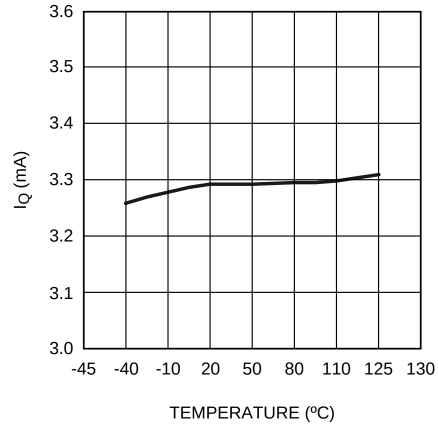


Figure 8. LMR10520X I_Q (Quiescent Current)

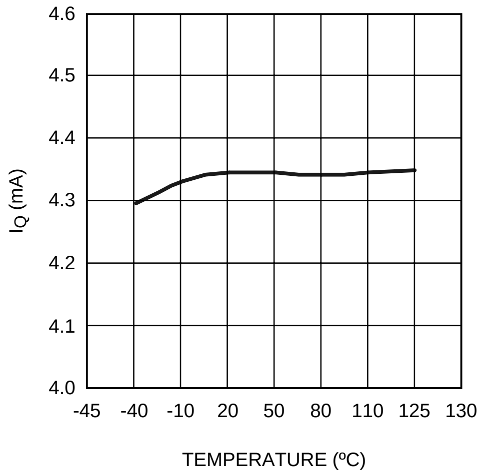


Figure 9. LMR10520Y I_Q (Quiescent Current)

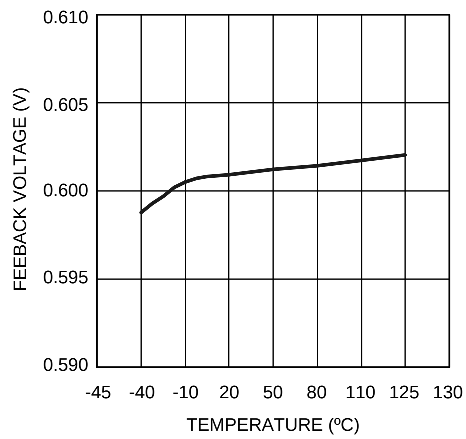
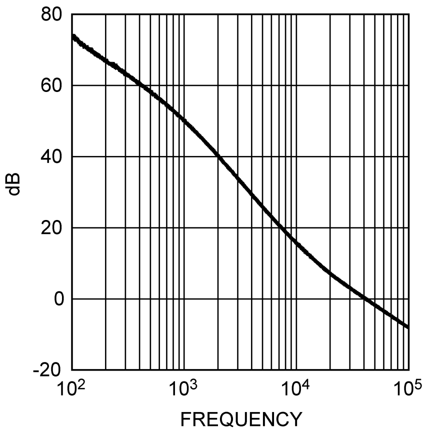
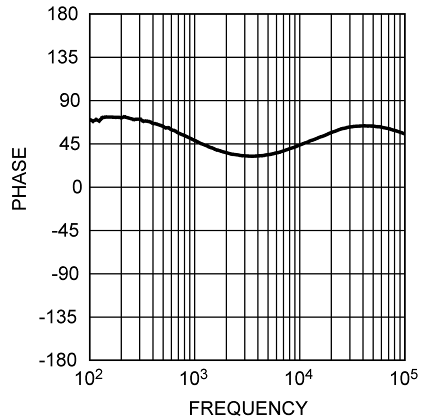


Figure 10. V_{FB} vs Temperature



V_{IN} = 5 V V_{OUT} = 1.2 V at 1 A

Figure 11. Gain vs Frequency



V_{IN} = 5 V V_{OUT} = 1.2 V at 1 A

Figure 12. Phase Plot vs Frequency

7 Detailed Description

7.1 Overview

The following operating description of the LMR10520 refers to *Functional Block Diagram* and to the waveforms in Figure 13. The LMR10520 supplies a regulated output voltage by switching the internal PMOS control switch at constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal PMOS control switch. During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current sense amplifier, which generates an output proportional to the switch current. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the output switch turns off until the next switching cycle begins. During the switch off-time, inductor current discharges through the Schottky catch diode, which forces the SW pin to swing below ground by the forward voltage (V_D) of the Schottky catch diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

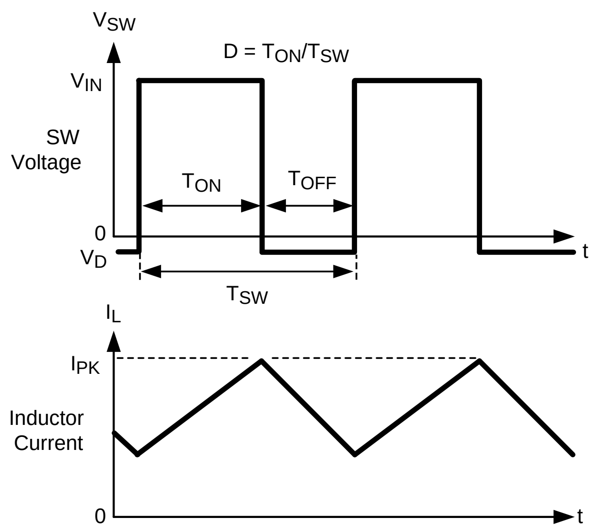
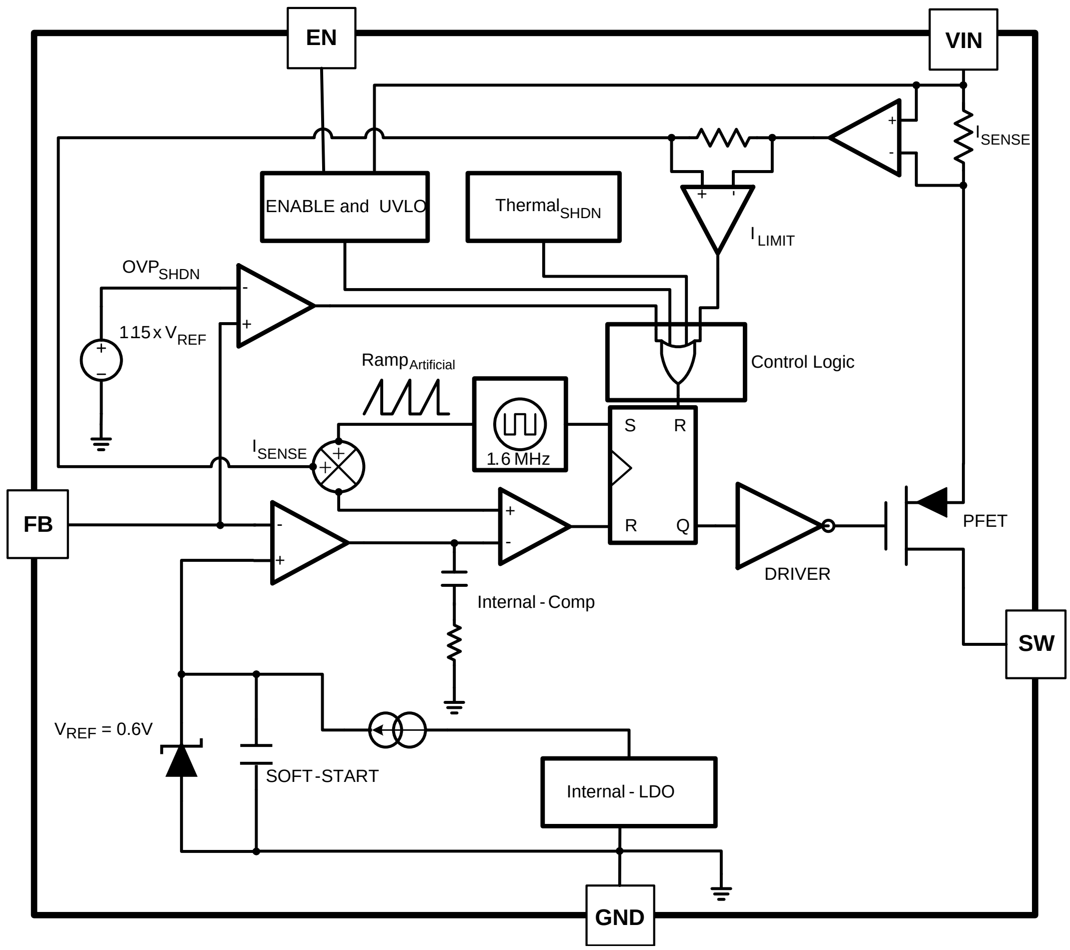


Figure 13. Typical Waveforms

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft-Start

This function forces V_{OUT} to increase at a controlled rate during start-up. During soft start, the error amplifier's reference voltage ramps from 0 V to its nominal value of 0.6 V in approximately 600 µs. This forces the regulator output to ramp up in a controlled fashion, which helps reduce inrush current.

7.3.2 Output Overvoltage Protection

The overvoltage comparator compares the FB pin voltage to a voltage that is 15% higher than the internal reference V_{REF}. Once the FB pin voltage goes 15% above the internal reference, the internal PMOS control switch is turned off, which allows the output voltage to decrease toward regulation.

7.3.3 Undervoltage Lockout

Undervoltage lockout (UVLO) prevents the LMR10520 from operating until the input voltage exceeds 2.73 V (typical). The UVLO threshold has approximately 430 mV of hysteresis, so the part will operate until V_{IN} drops below 2.3 V (typical). Hysteresis prevents the part from turning off during power-up if V_{IN} is non-monotonic.

7.3.4 Current Limit

The LMR10520 uses cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 2.5 A (typical), and turns off the switch until the next switching cycle begins.

7.3.5 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch doesn't turn on until the junction temperature drops to approximately 150°C.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMR10520 is internally compensated, so it is simple to use and requires few external components. The regulator has a preset switching frequency of 1.6 MHz or 3 MHz. This high frequency allows the LMR10520 to operate with small surface mount capacitors and inductors, resulting in a DC/DC converter that requires a minimum amount of board space

8.2 Typical Application

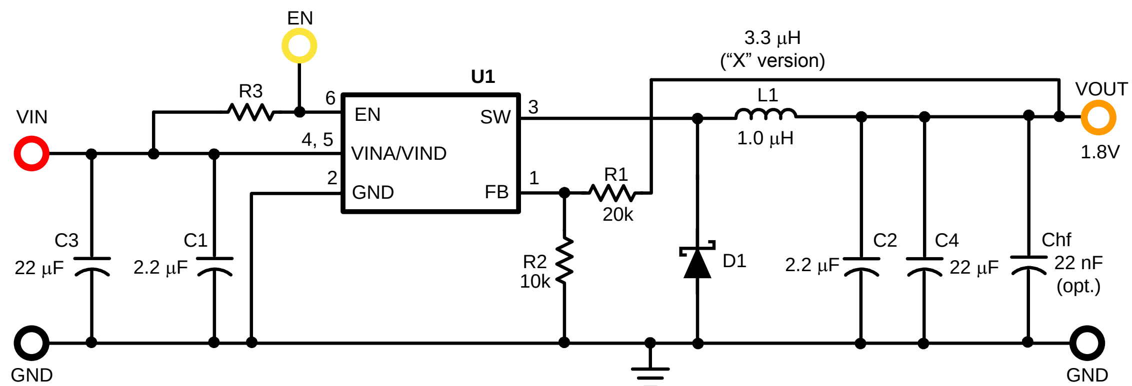


Figure 14. Typical Application Schematic

8.2.1 Detailed Design Procedure

8.2.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR10520 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

Typical Application (continued)

8.2.1.2 Inductor Selection

The duty cycle (D) can be approximated quickly using the ratio of output voltage (V_O) to input voltage (V_{IN}):

The catch diode (D1) forward-voltage drop and the voltage drop across the internal PMOS must be included to calculate a more accurate duty cycle. Calculate D by using the following formula:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}} \tag{1}$$

V_{SW} can be approximated by:

$$V_{SW} = I_{OUT} \times R_{DSON} \tag{2}$$

The diode forward drop (V_D) can range from 0.3 V to 0.7 V depending on the quality of the diode. The lower the V_D, the higher the operating efficiency of the converter. The inductor value determines the output ripple current. Lower inductor values decrease the size of the inductor, but increase the output ripple current. An increase in the inductor value will decrease the output ripple current.

One must ensure that the minimum current limit (2.4A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated by:

$$I_{LPK} = I_{OUT} + \Delta i_L \tag{3}$$

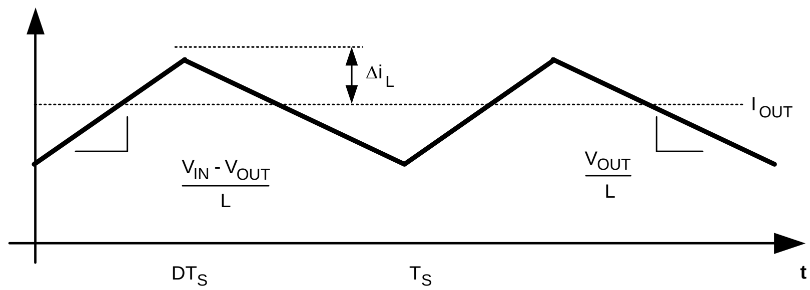


Figure 15. Inductor Current

$$\frac{V_{IN} - V_{OUT}}{L} = \frac{2\Delta i_L}{DT_S} \tag{4}$$

In general,

$$\Delta i_L = 0.1 \times (I_{OUT}) \rightarrow 0.2 \times (I_{OUT}) \tag{5}$$

If Δi_L = 20% of 2 A, the peak current in the inductor will be 2.4A. The minimum ensured current limit over all operating conditions is 2.4 A. One can either reduce Δi_L, or make the engineering judgment that zero margin will be safe enough. The typical current limit is 3.25 A.

The LMR10520 operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple. See the *Output Capacitor* section for more details on calculating output voltage ripple. Now that the ripple current is determined, the inductance is calculated by:

$$L = \left(\frac{DT_S}{2\Delta i_L}\right) \times (V_{IN} - V_{OUT})$$

where

$$T_S = \frac{1}{f_S} \qquad (7) \tag{7}$$

Typical Application (continued)

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation will result in a sudden reduction in inductance and prevent the regulator from operating correctly. Because of the speed of the internal current limit, the peak current of the inductor need only be specified for the required maximum output current. For example, if the designed maximum output current is 1 A, and the peak current is 1.25 A, then the inductor should be specified with a saturation current limit of > 1.25 A. There is no need to specify the saturation or peak current of the inductor at the 3.25 A typical switch current limit. The difference in inductor size is a factor of 5. Because of the operating frequency of the LMR10520, ferrite based inductors are preferred to minimize core losses. This presents little restriction since the variety of ferrite-based inductors is huge. Lastly, inductors with lower series resistance (R_{DCR}) will provide better operating efficiency. For recommended inductors, see *Other System Examples*.

8.2.1.3 Input Capacitor

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage, RMS current rating, and equivalent series inductance (ESL). The recommended input capacitance is 22 µF. The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating (I_{RMS-IN}) must be greater than:

$$I_{RMS\_IN} \sqrt{D\left[I_{OUT}^{2}\,(1\text{-}D) + \frac{\Delta i^{2}}{3}\right]} \tag{8}$$

Neglecting inductor ripple simplifies the above equation to:

$$I_{RMS\_IN} = I_{OUT} \times \sqrt{D(1 - D)} \tag{9}$$

It can be shown from the above equation that maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle D is closest to 0.5. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. A large leaded capacitor will have high ESL and a 0805 ceramic chip capacitor will have very low ESL. At the operating frequencies of the LMR10520, leaded capacitors may have an ESL so large that the resulting impedance (2πfL) will be higher than that required to provide stable operation. As a result, surface mount capacitors are strongly recommended.

Sanyo POSCAP, Tantalum or Niobium, Panasonic SP, and multilayer ceramic capacitors (MLCC) are all good choices for both input and output capacitors and have very low ESL. For MLCCs it is recommended to use X7R or X5R type capacitors due to their tolerance and temperature characteristics. Consult capacitor manufacturer datasheets to see how rated capacitance varies over operating conditions.

8.2.1.4 Output Capacitor

The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output ripple of the converter is:

$$\Delta V_{OUT} = \Delta I_L \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \tag{10}$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple will be approximately sinusoidal and 90° phase shifted from the switching action. Given the availability and quality of MLCCs and the expected output voltage of designs using the LMR10520, there is really no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise will couple through parasitic capacitances in the inductor to the output. A ceramic capacitor will bypass this noise while a tantalum will not. Since the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications will require a minimum of 22 µF of output capacitance. Capacitance often, but not always, can be increased significantly with little detriment to the regulator stability. Like the input capacitor, recommended multilayer ceramic capacitors are X7R or X5R types.

Typical Application (continued)

8.2.1.5 Catch Diode

The catch diode (D1) conducts during the switch off-time. A Schottky diode is recommended for its fast switching times and low forward voltage drop. The catch diode should be chosen so that its current rating is greater than:

$$I_{D1} = I_{OUT} \times (1\text{-}D) \tag{11}$$

The reverse breakdown rating of the diode must be at least the maximum input voltage plus appropriate margin. To improve efficiency, choose a Schottky diode with a low forward voltage drop.

8.2.1.6 Output Voltage

The output voltage is set using the following equation where R2 is connected between the FB pin and GND, and R1 is connected between V_O and the FB pin. A good value for R2 is 10kΩ. When designing a unity gain converter (Vo = 0.6V), R1 should be between 0Ω and 100Ω, and R2 should be equal or greater than 10kΩ.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \tag{12}$$

$$V_{REF} = 0.60V \tag{13}$$

8.2.1.7 Calculating Efficiency and Junction Temperature

The complete LMR10520 DC/DC converter efficiency can be calculated in the following manner.

$$\eta = \frac{P_{OUT}}{P_{IN}} \tag{14}$$

Or

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \tag{15}$$

Calculations for determining the most significant power losses are shown below. Other losses totaling less than 2% are not discussed.

Power loss (P_{LOSS}) is the sum of two basic types of losses in the converter: switching and conduction. Conduction losses usually dominate at higher output loads, whereas switching losses remain relatively fixed and dominate at lower output loads. The first step in determining the losses is to calculate the duty cycle (D):

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}} \tag{16}$$

V_{SW} is the voltage drop across the internal PFET when it is on, and is equal to:

$$V_{SW} = I_{OUT} \times R_{DSON} \tag{17}$$

V_D is the forward voltage drop across the Schottky catch diode. It can be obtained from the diode manufactures Electrical Characteristics section. If the voltage drop across the inductor (V_{DCR}) is accounted for, the equation becomes:

$$D = \frac{V_{OUT} + V_D + V_{DCR}}{V_{IN} + V_D + V_{DCR} - V_{SW}} \tag{18}$$

The conduction losses in the free-wheeling Schottky diode are calculated as follows:

$$P_{DIODE} = V_D \times I_{OUT} \times (1\text{-}D) \tag{19}$$

Often this is the single most significant power loss in the circuit. Care should be taken to choose a Schottky diode that has a low forward voltage drop.

Typical Application (continued)

Another significant external power loss is the conduction loss in the output inductor. The equation can be simplified to:

$$P_{IND} = I_{OUT}^2 \times R_{DCR} \quad (20)$$

The LMR10520 conduction loss is mainly associated with the internal PFET:

$$P_{COND} = (I_{OUT}^2 \times D)\left(1 + \frac{1}{3} \times \left(\frac{\Delta i_L}{I_{OUT}}\right)^2\right) R_{DSON} \quad (21)$$

If the inductor ripple current is fairly small, the conduction losses can be simplified to:

$$P_{COND} = I_{OUT}^2 \times R_{DSON} \times D \quad (22)$$

Switching losses are also associated with the internal PFET. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss. The simplest means to determine this loss is to empirically measuring the rise and fall times (10% to 90%) of the switch at the switch node.

Switching Power Loss is calculated as follows:

$$P_{SWR} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{RISE}) \quad (23)$$

$$P_{SWF} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{FALL}) \quad (24)$$

$$P_{SW} = P_{SWR} + P_{SWF} \quad (25)$$

Another loss is the power required for operation of the internal circuitry:

$$P_Q = I_Q \times V_{IN} \quad (26)$$

I_Q is the quiescent operating current, and is typically around 3.3 mA for the 1.6-MHz frequency option.

Typical application power losses are:

Table 1. Power Loss Tabulation

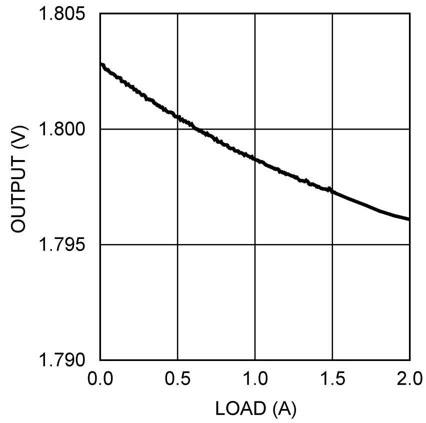
V_{IN}	5 V		
V_{OUT}	3.3 V	P_{OUT}	5.78 W
I_{OUT}	1.75 A		
V_D	0.45 V	P_{DIODE}	262 mW
F_{SW}	1.6 MHz		
I_Q	3.3 mA	P_Q	16.5 mW
T_{RISE}	4 ns	P_{SWR}	28 mW
T_{FALL}	4 ns	P_{SWF}	28 mW
$R_{DS(ON)}$	150 mΩ	P_{COND}	306 mW
IND_{DCR}	50 mΩ	P_{IND}	153 mW
D	0.667	P_{LOSS}	794 mW
η	88%	$P_{INTERNAL}$	379 mW

$$\Sigma P_{COND} + P_{SW} + P_{DIODE} + P_{IND} + P_Q = P_{LOSS} \quad (27)$$

$$\Sigma P_{COND} + P_{SWF} + P_{SWR} + P_Q = P_{INTERNAL} \quad (28)$$

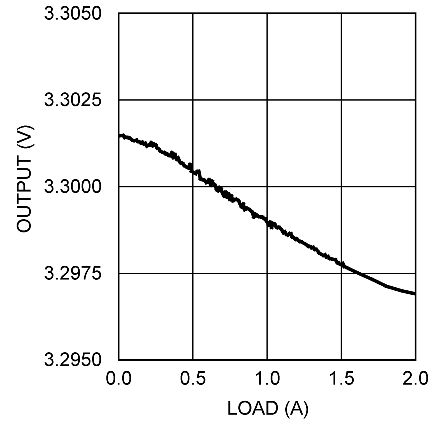
$$P_{INTERNAL} = 379\text{mW} \quad (29)$$

8.2.2 Application Curves



V_{IN} = 3.3 V V_{OUT} = 1.8 V (All Options)

Figure 16. Load Regulation



V_{IN} = 3.3 V V_{OUT} = 3.3 V (All Options)

Figure 17. Load Regulation

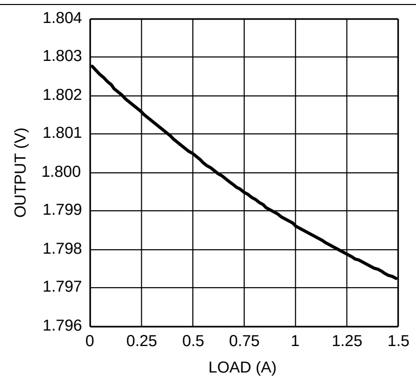
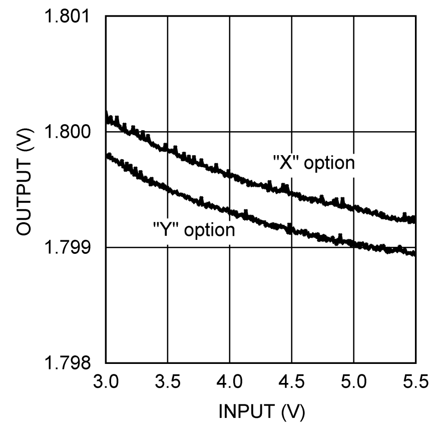


Figure 18. Load Regulation



V_{OUT} = 1.8 V I_{OUT} = 500 mA

Figure 19. Line Regulation

8.2.3 Other System Examples

8.2.3.1 LMR10520X Design Example 1

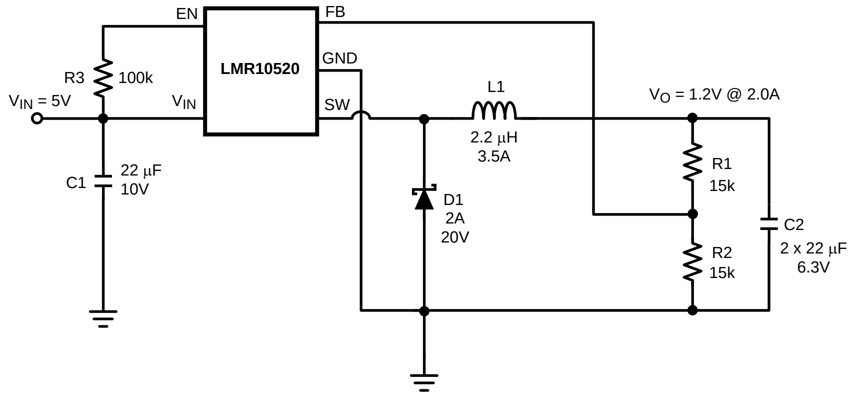


Figure 20. LMR10520x (1.6 MHz): V_{IN} = 5 V, V_{OUT} = 1.2 V at 2 A

8.2.3.2 LMR10510X Design Example 2

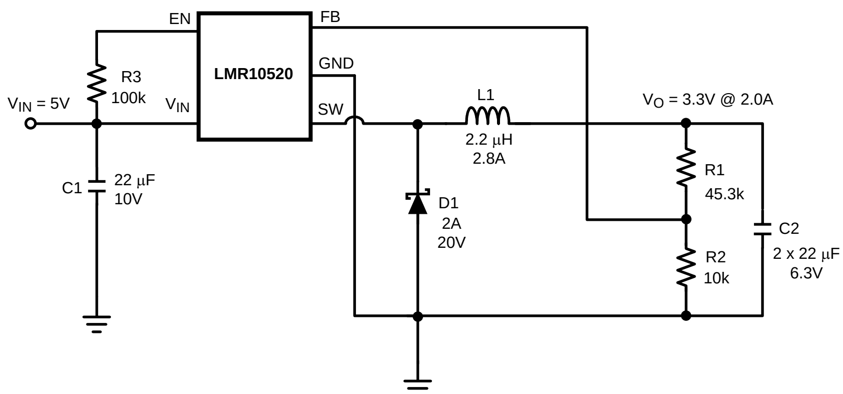


Figure 21. LMR10520X (1.6 MHz): V_{IN} = 5 V, V_{OUT} = 3.3 V at 2 A

8.2.3.3 LMR10510Y Design Example 3

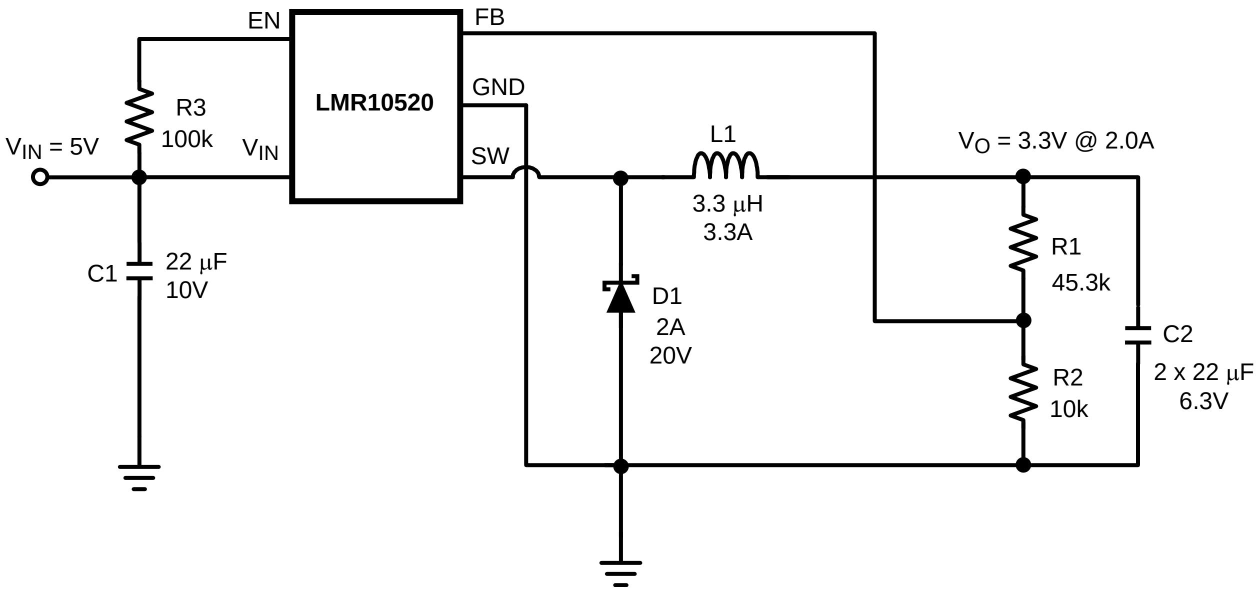


Figure 22. LMR10520Y (3 MHz): V_{IN} = 5 V, V_{OUT} = 3.3 V at 2 A

8.2.3.4 LMR10510Y Design Example 4

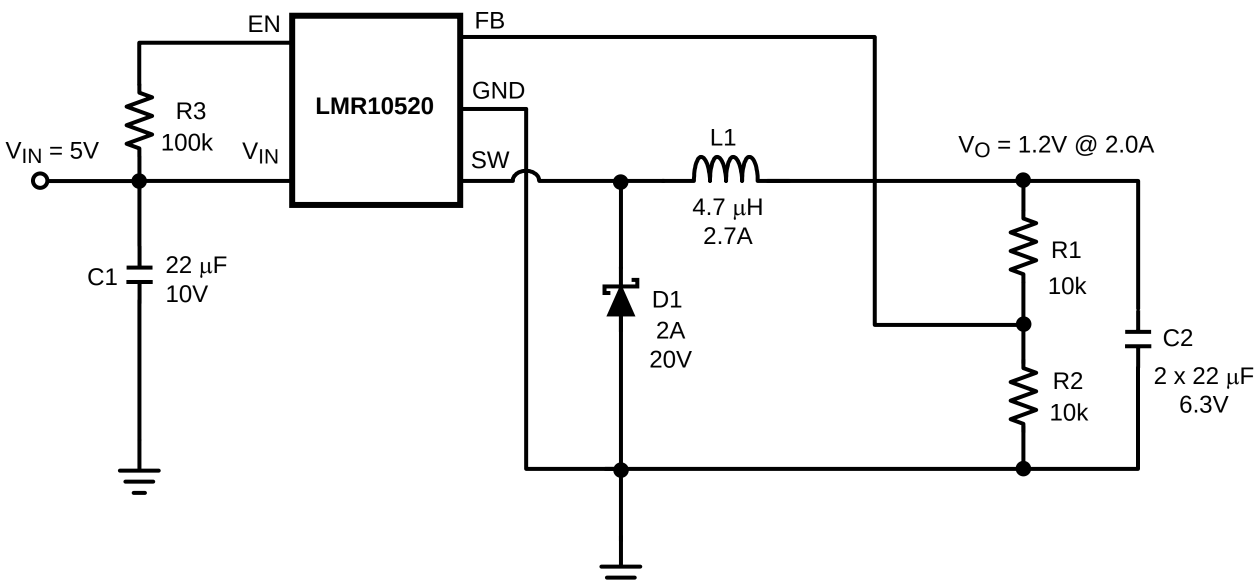


Figure 23. LMR10520Y (3 MHz): V_{IN} = 5 V, V_{OUT} = 1.2 V at 2 A

9 Layout

9.1 Layout Guidelines

When planning layout there are a few things to consider when trying to achieve a clean, regulated output. The most important consideration is the close coupling of the GND connections of the input capacitor and the catch diode D1. Place these ground ends close to one another and be connected to the GND plane with at least two through-holes. Place these components as close to the IC as possible. Next in importance is the location of the GND connection of the output capacitor, which should be near the GND connections of CIN and D1. There should be a continuous ground plane on the bottom layer of a two-layer board except under the switching node island. The FB pin is a high impedance node and care should be taken to make the FB trace short to avoid noise pickup and inaccurate regulation. Place the feedback resistors as close as possible to the IC, with the GND of R1 placed as close as possible to the GND of the IC. Route the V_{OUT} trace to R2 away from the inductor and any other traces that are switching. High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they should be as short and wide as possible. However, making the traces wide increases radiated noise, so the designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor. The remaining components should also be placed as close as possible to the IC. See

Application Note AN-1229 for further considerations and the LMR10520 demo board as an example of a good layout.

9.2 Layout Example

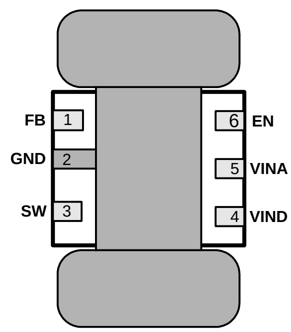


Figure 24. 6-Lead WSON PCB Dog-Bone Layout

9.3 Thermal Definitions

T_J = Chip junction temperature

T_A = Ambient temperature

$R_{\theta JC}$ = Thermal resistance from chip junction to device case

$R_{\theta JA}$ = Thermal resistance from chip junction to ambient air

Heat in the LMR10520 due to internal power dissipation is removed through conduction and/or convection.

Conduction: Heat transfer occurs through cross sectional areas of material. Depending on the material, the transfer of heat can be considered to have poor to good thermal conductivity properties (insulator vs. conductor).

Heat Transfer goes as:

Silicon → package → lead frame → PCB

Convection: Heat transfer is by means of airflow. This could be from a fan or natural convection. Natural convection occurs when air currents rise from the hot device to cooler air.

Thermal impedance is defined as:

$$R_{\theta} = \frac{\Delta T}{Power} \tag{30}$$

Thermal impedance from the silicon junction to the ambient air is defined as:

$$R_{\theta JA} = \frac{T_J - T_A}{Power} \tag{31}$$

The PCB size, weight of copper used to route traces and ground plane, and number of layers within the PCB can greatly effect $R_{\theta JA}$. The type and number of thermal vias can also make a large difference in the thermal impedance. Thermal vias are necessary in most applications. They conduct heat from the surface of the PCB to the ground plane. Four to six thermal vias should be placed under the exposed pad to the ground plane.

Thermal impedance also depends on the thermal properties of the application operating conditions (Vin, Vo, Io etc), and the surrounding circuitry.

Silicon Junction Temperature Determination Method 1:

To accurately measure the silicon temperature for a given application, two methods can be used. The first method requires the user to know the thermal impedance of the silicon junction to case temperature.

$R_{\theta JC}$ is approximately 18°C/Watt for the 6-pin WSON package with the exposed pad. Knowing the internal dissipation from the efficiency calculation given previously, and the case temperature, which can be empirically measured on the bench we have:

$$R_{\theta JC} = \frac{T_J - T_C}{Power}$$

where

- T_C is the temperature of the exposed pad and can be measured on the bottom side of the PCB. (32)

Therefore:

$$T_j = (R_{\theta JC} \times P_{LOSS}) + T_C \tag{33}$$

From the previous example:

$$T_j = (R_{\theta JC} \times P_{INTERNAL}) + T_C \tag{34}$$

$$T_j = 18°C/W \times 0.213W + T_C \tag{35}$$

The second method can give a very accurate silicon junction temperature.

Thermal Definitions (continued)

The first step is to determine $R_{\theta JA}$ of the application. The LMR10520 has over-temperature protection circuitry. When the silicon temperature reaches 165°C, the device stops switching. The protection circuitry has a hysteresis of about 15°C. Once the silicon temperature has decreased to approximately 150°C, the device will start to switch again. Knowing this, the $R_{\theta JA}$ for any application can be characterized during the early stages of the design one may calculate the $R_{\theta JA}$ by placing the PCB circuit into a thermal chamber. Raise the ambient temperature in the given working application until the circuit enters thermal shutdown. If the SW-pin is monitored, it will be obvious when the internal PFET stops switching, indicating a junction temperature of 165°C. Knowing the internal power dissipation from the above methods, the junction temperature, and the ambient temperature $R_{\theta JA}$ can be determined.

$$R_{\theta JA} = \frac{165° - Ta}{P_{INTERNAL}} \tag{36}$$

Once this is determined, the maximum ambient temperature allowed for a desired junction temperature can be found.

An example of calculating $R_{\theta JA}$ for an application using the LMR10520 is shown below.

A sample PCB is placed in an oven with no forced airflow. The ambient temperature was raised to 120°C, and at that temperature, the device went into thermal shutdown.

From the previous example:

$$P_{INTERNAL} = 379\ \text{mW} \tag{37}$$

$$R_{\theta JA} = \frac{165°C - 120°C}{379\ \text{mW}} = 119°C/W \tag{38}$$

Since the junction temperature must be kept below 125°C, then the maximum ambient temperature can be calculated as:

$$T_j - (R_{\theta JA} \times P_{LOSS}) = T_A \tag{39}$$

$$125°C – (119°C/W \times 379\ \text{mW}) = 80°C \tag{40}$$

9.4 WSON Package

For certain high power applications, the PCB land may be modified to a "dog bone" shape (see Figure 24). By increasing the size of ground plane, and adding thermal vias, the $R_{\theta JA}$ for the application can be reduced.

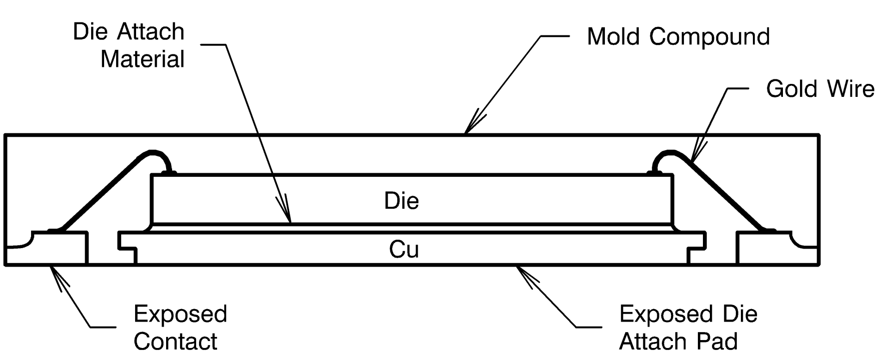


Figure 25. Internal WSON Connection

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.1.2 Development Support

10.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR10520 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.4 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR10520XSD/NOPB	ACTIVE	WSON	NGG	6	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L266B	Samples
LMR10520XSDE/NOPB	ACTIVE	WSON	NGG	6	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L266B	Samples
LMR10520XSDX/NOPB	ACTIVE	WSON	NGG	6	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L266B	Samples
LMR10520YSD/NOPB	ACTIVE	WSON	NGG	6	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L267B	Samples
LMR10520YSDE/NOPB	ACTIVE	WSON	NGG	6	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L267B	Samples
LMR10520YSDX/NOPB	ACTIVE	WSON	NGG	6	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L267B	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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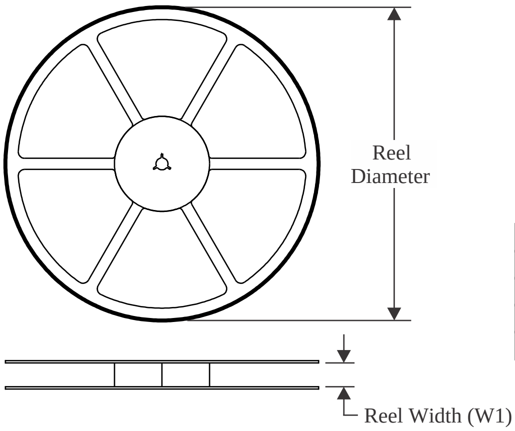
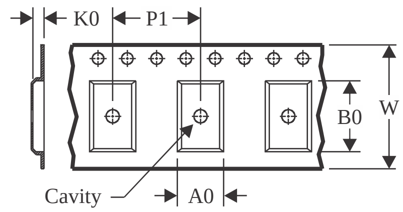
TAPE AND REEL INFORMATION

REEL DIMENSIONS

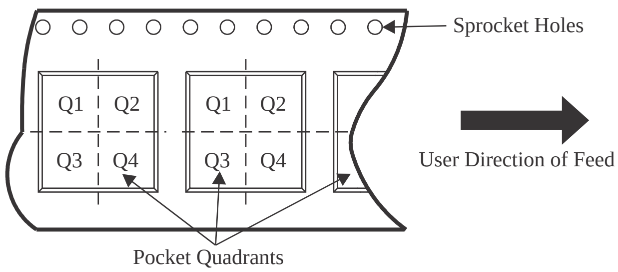


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

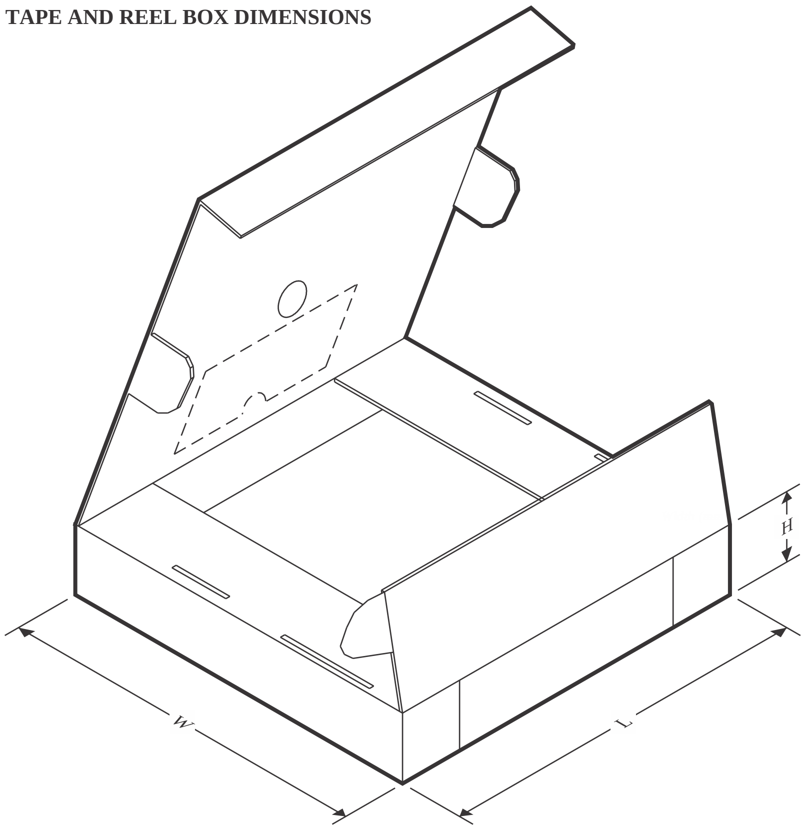
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR10520XSD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR10520XSDE/NOPB	WSON	NGG	6	250	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR10520XSDX/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR10520YSD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR10520YSDE/NOPB	WSON	NGG	6	250	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR10520YSDX/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

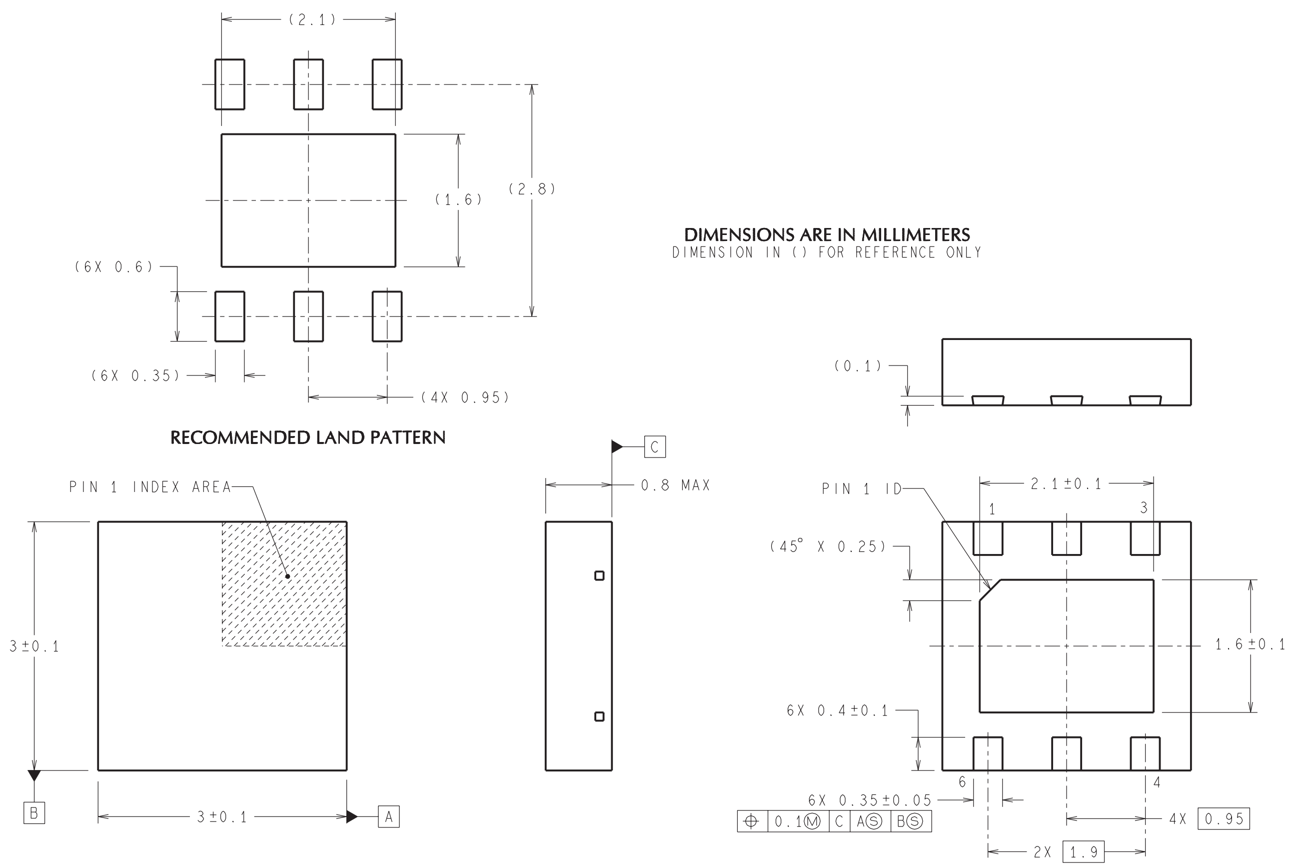
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR10520XSD/NOPB	WSON	NGG	6	1000	208.0	191.0	35.0
LMR10520XSDE/NOPB	WSON	NGG	6	250	208.0	191.0	35.0
LMR10520XSDX/NOPB	WSON	NGG	6	4500	356.0	356.0	35.0
LMR10520YSD/NOPB	WSON	NGG	6	1000	208.0	191.0	35.0
LMR10520YSDE/NOPB	WSON	NGG	6	250	208.0	191.0	35.0
LMR10520YSDX/NOPB	WSON	NGG	6	4500	356.0	356.0	35.0

NGG0006A



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