LMR64010 SIMPLE SWITCHER® 40Vout, 1A Step-Up Voltage Regulator in SOT-23

Check for Samples: LMR64010

FEATURES
- Input Voltage Range of 2.7V to 14V
- Output Voltage up to 40V
- Switch Current up to 1A
- 1.6 MHz Switching Frequency
- Low Shutdown Iq, <1 µA
- Cycle-by-Cycle Current Limiting
- Internally Compensated
- SOT-23-5 Packaging (2.92 x 2.84 x 1.08mm)
- Fully Enabled for WEBENCH® Power Designer

DESCRIPTION
The LMR64010 switching regulators is a current-mode boost converter operating at a fixed frequency of 1.6 MHz.

The use of SOT-23 package, made possible by the minimal power loss of the internal 1A switch, and use of small inductors and capacitors result in the industry's highest power density. The 40V internal switch makes these solutions perfect for boosting to voltages of 16V or greater.

These parts have a logic-level shutdown pin that can be used to reduce quiescent current and extend battery life.

Protection is provided through cycle-by-cycle current limiting and thermal shutdown. Internal compensation simplifies design and reduces component count.

PERFORMANCE BENEFITS
- Extremely Easy to Use
- Tiny Overall Solution Reduces System Cost

APPLICATIONS
- Boost Conversions from 3.3V, 5V, and 12V Rails
- Space Constrained Applications
- Embedded Systems
- LCD Displays
- LED Applications

System Performance

![Efficiency vs. Load Current](image)

![Efficiency vs. Load Current](image)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Copyright © 2011–2013, Texas Instruments Incorporated

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.
PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SW</td>
<td>Drain of the internal FET switch.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Analog and power ground.</td>
</tr>
<tr>
<td>3</td>
<td>FB</td>
<td>Feedback point that connects to external resistive divider.</td>
</tr>
<tr>
<td>4</td>
<td>SHDN</td>
<td>Shutdown control input. Connect to ( V_{IN} ) if this feature is not used.</td>
</tr>
<tr>
<td>5</td>
<td>( V_{IN} )</td>
<td>Analog and power input.</td>
</tr>
</tbody>
</table>
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Operating Junction Temperature Range</td>
<td>−40°C to +125°C</td>
</tr>
<tr>
<td>Lead Temp. (Soldering, 5 sec.)</td>
<td>300°C</td>
</tr>
<tr>
<td>Power Dissipation(3)</td>
<td>Internally Limited</td>
</tr>
<tr>
<td>FB Pin Voltage</td>
<td>−0.4V to +6V</td>
</tr>
<tr>
<td>SW Pin Voltage</td>
<td>−0.4V to +40V</td>
</tr>
<tr>
<td>Input Supply Voltage</td>
<td>−0.4V to +14.5V</td>
</tr>
<tr>
<td>SHDN Pin Voltage</td>
<td>−0.4V to VIN + 0.3V</td>
</tr>
<tr>
<td>( \theta_{J-A} ) (SOT-23-5)</td>
<td>265°C/W</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ESD Rating (4)</th>
<th>Description</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human Body Model</td>
<td></td>
<td>2 kV</td>
</tr>
<tr>
<td>Machine Model</td>
<td></td>
<td>200V</td>
</tr>
</tbody>
</table>

For soldering specifications: [http://www.ti.com/lit/SNOA549](http://www.ti.com/lit/SNOA549)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of the limits set forth under the operating ratings which specify the intended range of operating conditions.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) The maximum power dissipation which can be safely dissipated for any application is a function of the maximum junction temperature, \( T_{J \text{MAX}} = 125°C \), the junction-to-ambient thermal resistance for the SOT-23 package, \( \theta_{J-A} = 265°C/W \), and the ambient temperature, \( T_A \). The maximum allowable power dissipation at any ambient temperature for designs using this device can be calculated using the formula:

\[
P_{(\text{MAX})} = \frac{T_{J \text{MAX}} - T_A}{\theta_{J-A}} = \frac{125 - T_A}{265}
\]

If power dissipation exceeds the maximum specified above, the internal thermal protection circuitry will protect the device by reducing the output voltage as required to maintain a safe junction temperature.

(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.
**Electrical Characteristics**

Limits in standard typeface are for $T_J = 25^\circ C$, and limits in **boldface type** apply over the full operating temperature range ($-40^\circ C \leq T_J \leq +125^\circ C$). Unless otherwise specified: $V_{IN} = 5V$, $V_{SHDN} = 5V$, $I_L = 0A$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min$^{(1)}$</th>
<th>Typ$^{(2)}$</th>
<th>Max$^{(1)}$</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input Voltage</td>
<td>2.7</td>
<td></td>
<td>14</td>
<td>V</td>
</tr>
<tr>
<td>$I_{SW}$</td>
<td>Switch Current Limit</td>
<td>See$^{(3)}$</td>
<td>1.0</td>
<td>1.5</td>
<td>A</td>
</tr>
<tr>
<td>$R_{DS(ON)}$</td>
<td>Switch ON Resistance</td>
<td>$I_{SW} = 100$ mA</td>
<td>500</td>
<td>650</td>
<td>mΩ</td>
</tr>
<tr>
<td>$SHDN_{TH}$</td>
<td>Shutdown Threshold</td>
<td>Device ON</td>
<td>1.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Device OFF</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SHDN}$</td>
<td>Shutdown Pin Bias Current</td>
<td>$V_{SHDN} = 0$</td>
<td>0</td>
<td>0</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{SHDN} = 5V$</td>
<td>0</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>$V_{FB}$</td>
<td>Feedback Pin Reference Voltage</td>
<td>$V_{IN} = 3V$</td>
<td>1.205</td>
<td>1.230</td>
<td>1.255</td>
</tr>
<tr>
<td>$I_{FB}$</td>
<td>Feedback Pin Bias Current</td>
<td>$V_{FB} = 1.23V$</td>
<td>60</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent Current</td>
<td>$V_{SHDN} = 5V$, Switching</td>
<td>2.1</td>
<td>3.0</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{SHDN} = 5V$, Not Switching</td>
<td>400</td>
<td>500</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{SHDN} = 0$</td>
<td>0.024</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{FB}$</td>
<td>FB Voltage Line Regulation</td>
<td>$2.7V \leq V_{IN} \leq 14V$</td>
<td>0.02</td>
<td></td>
<td>%/V</td>
</tr>
<tr>
<td>$F_{SW}$</td>
<td>Switching Frequency</td>
<td>1.15</td>
<td>1.6</td>
<td>1.85</td>
<td>MHz</td>
</tr>
<tr>
<td>$D_{MAX}$</td>
<td>Maximum Duty Cycle</td>
<td>87</td>
<td>93</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$I_L$</td>
<td>Switch Leakage</td>
<td>Not Switching $V_{SW} = 5V$</td>
<td>1</td>
<td></td>
<td>µA</td>
</tr>
</tbody>
</table>

$^{(1)}$ Limits are ensured by testing, statistical correlation, or design.

$^{(2)}$ Typical values are derived from the mean value of a large quantity of samples tested during characterization and represent the most likely expected value of the parameter at room temperature.

$^{(3)}$ Switch current limit is dependent on duty cycle (see **Typical Performance Characteristics**). Limits shown are for duty cycles $\leq 50\%$.
Typical Performance Characteristics

Unless otherwise specified: $V_{IN} = 5V$, SHDN pin is tied to $V_{IN}$.

![IQ VIN (Active) vs Temperature](image1)

![Oscillator Frequency vs Temperature](image2)

![Max. Duty Cycle vs Temperature](image3)

![Feedback Voltage vs Temperature](image4)

![RDS(ON) vs Temperature](image5)

![Current Limit vs Temperature](image6)
Typical Performance Characteristics (continued)

Unless otherwise specified: $V_{IN} = 5\, \text{V}$, SHDN pin is tied to $V_{IN}$.

**Figure 8.**

**Figure 9.**

**Figure 10.**

**Figure 11.**

**Figure 12.**

**Figure 13.**
Typical Performance Characteristics (continued)

Unless otherwise specified: \( V_{IN} = 5V \), SHDN pin is tied to \( V_{IN} \).

**Efficiency vs Load Current (\( V_{OUT} = 35V \))**

![Graph 1](image1)

**Efficiency vs Load Current (\( V_{OUT} = 40V \))**

![Graph 2](image2)

**Block Diagram**

![Block Diagram](image3)

Copyright © 2011–2013, Texas Instruments Incorporated
APPLICATION INFORMATION

Theory of Operation

The LMR64010 is a switching converter IC that operates at a fixed frequency (1.6 MHz) using current-mode control for fast transient response over a wide input voltage range and incorporates pulse-by-pulse current limiting protection. Because this is current mode control, a 50 mΩ sense resistor in series with the switch FET is used to provide a voltage (which is proportional to the FET current) to both the input of the pulse width modulation (PWM) comparator and the current limit amplifier.

At the beginning of each cycle, the S-R latch turns on the FET. As the current through the FET increases, a voltage (proportional to this current) is summed with the ramp coming from the ramp generator and then fed into the input of the PWM comparator. When this voltage exceeds the voltage on the other input (coming from the Gm amplifier), the latch resets and turns the FET off. Since the signal coming from the Gm amplifier is derived from the feedback (which samples the voltage at the output), the action of the PWM comparator constantly sets the correct peak current through the FET to keep the output voltage in regulation.

Q1 and Q2 along with R3 - R6 form a bandgap voltage reference used by the IC to hold the output in regulation. The currents flowing through Q1 and Q2 will be equal, and the feedback loop will adjust the regulated output to maintain this. Because of this, the regulated output is always maintained at a voltage level equal to the voltage at the FB node "multiplied up" by the ratio of the output resistive divider.

The current limit comparator feeds directly into the flip-flop, that drives the switch FET. If the FET current reaches the limit threshold, the FET is turned off and the cycle terminated until the next clock pulse. The current limit input terminates the pulse regardless of the status of the output of the PWM comparator.

Application Hints

SELECTING THE EXTERNAL CAPACITORS

The best capacitors for use with the LMR64010 are multi-layer ceramic capacitors. They have the lowest ESR (equivalent series resistance) and highest resonance frequency which makes them optimum for use with high frequency switching converters.

When selecting a ceramic capacitor, only X5R and X7R dielectric types should be used. Other types such as Z5U and Y5F have such severe loss of capacitance due to effects of temperature variation and applied voltage, they may provide as little as 20% of rated capacitance in many typical applications. Always consult capacitor manufacturer’s data curves before selecting a capacitor.

SELECTING THE OUTPUT CAPACITOR

A single ceramic capacitor of value 4.7 µF to 10 µF will provide sufficient output capacitance for most applications. For output voltages below 10V, a 10 µF capacitance is required. If larger amounts of capacitance are desired for improved line support and transient response, tantalum capacitors can be used in parallel with the ceramics. Aluminum electrolytics with ultra low ESR such as Sanyo Oscon can be used, but are usually prohibitively expensive. Typical Al electrolytic capacitors are not suitable for switching frequencies above 500 kHz due to significant ringing and temperature rise due to self-heating from ripple current. An output capacitor with excessive ESR can also reduce phase margin and cause instability.

SELECTING THE INPUT CAPACITOR

An input capacitor is required to serve as an energy reservoir for the current which must flow into the coil each time the switch turns ON. This capacitor must have extremely low ESR, so ceramic is the best choice. We recommend a nominal value of 2.2 µF, but larger values can be used. Since this capacitor reduces the amount of voltage ripple seen at the input pin, it also reduces the amount of EMI passed back along that line to other circuitry.
FEED-FORWARD COMPENSATION

Although internally compensated, the feed-forward capacitor $C_f$ is required for stability (see Basic Application Circuit). Adding this capacitor puts a zero in the loop response of the converter. Without it, the regulator loop can oscillate. The recommended frequency for the zero $f_z$ should be approximately 8 kHz. $C_f$ can be calculated using the formula:

$$C_f = \frac{1}{(2 \times \pi \times R_1 \times f_z)}$$

(1)

SELECTING DIODES

The external diode used in the typical application should be a Schottky diode. If the switch voltage is less than 15V, a 20V diode such as the MBR0520 is recommended. If the switch voltage is between 15V and 25V, a 30V diode such as the MBR0530 is recommended. If the switch voltage exceeds 25V, a 40V diode such as the MBR0540 should be used.

The MBR05XX series of diodes are designed to handle a maximum average current of 0.5A. For applications exceeding 0.5A average but less than 1A, a Toshiba CRS08 can be used.

LAYOUT HINTS

High frequency switching regulators require very careful layout of components in order to get stable operation and low noise. All components must be as close as possible to the LMR64010 device. It is recommended that a 4-layer PCB be used so that internal ground planes are available.

As an example, a recommended layout of components is shown:

---

Figure 16. Recommended PCB Component Layout

---

Some additional guidelines to be observed:

1. Keep the path between $L_1$, $D_1$, and $C_2$ extremely short. Parasitic trace inductance in series with $D_1$ and $C_2$ will increase noise and ringing.
2. The feedback components $R_1$, $R_2$ and $C_F$ must be kept close to the FB pin of $U_1$ to prevent noise injection on the FB pin trace.
3. If internal ground planes are available (recommended) use vias to connect directly to ground at pin 2 of $U_1$, as well as the negative sides of capacitors $C_1$ and $C_2$.  

Copyright © 2011–2013, Texas Instruments Incorporated

Submit Documentation Feedback

Product Folder Links: LMR64010
Setting the Output Voltage

The output voltage is set using the external resistors R1 and R2 (see Basic Application Circuit). A value of approximately 13.3 kΩ is recommended for R2 to establish a divider current of approximately 92 µA. R1 is calculated using the formula:

\[ R1 = R2 \times \left( \frac{V_{OUT}}{1.23} - 1 \right) \]  

(2)

Duty Cycle

The maximum duty cycle of the switching regulator determines the maximum boost ratio of output-to-input voltage that the converter can attain in continuous mode of operation. The duty cycle for a given boost application is defined as:

\[ \text{Duty Cycle} = \frac{V_{OUT} + V_{DIODE} - V_{IN}}{V_{OUT} + V_{DIODE} - V_{SW}} \]  

(3)

This applies for continuous mode operation.

The equation shown for calculating duty cycle incorporates terms for the FET switch voltage and diode forward voltage. The actual duty cycle measured in operation will also be affected slightly by other power losses in the circuit such as wire losses in the inductor, switching losses, and capacitor ripple current losses from self-heating. Therefore, the actual (effective) duty cycle measured may be slightly higher than calculated to compensate for these power losses. A good approximation for effective duty cycle is:

\[ \text{DC (eff)} = (1 - \text{Efficiency} \times \frac{V_{IN}}{V_{OUT}}) \]

where

- the efficiency can be approximated from the curves provided.  

(4)

Inductance Value

The first question we are usually asked is: “How small can I make the inductor?” (because they are the largest sized component and usually the most costly). The answer is not simple and involves tradeoffs in performance. Larger inductors mean less inductor ripple current, which typically means less output voltage ripple (for a given size of output capacitor). Larger inductors also mean more load power can be delivered because the energy stored during each switching cycle is:

\[ E = \frac{L}{2} \times (I_p)^2 \]

where

- “Ip” is the peak inductor current.  

(5)
An important point to observe is that the LMR64010 will limit its switch current based on peak current. This means that since \( I_p(\text{max}) \) is fixed, increasing \( L \) will increase the maximum amount of power available to the load. Conversely, using too little inductance may limit the amount of load current which can be drawn from the output.

Best performance is usually obtained when the converter is operated in “continuous” mode at the load current range of interest, typically giving better load regulation and less output ripple. Continuous operation is defined as not allowing the inductor current to drop to zero during the cycle. It should be noted that all boost converters shift over to discontinuous operation as the output load is reduced far enough, but a larger inductor stays “continuous” over a wider load current range.

To better understand these tradeoffs, a typical application circuit (5V to 12V boost with a 10 \( \mu \)H inductor) will be analyzed. We will assume:

\[
V_{IN} = 5V, V_{OUT} = 12V, V_{DIODE} = 0.5V, V_{SW} = 0.5V
\]

Since the frequency is 1.6 MHz (nominal), the period is approximately 0.625 \( \mu \)s. The duty cycle will be 62.5\%, which means the ON time of the switch is 0.390 \( \mu \)s. It should be noted that when the switch is ON, the voltage across the inductor is approximately 4.5V.

Using the equation:

\[
V = L \left( \frac{\text{di}}{\text{dt}} \right)
\]  

We can then calculate the \( \frac{\text{di}}{\text{dt}} \) rate of the inductor which is found to be 0.45 A/\( \mu \)s during the ON time. Using these facts, we can then show what the inductor current will look like during operation:

During the 0.390 \( \mu \)s ON time, the inductor current ramps up 0.176A and ramps down an equal amount during the OFF time. This is defined as the inductor “ripple current”. It can also be seen that if the load current drops to about 33 mA, the inductor current will begin touching the zero axis which means it will be in discontinuous mode. A similar analysis can be performed on any boost converter, to make sure the ripple current is reasonable and continuous operation will be maintained at the typical load current values.
**MAXIMUM SWITCH CURRENT**

The maximum FET switch current available before the current limiter cuts in is dependent on duty cycle of the application. This is illustrated in the graphs below which show both the typical and specified values of switch current as a function of effective (actual) duty cycle:

![Switch Current Limit vs Duty Cycle](image)

**CALCULATING LOAD CURRENT**

As shown in the figure which depicts inductor current, the load current is related to the average inductor current by the relation:

\[
I_{LOAD} = I_{IND}(AVG) \times (1 - DC)
\]

where

- "DC" is the duty cycle of the application.  

\[
I_{SW} = I_{IND}(AVG) + \frac{1}{2} (I_{RIPPLE})
\]

Inductor ripple current is dependent on inductance, duty cycle, input voltage and frequency:

\[
I_{RIPPLE} = DC \times (V_{IN} - V_{SW}) / (f \times L)
\]

combining all terms, we can develop an expression which allows the maximum available load current to be calculated:

\[
I_{LOAD(max)} = (1 - DC) \times (I_{SW(max)} \cdot DC (V_{IN} - V_{SW})) \]

\[
= \frac{2IL}{2IL}
\]

**Figure 20. Switch Current Limit vs Duty Cycle**
The equation shown to calculate maximum load current takes into account the losses in the inductor or turn-OFF switching losses of the FET and diode. For actual load current in typical applications, we took bench data for various input and output voltages and displayed the maximum load current available for a typical device in graph form:

![Figure 21. Max. Load Current vs V_IN](image)

**DESIGN PARAMETERS V_{SW} AND I_{SW}**

The value of the FET "ON" voltage (referred to as $V_{SW}$ in the equations) is dependent on load current. A good approximation can be obtained by multiplying the "ON Resistance" of the FET times the average inductor current.

FET on resistance increases at $V_{IN}$ values below 5V, since the internal N-FET has less gate voltage in this input voltage range (see Typical Performance Characteristics curves). Above $V_{IN} = 5V$, the FET gate voltage is internally clamped to 5V.

The maximum peak switch current the device can deliver is dependent on duty cycle. The minimum value is specified to be $> 1A$ at duty cycle below 50%. For higher duty cycles, see Typical Performance Characteristics curves.

**THERMAL CONSIDERATIONS**

At higher duty cycles, the increased ON time of the FET means the maximum output current will be determined by power dissipation within the LMR64010 FET switch. The switch power dissipation from ON-state conduction is calculated by:

$$P_{(SW)} = DC \times I_{IND}(AVE)^2 \times R_{DS(ON)}$$

(11)

There will be some switching losses as well, so some derating needs to be applied when calculating IC power dissipation.
MINIMUM INDUCTANCE

In some applications where the maximum load current is relatively small, it may be advantageous to use the smallest possible inductance value for cost and size savings. The converter will operate in discontinuous mode in such a case.

The minimum inductance should be selected such that the inductor (switch) current peak on each cycle does not reach the 1A current limit maximum. To understand how to do this, an example will be presented.

In the example, minimum switching frequency of 1.15 MHz will be used. This means the maximum cycle period is the reciprocal of the minimum frequency:

$$T_{ON(max)} = \frac{1}{1.15M} = 0.870 \, \mu s$$  \hspace{1cm} (12)

We will assume the input voltage is 5V, $V_{OUT} = 12V$, $V_{SW} = 0.2V$, $V_{DIODE} = 0.3V$. The duty cycle is:

Duty Cycle = 60.3%

Therefore, the maximum switch ON time is 0.524 $\mu s$. An inductor should be selected with enough inductance to prevent the switch current from reaching 1A in the 0.524 $\mu s$ ON time interval (see below):

![Figure 22. Discontinuous Design, 5V–12V Boost](image)

The voltage across the inductor during ON time is 4.8V. Minimum inductance value is found by:

$$V = L \times \frac{dl}{dt}, L = \frac{V}{\frac{dt}{dl}} = 4.8 \times \frac{0.524\mu \text{s}}{1} = 2.5 \, \mu H$$ \hspace{1cm} (13)

In this case, a 2.7 $\mu H$ inductor could be used assuming it provided at least that much inductance up to the 1A current value. This same analysis can be used to find the minimum inductance for any boost application.

When selecting an inductor, make certain that the continuous current rating is high enough to avoid saturation at peak currents. A suitable core type must be used to minimize core (switching) losses, and wire power losses must be considered when selecting the current rating.

SHUTDOWN PIN OPERATION

The device is turned off by pulling the shutdown pin low. If this function is not going to be used, the pin should be tied directly to $V_{IN}$. If the SHDN function will be needed, a pull-up resistor must be used to $V_{IN}$ (approximately 50k–100k$\Omega$ recommended). The SHDN pin must not be left unterminated.
## REVISION HISTORY

### Changes from Revision A (April 2013) to Revision B

<table>
<thead>
<tr>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changed layout of National Data Sheet to TI format</td>
<td>14</td>
</tr>
</tbody>
</table>
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Top-Side Markings</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMR64010XMF/NOPB</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>SF9B</td>
</tr>
<tr>
<td>LMR64010XMFE/NOPB</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>SF9B</td>
</tr>
<tr>
<td>LMR64010XMFX/NOPB</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>SF9B</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. — The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

![Reel Dimensions Diagram](image)

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>Dimension designed to accommodate the component width</td>
</tr>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

![Quadrant Assignments Diagram](image)

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMR64010XMF/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>LMR64010XMFE/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>LMR64010XMFX/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMR64010XMF/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>LMR64010XMFE/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>LMR64010XMFX/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.
Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and/or implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, “Designers”) understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers’ applications and compliance of their applications (and of all TI products used in or for Designers’ applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI’s provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, is intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer’s company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY TECHNOLOGIES, PATENT RIGHTS OR ANY OTHER INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designers may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S. TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.