TLV6700 Micropower, 18-V Window Comparator With 400-mV Reference

1 Features
- Wide Supply Voltage Range: 1.8 V to 18 V
- Adjustable Threshold: Down to 400 mV
- High Threshold Accuracy:
  - 0.5% Max at 25°C
  - 1.0% Max Over Temperature
- Low Quiescent Current: 5.5 µA (Typ)
- Open-Drain Outputs
- Internal Hysteresis: 5.5 mV (Typ)
- Temperature Range: –40°C to 125°C
- Package: Thin SOT-23-6

2 Applications
- Notebook PCs and Tablets
- Smartphones
- Digital Cameras
- Video Game Controllers
- Relays and Circuit Breakers
- Portable Medical Devices
- Door and Window Sensors
- Portable- and Battery-Powered Products

3 Description
The TLV6700 is a high voltage window comparator that operates over a 1.8 V to 18 V range. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V. The TLV6700 can be used as a window comparator or as two independent comparators; the monitored voltage can be set with the use of external resistors.

OUTA is driven low when the voltage at INA+ drops below \(V_{ITP} - V_{HYS}\), and goes high when the voltage returns above the respective threshold \(V_{ITP}\). OUTB is driven low when the voltage at INB– rises above \(V_{ITP}\) and goes high when the voltage drops below the respective threshold \(V_{ITP} - V_{HYS}\). Both comparators in the TLV6700 include built-in hysteresis to reject brief glitches, thereby ensuring stable output operation without false triggering.

The TLV6700 is available in a Thin SOT-23-6 and is specified over the junction temperature range of –40°C to 125°C.

Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV6700</td>
<td>SOT-23 (6)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Block Diagram
Table of Contents

1 Features .......................................................... 1
2 Applications .................................................. 1
3 Description ................................................... 1
4 Revision History .................................................. 2
5 Device Comparison Table ......................................... 2
6 Pin Configuration and Functions .................................. 3
7 Specifications ..................................................... 4
   7.1 Absolute Maximum Ratings .............................. 4
   7.2 ESD Ratings ................................................. 4
   7.3 Recommended Operating Conditions ................... 4
   7.4 Thermal Information ......................................... 4
   7.5 Electrical Characteristics .................................. 5
   7.6 Timing Requirements ....................................... 6
   7.7 Switching Characteristics .................................. 6
   7.8 Typical Characteristics ..................................... 7
8 Detailed Description .............................................. 9
   8.1 Overview ..................................................... 9
   8.2 Functional Block Diagram.................................. 9
   8.3 Feature Description ........................................... 9
   8.4 Device Functional Modes .................................... 11
9 Application and Implementation ................................ 12
   9.1 Application Information ...................................... 12
   9.2 Typical Application ......................................... 15
   9.3 Do's and Don'ts ............................................... 17
10 Power Supply Recommendations .................................. 18
11 Layout .......................................................... 18
   11.1 Layout Guidelines ........................................... 18
   11.2 Layout Example .............................................. 19
12 Device and Documentation Support ............................. 20
   12.1 Device Support ............................................... 20
   12.2 Receiving Notification of Documentation Updates ........... 20
   12.3 Community Resources ...................................... 20
   12.4 Trademarks .................................................. 20
   12.5 Electrostatic Discharge Caution ......................... 20
   12.6 Glossary .................................................... 20
13 Mechanical, Packaging, and Orderable Information ........... 20
4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2018) to Revision A

• Changed Advance Information to Production Data release .......................................................... 1

5 Device Comparison Table

Table 1. TLV67xx Integrated Comparator Family

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>CONFIGURATION</th>
<th>OPERATING VOLTAGE RANGE</th>
<th>THRESHOLD ACCURACY OVER TEMPERATURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV6700</td>
<td>Window</td>
<td>1.8 V to 18 V</td>
<td>1%</td>
</tr>
<tr>
<td>TLV6703</td>
<td>Non-Inverting Single Channel</td>
<td>1.8 V to 18 V</td>
<td>1%</td>
</tr>
<tr>
<td>TLV6710</td>
<td>Window</td>
<td>1.8 V to 36 V</td>
<td>0.75%</td>
</tr>
<tr>
<td>TLV6713</td>
<td>Non-Inverting Single Channel</td>
<td>1.8 V to 36 V</td>
<td>0.75%</td>
</tr>
</tbody>
</table>
6 Pin Configuration and Functions

![DDC Package SOT-23-6 Top View](image)

**Pin Functions**

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>2</td>
<td>Ground</td>
</tr>
<tr>
<td>INA+</td>
<td>3</td>
<td>I</td>
</tr>
<tr>
<td>INB–</td>
<td>4</td>
<td>I</td>
</tr>
<tr>
<td>OUTA</td>
<td>1</td>
<td>O</td>
</tr>
<tr>
<td>OUTB</td>
<td>6</td>
<td>O</td>
</tr>
<tr>
<td>VDD</td>
<td>5</td>
<td>I</td>
</tr>
</tbody>
</table>

**Description**

- **GND**: Ground
- **INA+**: This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage ($V_{ITH}$), OUTA is driven low.
- **INB–**: This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal exceeds the threshold voltage ($V_{ITH}$), OUTB is driven low.
- **OUTA**: INA+ comparator open-drain output. OUTA is driven low when the voltage at this comparator is below ($V_{ITH} - V_{HYS}$). The output goes high when the sense voltage returns above the respective threshold ($V_{ITH}$).
- **OUTB**: INB– comparator open-drain output. OUTB is driven low when the voltage at this comparator exceeds $V_{ITH}$. The output goes high when the sense voltage returns below the respective threshold ($V_{ITH} - V_{HYS}$).
- **VDD**: Supply voltage input. Connect a 1.8-V to 18-V supply to VDD to power the device. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin.
7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Voltage(^{(2)})</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{DD})</td>
<td>–0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>OUTA, OUTB</td>
<td>–0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>INA+, INB–</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Current</td>
<td>40</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Operating junction temperature, T(_J)</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, T(_stg)</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(^{(1)})</td>
<td>±2500</td>
<td>V</td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(^{(2)})</td>
<td>±1000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Voltage</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{DD})</td>
<td>1.8</td>
<td>18</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V(_i)</td>
<td>0</td>
<td>6.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V(_O)</td>
<td>0</td>
<td>18</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>TLY6700</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDC (SOT)</td>
<td>UNIT</td>
</tr>
<tr>
<td>6 PINS</td>
<td></td>
</tr>
<tr>
<td>R(_{ja})</td>
<td>204.6</td>
</tr>
<tr>
<td>R(_{JC}^{(top)})</td>
<td>50.5</td>
</tr>
<tr>
<td>R(_{JB})</td>
<td>54.3</td>
</tr>
<tr>
<td>ψ(_{JT})</td>
<td>0.8</td>
</tr>
<tr>
<td>ψ(_{JB})</td>
<td>52.8</td>
</tr>
<tr>
<td>R(_{JC}^{(bot)})</td>
<td>N/A</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
7.5  Electrical Characteristics

Over the operating temperature range of $T_J = -40^\circ C$ to $125^\circ C$, and $1.8 \text{ V} < V_{\text{DD}} < 18 \text{ V}$, unless otherwise noted. Typical values are at $T_J = 25^\circ C$ and $V_{\text{DD}} = 5 \text{ V}$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{POR}}$</td>
<td>Power-on reset voltage $^{(1)}$ $V_{\text{OL}}$ max = 0.2 \text{ V}, $I_{\text{(OUTA/B)}} = 15 \mu\text{A}$</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{IT+}}$</td>
<td>Positive-going input threshold voltage $V_{\text{DD}} = 1.8 \text{ V}$ and $18 \text{ V}$, $T_J = 25^\circ C$</td>
<td>398</td>
<td>400</td>
<td>402.5</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{DD}} = 1.8 \text{ V}$ and $18 \text{ V}$, $T_J = -40^\circ C$ to $125^\circ C$</td>
<td>396</td>
<td></td>
<td>404</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{IT–}}$</td>
<td>Negative-going input threshold voltage $V_{\text{DD}} = 1.8 \text{ V}$ and $18 \text{ V}$, $T_J = 25^\circ C$</td>
<td>391.6</td>
<td>394.5</td>
<td>397.5</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{DD}} = 1.8 \text{ V}$ and $18 \text{ V}$, $T_J = -40^\circ C$ to $125^\circ C$</td>
<td>387</td>
<td></td>
<td>400</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{hys}}$</td>
<td>Hysteresis voltage ($hys = V_{\text{IT+}} - V_{\text{IT–}}$)</td>
<td>5.5</td>
<td>12</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$I_{\text{(INA+)}}$</td>
<td>Input current (at the INA+ terminal) $V_{\text{DD}} = 1.8 \text{ V}$ and $18 \text{ V}$, $V_I = 6.5 \text{ V}$</td>
<td>–25</td>
<td>1</td>
<td>25</td>
<td>nA</td>
</tr>
<tr>
<td>$I_{\text{(INB–)}}$</td>
<td>Input current (at the INB– terminal) $V_{\text{DD}} = 1.8 \text{ V}$ and $18 \text{ V}$, $V_I = 0.1 \text{ V}$</td>
<td>–15</td>
<td>1</td>
<td>15</td>
<td>nA</td>
</tr>
<tr>
<td>$V_{\text{OL}}$</td>
<td>Low-level output voltage $V_{\text{DD}} = 1.3 \text{ V}$, $I_O = 0.4 \text{ mA}$</td>
<td>250</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{DD}} = 1.8 \text{ V}$, $I_O = 3 \text{ mA}$</td>
<td>250</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{\text{DD}} = 5 \text{ V}$, $I_O = 5 \text{ mA}$</td>
<td>250</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{Iq(OD)}}$</td>
<td>Open-drain output leakage-current $V_{\text{DD}} = 1.8 \text{ V}$ and $18 \text{ V}$, $V_O = V_{\text{DD}}$</td>
<td>300</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{DD}} = 1.8 \text{ V}$, $V_O = 18 \text{ V}$</td>
<td>300</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{DD}}$</td>
<td>Supply current $V_{\text{DD}} = 1.8 \text{ V}$, no load</td>
<td>5.5</td>
<td>11</td>
<td></td>
<td>\mu\text{A}</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{DD}} = 5 \text{ V}$</td>
<td>6</td>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{\text{DD}} = 12 \text{ V}$</td>
<td>6</td>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{\text{DD}} = 18 \text{ V}$</td>
<td>7</td>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Start-up delay $^{(2)}$</td>
<td></td>
<td>150</td>
<td>450</td>
<td></td>
<td>\mu\text{s}</td>
</tr>
<tr>
<td>$UVLO$</td>
<td>Undervoltage lockout $^{(3)}$ $V_{\text{DD}}$ falling</td>
<td>1.3</td>
<td>1.7</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

$^{(1)}$ The lowest supply voltage ($V_{\text{DD}}$) at which output is active: $t_{\text{(VDD)}} > 15 \mu\text{s/V}$. Below $V_{\text{(POR)}}$, the output cannot be determined.

$^{(2)}$ During power on, $V_{\text{DD}}$ must exceed 1.8 V for 450 µs (max) before the output is in a correct state.

$^{(3)}$ When $V_{\text{DD}}$ falls below UVLO, OUTA is driven low and OUTB goes to high impedance. The outputs cannot be determined below $V_{\text{(POR)}}$. 
7.6 Timing Requirements
over operating temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PHL}$</td>
<td>High-to-low propagation delay$^{(1)}$</td>
<td></td>
<td></td>
<td>18</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>$V_{DD} = 5 \text{ V, } 10\text{-mV input overdrive, } R_p = 10 \text{kΩ, } V_{OH} = 0.9 \times V_{DD}, V_{OL} = 400 \text{ mV, see Figure 1}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>Low-to-high propagation delay$^{(1)}$</td>
<td></td>
<td></td>
<td>29</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>$V_{DD} = 5 \text{ V, } 10\text{-mV input overdrive, } R_p = 10 \text{kΩ, } V_{OH} = 0.9 \times V_{DD}, V_{OL} = 400 \text{ mV, see Figure 1}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) High-to-low and low-to-high refers to the transition at the input terminals (INA+ and INB–).

7.7 Switching Characteristics
Over operating temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_r$</td>
<td>Output rise time</td>
<td></td>
<td></td>
<td>2.2</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>$V_{DD} = 5 \text{ V, } 10\text{-mV input overdrive, } R_p = 10 \text{kΩ, } V_{O} = (0.1 \text{ to } 0.9) \times V_{DD}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_f$</td>
<td>Output fall time</td>
<td></td>
<td></td>
<td>0.22</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>$V_{DD} = 5 \text{ V, } 10\text{-mV input overdrive, } R_p = 10 \text{kΩ, } V_{O} = (0.1 \text{ to } 0.9) \times V_{DD}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) $V_{DD}$, $V_{O}$, and $R_p$ are defined for positive going transitions.

Figure 1. Timing Diagram
7.8 Typical Characteristics

at $T_J = 25°C$ and $V_{DD} = 5$ V (unless otherwise noted)

![Figure 2. Supply Current ($I_{DD}$) vs Supply Voltage ($V_{DD}$)](image1)

![Figure 3. Rising Input Threshold Voltage ($V_{IT+}$) vs Temperature](image2)

![Figure 4. Hysteresis ($V_{hys}$) vs Temperature](image3)

![Figure 5. Propagation Delay vs Temperature (High-to-Low Transition at the Inputs)](image4)

![Figure 6. Propagation Delay vs Temperature (Low-to-High Transition at the Inputs)](image5)

![Figure 7. Minimum Pulse Duration vs Threshold Overdrive Voltage](image6)
Typical Characteristics (continued)

at $T_J = 25^\circ C$ and $V_{DD} = 5 \text{ V}$ (unless otherwise noted)

```
Figure 8. Supply Current ($I_{DD}$) vs Output Sink Current

Figure 9. Output Voltage Low ($V_{OL}$) vs Output Sink Current ($-40^\circ C$)

Figure 10. Output Voltage Low ($V_{OL}$) vs Output Sink Current ($0^\circ C$)

Figure 11. Output Voltage Low ($V_{OL}$) vs Output Sink Current ($25^\circ C$)

Figure 12. Output Voltage Low ($V_{OL}$) vs Output Sink Current ($85^\circ C$)

Figure 13. Output Voltage Low ($V_{OL}$) vs Output Sink Current ($125^\circ C$)
```
8 Detailed Description

8.1 Overview

The TLV6700 device combines two comparators for overvoltage and undervoltage detection. The TLV6700 has a wide-supply voltage range (1.8 V to 18 V) with a high-accuracy rising-input threshold of 400 mV (1% over temperature) and built-in hysteresis. The outputs are also rated to 18 V, independent of supply voltage, and can sink up to 40 mA.

The TLV6700 is designed to assert the output signals, as shown in Table 2. Each input terminal can be set to monitor any voltage above 0.4 V using an external resistor divider network. Each input pin has very low input leakage current, allowing the use of large resistor dividers without sacrificing system accuracy. With the use of two input terminals of different polarities, the TLV6700 forms a window comparator. The relationship between the inputs and the outputs is shown in Table 2. Broad voltage thresholds can be supported that allow the device to be used in a wide array of applications.

Table 2. TLV6700 Truth Table

<table>
<thead>
<tr>
<th>CONDITION</th>
<th>OUTPUT</th>
<th>OUTPUT STATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>INA+ &gt; (V_{IT^+})</td>
<td>OUTA high</td>
<td>Output A high impedance</td>
</tr>
<tr>
<td>INA+ &lt; (V_{IT^-})</td>
<td>OUTA low</td>
<td>Output A sinking</td>
</tr>
<tr>
<td>INB− &gt; (V_{IT^+})</td>
<td>OUTB low</td>
<td>Output B sinking</td>
</tr>
<tr>
<td>INB− &lt; (V_{IT^-})</td>
<td>OUTB high</td>
<td>Output B high impedance</td>
</tr>
</tbody>
</table>

8.2 Functional Block Diagram

8.3 Feature Description

8.3.1 Inputs (INA+, INB−)

The TLV6700 device combines two comparators. Each comparator has one external input (inverting and noninverting); the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to the reference voltage (400 mV). Both comparators also have a built-in falling hysteresis that makes the device less sensitive to supply rail noise and ensures stable operation.

The comparator inputs can swing from ground to 6.5 V, regardless of the device supply voltage used. Although not required in most cases, good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the comparator input for extremely noisy applications to reduce sensitivity to transients and layout parasitics.

For comparator A, the corresponding output (OUTA) is driven to logic low when the input INA+ voltage drops below \((V_{IT^+} - V_{hyp})\). When the voltage exceeds \(V_{IT^+}\), the output (OUTA) goes to a high-impedance state; see Figure 1.
Feature Description (continued)

For comparator B, the corresponding output (OUTB) is driven to logic low when the voltage at input INB– exceeds \( V_{IT+} \). When the voltage drops below \( V_{IT+} - V_{hys} \) the output (OUTB) goes to a high-impedance state; see Figure 1. Together, these comparators form a window-detection function as discussed in the *Window Comparator* section.

8.3.2 Outputs (OUTA, OUTB)

In a typical TLV6700 application, the outputs are connected to a GPIO input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]).

The TLV6700 device provides two open-drain outputs (OUTA and OUTB). Pullup resistors must be used to hold these lines high when the output goes to high impedance (not asserted). By connecting pullup resistors to the proper voltage rails, the outputs can be connected to other devices at the correct interface-voltage levels. The TLV6700 outputs can be pulled up to 18 V, independent of the device supply voltage. By using wired-OR logic, OUTA and OUTB can merge into one logic signal that goes low if either outputs are asserted because of a fault condition.

Table 2 and the *Inputs (INA+, INB–)* section describe how the outputs are asserted or deasserted. See Figure 1 for a timing diagram that describes the relationship between threshold voltages and the respective output.

8.3.3 Window Comparator

The inverting and noninverting configuration of the comparators forms a window-comparator detection circuit using a resistor divider network, as illustrated in Figure 14 and Figure 15. The input terminals can monitor any system voltage above 400 mV with the use of a resistor divider network. The INA+ and INB– terminals monitor for undervoltage and overvoltage conditions, respectively.

![Figure 14. Window Comparator Block Diagram](image-url)
8.3.4 Immunity to Input Terminal Voltage Transients

The TLV6700 device is relatively immune to short voltage transient spikes on the input terminals. Sensitivity to transients depends on both transient duration and amplitude; see the Minimum Pulse Duration vs Threshold Overdrive Voltage curve (Figure 7) in the Typical Characteristics section.

8.4 Device Functional Modes

8.4.1 Normal Operation (\(V_{DD} > \text{UVLO}\))

When the voltage on \(V_{DD}\) is greater than 1.8 V for at least 150 µs, the OUTA and OUTB signals correspond to the voltage on INA+ and INB– as listed in Table 2.

8.4.2 Undervoltage Lockout (\(V_{(POR)} < V_{DD} < \text{UVLO}\))

When the voltage on \(V_{DD}\) is less than the device UVLO voltage, and greater than the power-on reset voltage, \(V_{(POR)}\), the OUTA and OUTB signals are asserted and high impedance, respectively, regardless of the voltage on INA+ and INB–.

8.4.3 Power-On Reset (\(V_{DD} < V_{(POR)}\))

When the voltage on \(V_{DD}\) is lower than the required voltage to internally pull the asserted output to GND (\(V_{(POR)}\)), both outputs are in a high-impedance state.
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV6700 device is a wide-supply voltage window comparator that operates over a $V_{DD}$ range of 1.8 V to 18 V. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for overvoltage and undervoltage detection. The device can be used either as a window comparator or as two independent voltage monitors. The monitored voltages are set with the use of external resistors.

9.1.1 $V_{PULLUP}$ to a Voltage Other Than $V_{DD}$

The outputs are often tied to $V_{DD}$ through a resistor. However, some applications may require the outputs to be pulled up to a higher or lower voltage than $V_{DD}$ to correctly interface with the input terminals of other devices.

![Figure 16. Interfacing to Voltages Other Than $V_{DD}$](image-url)
Application Information (continued)

9.1.2 Monitoring $V_{DD}$
Many applications monitor the same rail that is powering $V_{DD}$. In these applications the resistor divider is simply connected to the $V_{DD}$ rail.

![Figure 17. Monitoring the Same Voltage as $V_{DD}$](image)

9.1.3 Monitoring a Voltage Other Than $V_{DD}$
Some applications monitor rails other than the one that is powering $V_{DD}$. In these types of applications the resistor divider used to set the desired thresholds is connected to the rail that is being monitored.
Application Information (continued)

NOTE: The inputs can monitor a voltage higher than $V_{DD \max}$ with the use of an external resistor divider network.

Figure 18. Monitoring a Voltage Other Than $V_{DD}$
9.2 Typical Application

The TLV6700 device is a wide-supply voltage window comparator that operates over a $V_{DD}$ range of 1.8 to 18 V. The monitored voltages are set with the use of external resistors, so the device can be used either as a window comparator or as two independent overvoltage and undervoltage monitors.

![Figure 19. Typical Application Schematic](image)

9.2.1 Design Requirements

For this design example, use the values summarized in Table 3 as the input parameters.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>DESIGN REQUIREMENT</th>
<th>DESIGN RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Monitored voltage</td>
<td>12-V nominal rail with maximum rising and falling thresholds of ±10%</td>
<td>$V_{MON(UV)} = 10.99$ V $(8.33%) \pm 2.94%$, $V_{MON(OV)} = 13.14$ V $(8.33%) \pm 2.94%$</td>
</tr>
</tbody>
</table>

9.2.2 Detailed Design Procedure

9.2.2.1 Resistor Divider Selection

Use Equation 1 through Equation 4 to calculate the resistor divider values and target threshold voltages.

$$R_T = R_1 + R_2 + R_3$$

Select a value for $R_T$ such that the current through the divider is approximately 100 times higher than the input current at the INA+ and INB– terminals. The resistors can have high values to minimize current consumption as a result of low-input bias current without adding significant error to the resistive divider. See the application note Optimizing Resistor Dividers at a Comparator Input (SLVA450) for details on sizing input resistors.

Use Equation 2 to calculate the value of $R_3$.

$$R_3 = \frac{R_T}{V_{MON(OV)}} \times V_{IT+}$$

where:

$V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected

$$V_{MON(OV)} = 10.99$ V $(8.33\%) \pm 2.94\%$, $V_{MON(OV)} = 13.14$ V $(8.33\%) \pm 2.94\%$$
Use Equation 3 or Equation 4 to calculate the value of $R_2$.

$$R_2 = \left[ \frac{R_T}{V_{\text{MON (no UV)}}} \times V_{\text{IT+}} \right] - R_3$$

where:

$V_{\text{MON (no UV)}}$ is the target voltage at which an undervoltage condition is removed as $V_{\text{MON}}$ rises

$$R_2 = \left[ \frac{R_T}{V_{\text{MON (UV)}}} \times (V_{\text{IT+}} - V_{\text{sys}}) \right] - R_3$$

where:

$V_{\text{MON (UV)}}$ is the target voltage at which an undervoltage condition is detected

The worst-case tolerance can be calculated by referring to Equation 13 in application report SLVA450, Optimizing Resistor Dividers at a Comparator Input (available for download at www.ti.com). An example of the rising threshold error, $V_{\text{MON (OV)}}$, is given in Equation 5.

$$\% \text{ ACC} = \% \text{ TOL}(V_{\text{IT+ (INB)}}) + 2 \times \left[ 1 - \frac{V_{\text{IT+ (INB)}}}{V_{\text{MON (OV)}}} \right] \times \% \text{ TOL}_R = 1\% + 2 \times \left[ 1 - \frac{0.4}{13.2} \right] \times 1\% = 2.94\%$$

### 9.2.2.2 Pullup Resistor Selection

To ensure proper voltage levels, the pullup resistor value is selected by ensuring that the pullup voltage divided by the resistor does not exceed the sink-current capability of the device. This confirmation is calculated by verifying that the pullup voltage minus the output-leakage current ($I_{\text{Ikg(OD)}}$) multiplied by the resistor is greater than the desired logic-high voltage. These values are specified in the Electrical Characteristics table.

Use Equation 6 to calculate the value of the pullup resistor.

$$\frac{(V_{\text{HI}} - V_{\text{PU}})}{I_{\text{Ikg(OD)}}} \geq R_{\text{PU}} \geq \frac{V_{\text{PU}}}{T_O}$$

### 9.2.2.3 Input Supply Capacitor

Although an input capacitor is not required for stability, connecting a 0.1-μF low equivalent series resistance (ESR) capacitor across the $V_{\text{DD}}$ terminal and GND terminal is good analog design practice. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

### 9.2.2.4 Input Capacitors

Although not required in most cases, for extremely noisy applications, placing a 1-nF to 10-nF bypass capacitor from the comparator inputs (INA+, INB−) to the GND terminal is good analog design practice. This capacitor placement reduces device sensitivity to transients.
9.2.3 Application Curves

At $T_J = 25^\circ C$

![Figure 20. Start-Up Delay (Outputs Pulled Up to $V_{DD}$)](image)

![Figure 21. Start-Up Delay (Outputs Pulled Up to $V_{DD}$)](image)

9.3 Do's and Don'ts

It is good analog design practice to have a 0.1-µF decoupling capacitor from $V_{DD}$ to GND.

If the monitored rail is noisy, connect decoupling capacitors from the comparator inputs to GND.

Do not use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparators without also accounting for the effect to the accuracy.

Do not use pullup resistors that are too small, because the larger current sunk by the output then exceeds the desired low-level output voltage ($V_{OL}$).
10 Power Supply Recommendations

The TLV6700 has a 20 V absolute maximum rating on the VDD pin, with a recommended operating condition of 18 V. If the voltage supply that is providing power to VDD is susceptible to any large voltage transient that may exceed 20 V, or if the supply exhibits high voltage slew rates greater than 1 V/µs, take additional precautions. Place an RC filter between the supply and VDD to filter any high-frequency transient surges on the VDD pin. A 100-Ω resistor and 0.01-µF capacitor is required in these cases, as shown in Figure 22.

![Figure 22. Using an RC Filter to Remove High-Frequency Disturbances on VDD](image)

11 Layout

11.1 Layout Guidelines

Placing a 0.1-µF capacitor close to the VDD terminal to reduce the input impedance to the device is good analog design practice. The pullup resistors can be separated if separate logic functions are needed (as shown in Figure 23) or both resistors can be tied to a single pullup resistor if a logical AND function is desired.
11.2 Layout Example

Figure 23. TLV6700 Layout Schematic
12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support
The DIP Adapter Evaluation Module allows conversion of the SOT-23-6 package to a standard DIP-6 pinout for ease of prototyping and bench evaluation.

12.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV6700DDCR</td>
<td>ACTIVE</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>1I51</td>
<td></td>
</tr>
<tr>
<td>TLV6700DDCT</td>
<td>ACTIVE</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>1I51</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

** OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines “RoHS” to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, “RoHS” products are suitable for use in specified lead-free processes. TI may reference these types of products as “Pb-Free”.

**RoHS Exempt:** TI defines “RoHS Exempt” to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines “Green” to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI’s liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
**TAPE AND REEL INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV6700DDCR</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TLV6700DDCT</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>250</td>
<td>180.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Q1**: Pocket Quadrant 1
- **Q2**: Pocket Quadrant 2
- **Q3**: Pocket Quadrant 3
- **Q4**: Pocket Quadrant 4

*Dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV6700DDCR</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>3000</td>
<td>195.0</td>
<td>200.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TLV6700DDCT</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>250</td>
<td>195.0</td>
<td>200.0</td>
<td>45.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7. Board assembly site may have different recommendations for stencil design.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated