ADC081S101-MIL Single-Channel, 0.5 to 1-Msps, 8-Bit A/D Converter

1 Features

- Specified Over a Range of Sample Rates
- 6-Lead WSON and SOT-23 Packages
- Variable Power Management
- Single Power Supply with 2.7-V - 5.25-V Range
- SPI™/QSPI™/MICROWIRE/DSP Compatible
- DNL ± 0.07 LSB (typ)
- INL ± 0.05 LSB (typ)
- SNR 49.7 dB (typ)
- Power Consumption
  - 3-V Supply 2.0 mW (typ)
  - 5-V Supply 10.0 mW (typ)

2 Applications

- Portable Systems
- Remote Data Acquisitions
- Instrumentation and Control Systems

3 Description

The ADC081S101-MIL is a low-power, single channel CMOS 8-bit analog-to-digital converter with a high-speed serial interface. Unlike the conventional practice of specifying performance at a single sample rate only, the ADC081S101-MIL is fully specified over a sample rate range of 500 ksps to 1 Msps. The converter is based upon a successive-approximation register architecture with an internal track-and-hold circuit.

The output serial data is straight binary, and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and many common DSP serial interfaces.

The ADC081S101-MIL operates with a single supply that can range from 2.7 V to 5.25 V. Normal power consumption using a +3 V or +5 V supply is 2.0 mW and 10.0 mW, respectively. The power-down feature reduces the power consumption to just 2.5 µW using a +5 V supply.

The ADC081S101-MIL is packaged in an 6-lead WSON and SOT-23 packages. Operation over the industrial temperature range of −40°C to +85°C is ensured.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC081S101-MIL	SOT-23 (6 DBV)	2.90 x 1.60 mm
	WSON (6 NGF)	2.50 x 2.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram

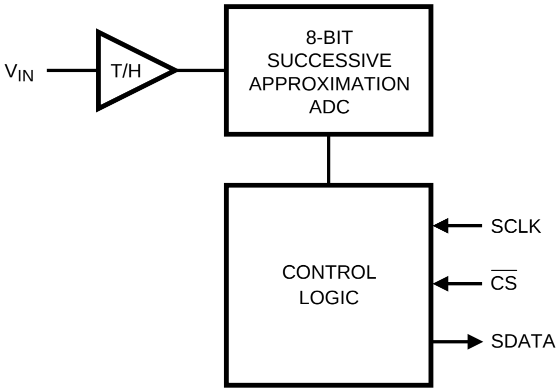


Table of Contents

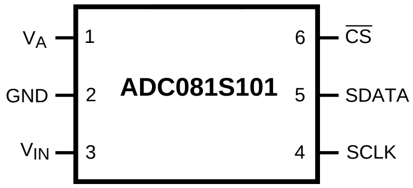
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2017	*	Initial release.

5 Pin Configuration and Functions

DBV or NGF Package
6-Lead SOT-23 or WSON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
ANALOG I/O			
3	V_{IN}	I	Analog input. This signal can range from 0 V to V_A.
DIGITAL I/O			
4	SCLK	I	Digital clock input. This clock directly controls the conversion and readout processes.
5	SDATA	O	Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
6	$\overline{CS}$	I	Chip select. On the falling edge of $\overline{CS}$, a conversion process begins.
POWER SUPPLY			
1	V_A	P	Positive supply pin. This pin should be connected to a quiet +2.7-V to +5.25-V source and bypassed to GND with a 1-µF capacitor and a 0.1-µF monolithic capacitor located within 1 cm of the power pin.
2	GND	G	The ground return for the supply and signals.
PAD	GND	G	For package suffix CISD(X) only, it is recommended that the center pad should be connected to ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
Analog supply voltage, V_A	–0.3	6.5	V
Voltage on any analog pin to GND	–0.3	$V_A + 0.3$	V
Input current at any pin(4)		±10	mA
Package input current(4)		±20	mA
Power consumption at $T_A = 25°C$	See(5)		
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the TI Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supply (that is, V_{IN} < GND or $V_{IN} > V_A$), the current at that pin must be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two. These specifications do not apply to the V_A pin. The current into the V_A pin is limited by the analog supply voltage specification.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_DMAX = (T_Jmax - T_A) / \theta_{JA}$. The values for maximum power dissipation listed above is reached only when the device is operated in a severe fault condition (that is, when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions must always be avoided.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±3500	V
		Machine model (MM)	±300	

(1) Human body model is 100-pF capacitor discharged through a 1.5-kΩ resistor. Machine model is 220 pF discharged through 0 Ω.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_A	Supply voltage	2.7	5.25	V
	Digital input pins voltage (regardless of supply voltage)	–0.3	5.25	V
	Analog input pins voltage	0	V_A	V
	Clock frequency	25	20000	kHz
	Sample rate		1	Msps
T_A	Operating temperature	–40	85	°C

(1) All voltages are measured with respect to GND = 0 V, unless otherwise specified.

6.4 Thermal Information

THERMAL METRIC[1]		ADC081S021		UNIT
		DBV (SOT-23)	NGF (WSON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	184.5	99.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	151.2	118.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.7	68.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.8	6.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.1	69.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	14.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

The following specifications apply for V_A = 2.7 V to 5.25 V, GND = 0V, f_{SCLK} = 10 MHz to 20 MHz, C_L = 15 pF f_{SAMPLE} = 500 ksps to 1 Msps, and T_A = 25°C, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP	MAX(2)	UNIT
STATIC CONVERTER CHARACTERISTICS						
	Resolution with no missing codes				8	Bits
INL	Integral non-linearity	T_A = 25°C		±0.05		LSB
		$T_A = T_{MIN}$ to T_{MAX}			±0.3	
DNL	Differential non-linearity	T_A = 25°C		±0.07		LSB
		$T_A = T_{MIN}$ to T_{MAX}			±0.3	
V_{OFF}	Offset error	T_A = 25°C		±0.03		LSB
		$T_A = T_{MIN}$ to T_{MAX}			±0.3	
GE	Gain error	T_A = 25°C		±0.08		LSB
		$T_A = T_{MIN}$ to T_{MAX}			±0.4	LSB
TUE	Total unadjusted error	T_A = 25°C		±0.07		LSB
		$T_A = T_{MIN}$ to T_{MAX}			±0.3	
DYNAMIC CONVERTER CHARACTERISTICS						
SINAD	Signal-to-noise plus distortion ratio	V_A = 2.7 V to 5.25 V, f_{IN} = 100 kHz, –0.02 dBFS		49.7		dB
		$T_A = T_{MIN}$ to T_{MAX}	49			
SNR	Signal-to-noise ratio	V_A = 2.7 V to 5.25 V, f_{IN} = 100 kHz, –0.02 dBFS		49.7		dB
THD	Total harmonic distortion	V_A = 2.7 V to 5.25 V, f_{IN} = 100 kHz, –0.02 dBFS		–77		dB
		$T_A = T_{MIN}$ to T_{MAX}			–65	
SFDR	Spurious-free dynamic range	V_A = 2.7 V to 5.25 V, f_{IN} = 100 kHz, –0.02 dBFS		68		dB
		$T_A = T_{MIN}$ to T_{MAX}	65			
ENOB	Effective number of bits	V_A = 2.7 V to 5.25 V, f_{IN} = 100 kHz, –0.02 dBFS		7.9		Bits
		$T_A = T_{MIN}$ to T_{MAX}	7.8			
IMD	Intermodulation distortion, second order terms	V_A = 5.25 V, f_a = 103.5 kHz, f_b = 113.5 kHz		–68		dB
	Intermodulation distortion, third order terms	V_A = 5.25 V, f_a = 103.5 kHz, f_b = 113.5 kHz		–68		dB
FPBW	–3 dB full power bandwidth	V_A = 5 V		11		MHz
		V_A = 3 V		8		MHz

(1) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(2) Data sheet minimum and maximum specification limits are specified by design, test, or statistical analysis.

Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.25 V, GND = 0V, f_{SCLK} = 10 MHz to 20 MHz, C_L = 15 pF f_{SAMPLE} = 500 ksps to 1 Msps, and T_A = 25°C, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP	MAX (2)	UNIT
ANALOG INPUT CHARACTERISTICS						
V_{IN}	Input range			0 to V_A		V
I_{DCL}	DC leakage current	$T_A = T_{MIN}$ to T_{MAX}			±1	µA
C_{INA}	Input capacitance	Track mode		30		pF
		Hold mode		4		pF
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Input high voltage	V_A = 5.25 V, $T_A = T_{MIN}$ to T_{MAX}	2.4			V
		V_A = 3.6 V, $T_A = T_{MIN}$ to T_{MAX}	2.1			V
V_{IL}	Input low voltage	V_A = 5 V, $T_A = T_{MIN}$ to T_{MAX}			0.8	V
		V_A = 3 V, $T_A = T_{MIN}$ to T_{MAX}			0.4	V
I_{IN}	Input current	V_{IN} = 0 V or V_A		±10		nA
		V_{IN} = 0 V or $V_{A,}$ $T_A = T_{MIN}$ to T_{MAX}			±1	µA
C_{IND}	Digital input capacitance			2		pF
		$T_A = T_{MIN}$ to T_{MAX}			4	
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output high voltage	I_{SOURCE} = 200 µA		V_A – 0.07		V
		I_{SOURCE} = 200 µA, $T_A = T_{MIN}$ to T_{MAX}	V_A – 0.2			
		I_{SOURCE} = 1 mA		V_A – 0.1		V
V_{OL}	Output low voltage	I_{SINK} = 200 µA		0.03		V
		I_{SINK} = 200 µA, $T_A = T_{MIN}$ to T_{MAX}			0.4	
		I_{SINK} = 1 mA		0.1		V
I_{OZH}, I_{OZL}	TRI-STATE leakage current			±0.1		µA
		$T_A = T_{MIN}$ to T_{MAX}			±10	
C_{OUT}	TRI-STATE output capacitance			2		pF
		$T_A = T_{MIN}$ to T_{MAX}			4	
	Output coding		Straight (natural) binary			
POWER SUPPLY CHARACTERISTICS						
V_A	Supply voltage	$T_A = T_{MIN}$ to T_{MAX}	2.7		5.25	V
I_A	Supply current, normal mode (operational, $\overline{CS}$ low)	V_A = 5.25 V, f_{SAMPLE} = 1 k\Msps, SOT-23 and WSON		2.0		mA
		V_A = 5.25 V, f_{SAMPLE} = 1 k\Msps, $T_A = T_{MIN}$ to T_{MAX}, SOT-23			3.2	
		V_A = 5.25 V, f_{SAMPLE} = 1 k\Msps, $T_A = T_{MIN}$ to T_{MAX}, WSON			2.6	
		V_A = 3.6 V, f_{SAMPLE} = 1 Msps, SOT-23 and WSON		0.6		mA
		V_A = 3.6 V, f_{SAMPLE} = 1 Msps, $T_A = T_{MIN}$ to T_{MAX}, SOT-23			1.5	
		V_A = 3.6 V, f_{SAMPLE} = 1 Msps, $T_A = T_{MIN}$ to T_{MAX}, WSON			1.1	
	Supply current, shutdown ($\overline{CS}$ high)	f_{SCLK} = 0 MHz, V_A = 5.25 V, f_{SAMPLE} = 0 ksps		500		nA
		f_{SCLK} = 20 MHz, V_A = 5.25 V, f_{SAMPLE} = 0 ksps		60		µA

Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.25 V, GND = 0V, f_{SCLK} = 10 MHz to 20 MHz, C_L = 15 pF f_{SAMPLE} = 500 ksps to 1 Msps, and T_A = 25°C, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP	MAX (2)	UNIT
P_D	Power consumption, normal mode (operational, $\overline{CS}$ low)	V_A = 5 V, SOT-23 and WSON		10		mW
		T_A = $T_{MIN}$to T_{MAX}, V_A = 5 V, SOT-23			16	
		T_A = $T_{MIN}$to $T_{MAX}$$V_A$ = 5 V, WSON			13	
		V_A = 3 V, SOT-23 and WSON		2.0		mW
		T_A = $T_{MIN}$to T_{MAX}, V_A = 3 V, SOT-23			4.5	
		T_A = $T_{MIN}$to $T_{MAX}$$V_A$ = 3 V, WSON			3.3	
	Power consumption, shutdown ($\overline{CS}$ high)	f_{SCLK} = 0 MHz, V_A = 5 V, f_{SAMPLE} = 0 ksps		2.5		µW
		f_{SCLK} = 20 MHz, V_A = 5 V, f_{SAMPLE} = 0 ksps		300		µW
AC ELECTRICAL CHARACTERISTICS						
f_{SCLK}	Clock frequency	T_A = $T_{MIN}$to T_{MAX}, See (3)	10		20	MHz
f_S	Sample rate	See (3)		50		ksps
		T_A = $T_{MIN}$to T_{MAX}, See (3)	500			
		T_A = $T_{MIN}$to T_{MAX}			1	Msps
t_{HOLD}	Hold time, falling edges	T_A = $T_{MIN}$to T_{MAX}			13	SCLK
DC	SCLK duty cycle	f_{SCLK} = 20 MHz		50%		
		T_A = $T_{MIN}$to T_{MAX}, f_{SCLK} = 20 MHz	40%		60%	
t_{ACQ}	Minimum time required for acquisition	T_A = $T_{MIN}$to T_{MAX}			350	ns
t_{QUIET}	Quiet time	T_A = $T_{MIN}$to T_{MAX}, See (4)	50			ns
t_{AD}	Aperture delay			3		ns
t_{AJ}	Aperture jitter			30		ps

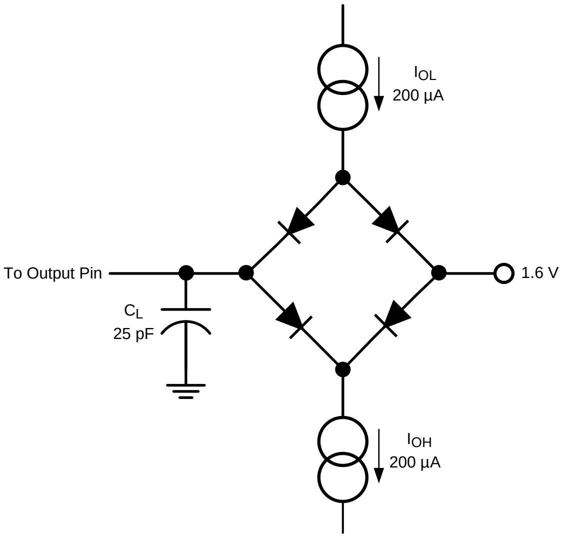
(3) This is the frequency range over which the electrical performance is ensured. The device is functional over a wider range which is specified under Operating Ratings.
(4) Minimum quiet time required by bus relinquish and the start of the next conversion.

6.6 Timing Requirements

The following specifications apply for V_A = 2.7 V to 5.25 V, GND = 0 V, f_{SCLK} = 10.0 MHz to 20.0 MHz, C_L = 25 pF, f_{SAMPLE} = 500 ksps to 1 Msps, and T_A = 25°C (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CS}	Minimum $\overline{CS}$ pulse width	$T_A = T_{MIN}$ to T_{MAX}	10			ns
t_{SU}	$\overline{CS}$ to SCLK setup time	$T_A = T_{MIN}$ to T_{MAX}	10			ns
t_{EN}	Delay from $\overline{CS}$ until SDATA TRI-STATE disabled(2)	$T_A = T_{MIN}$ to T_{MAX}			20	ns
t_{ACC}	Data access time after SCLK falling edge(3)	V_A = 2.7 V to 3.6 V, $T_A = T_{MIN}$ to T_{MAX}			40	ns
		V_A = 4.75 V to 5.25 V, $T_A = T_{MIN}$ to T_{MAX}			20	ns
t_{CL}	SCLK low pulse width	$T_A = T_{MIN}$ to T_{MAX}	0.4 × t_{SCLK}			ns
t_{CH}	SCLK high pulse width	$T_A = T_{MIN}$ to T_{MAX}	0.4 × t_{SCLK}			ns
t_H	SCLK to data valid hold time	V_A = 2.7 V to 3.6 V, $T_A = T_{MIN}$ to T_{MAX}	7			ns
		V_A = 4.75 V to 5.25 V, $T_A = T_{MIN}$ to T_{MAX}	5			ns
t_{DIS}	SCLK falling edge to SDATA high impedance(4)	V_A = 2.7 V to 3.6 V, $T_A = T_{MIN}$ to T_{MAX}	6		25	ns
		V_A = 4.75 V to 5.25 V, $T_A = T_{MIN}$ to T_{MAX}	5		25	ns
$t_{POWER-UP}$	Power-up time from full power down	T_A = 25°C		1		µs

(1) Data sheet minimum and maximum specification limits are specified by design, test, or statistical analysis.
(2) Measured with the timing test circuit and defined as the time taken by the output signal to cross 1 V.
(3) Measured with the timing test circuit and defined as the time taken by the output signal to cross 1 V or 2 V.
(4) t_{DIS} is derived from the time taken by the outputs to change by 0.5 V with the timing test circuit. The measured number is then adjusted to remove the effects of charging or discharging the output capacitance. This means that t_{DIS} is the true bus relinquish time, independent of the bus loading.



Copyright © 2017, Texas Instruments Incorporated

Figure 1. Timing Test Circuit

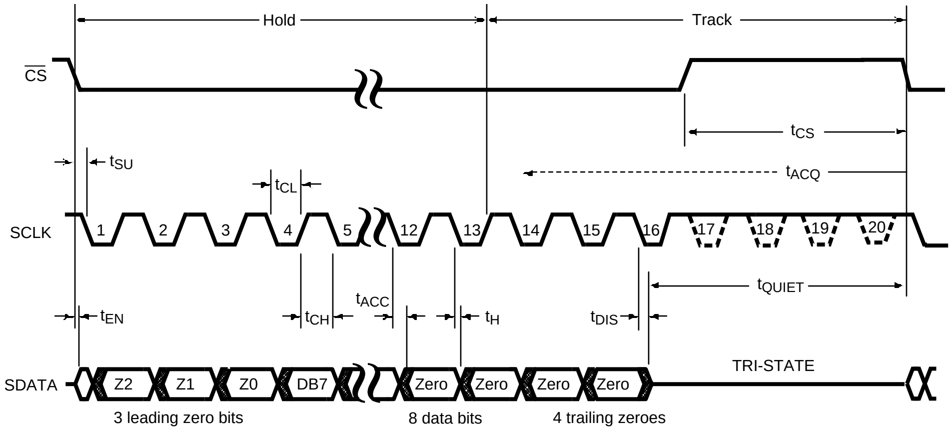


Figure 2. ADC081S101-MIL Serial Timing Diagram

7 Typical Characteristics

T_A = +25°C, f_{SAMPLE} = 500 ksps to 1 Msps, f_{SCLK} = 10 MHz to 20 MHz, f_{IN} = 100 kHz unless otherwise stated.

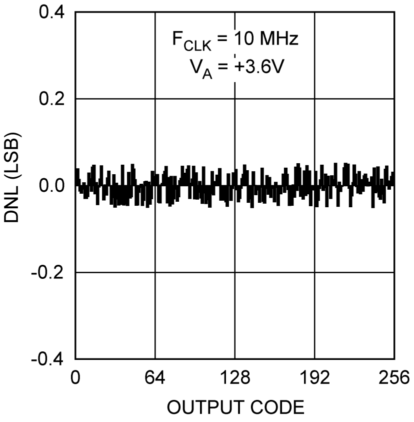


Figure 3. Dnl F_{SCLK} = 10 MHz

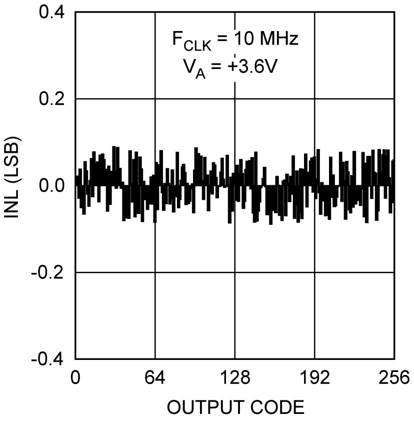


Figure 4. Inl F_{SCLK} = 10 MHz

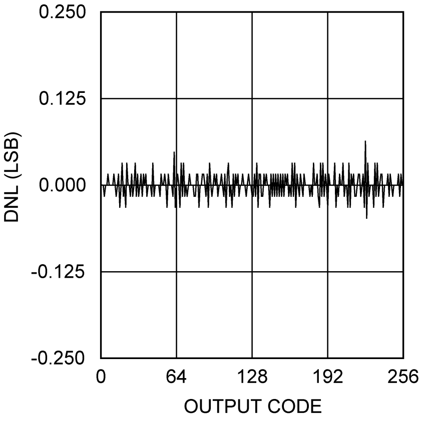


Figure 5. Dnl F_{SCLK} = 20 MHz

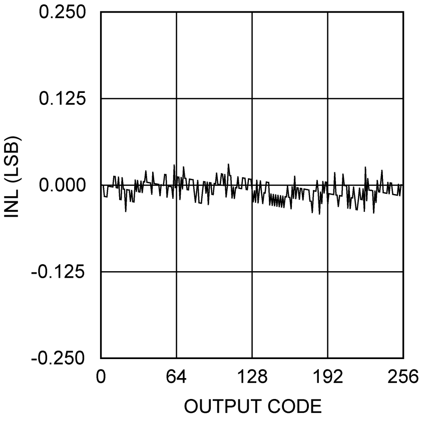


Figure 6. Inl F_{SCLK} = 20 MHz

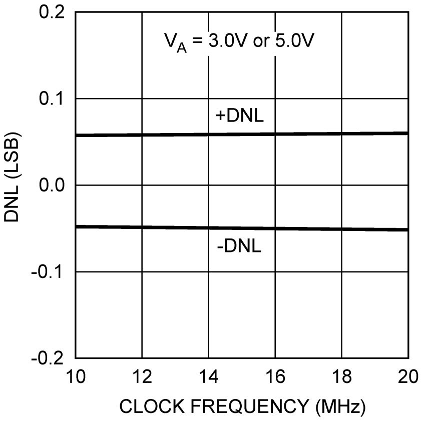


Figure 7. Dnl vs Clock Frequency

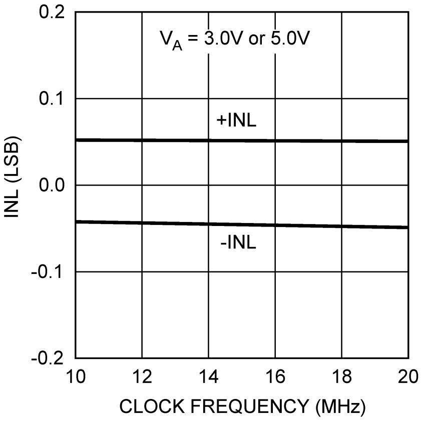


Figure 8. Inl vs Clock Frequency

Typical Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 500 ksps to 1 Msps, f_{SCLK} = 10 MHz to 20 MHz, f_{IN} = 100 kHz unless otherwise stated.

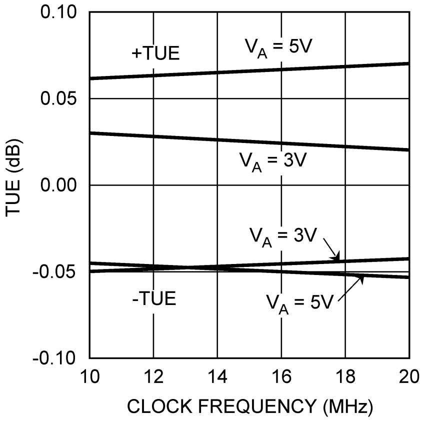


Figure 9. Total Unadjusted Error vs Clock Frequency

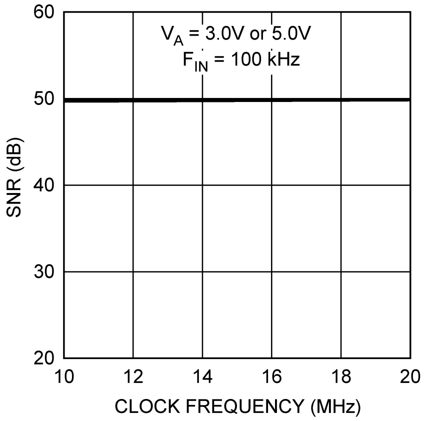


Figure 10. SNR vs Clock Frequency

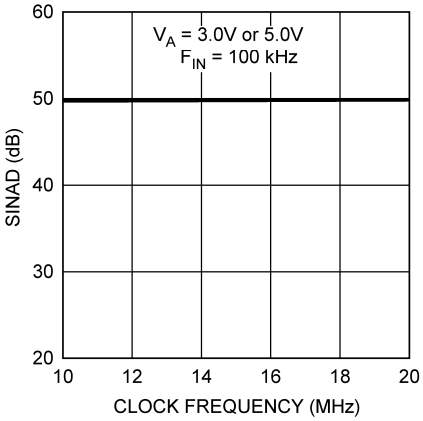


Figure 11. Sinad vs. Clock Frequency

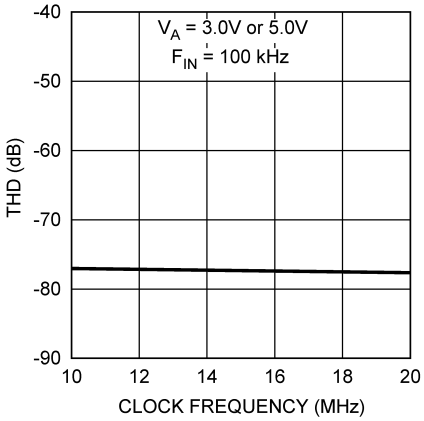


Figure 12. Thd vs. Clock Frequency

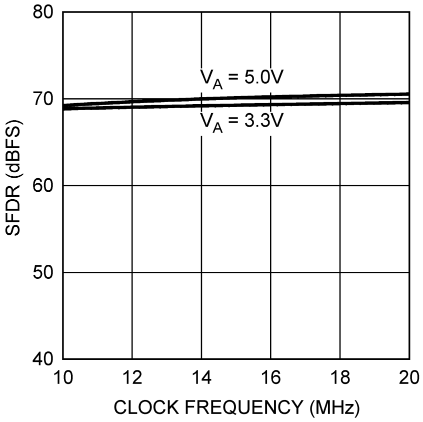


Figure 13. Sfdr vs. Clock Frequency

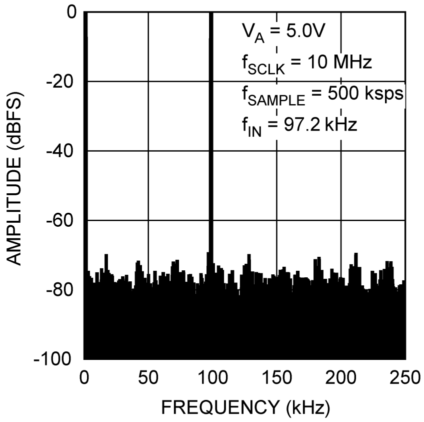


Figure 14. Spectral Response, V_A = 5v F_{SCLK} = 10 MHz

Typical Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 500 ksps to 1 Msps, f_{SCLK} = 10 MHz to 20 MHz, f_{IN} = 100 kHz unless otherwise stated.

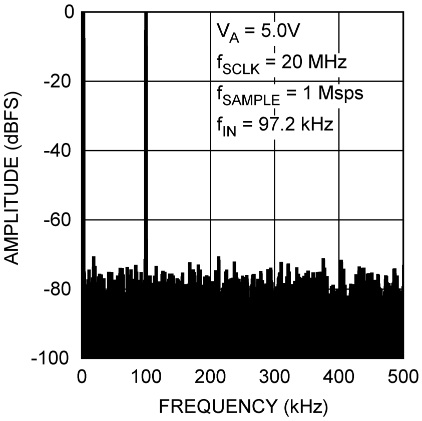


Figure 15. Spectral Response, V_A = 5v F_{SCLK} = 20 MHz

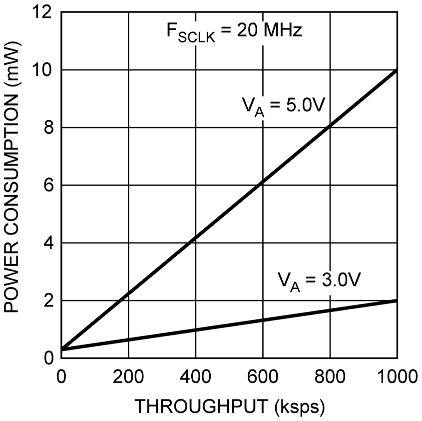


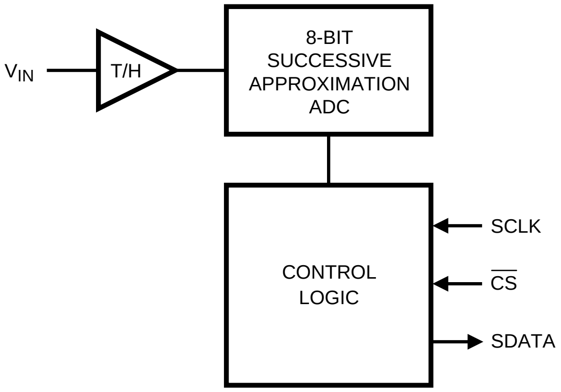
Figure 16. Power Consumption vs. Throughput, F_{SCLK} = 20 MHz

8 Detailed Description

8.1 Overview

The ADC081S101-MIL is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter core. Simplified schematics of the ADC081S101-MIL in both track and hold operation are shown in Figure 17 and Figure 18, respectively. In Figure 17, the device is in track mode: switch SW1 connects the sampling capacitor to the input, and SW2 balances the comparator inputs. The device is in this state until $\overline{CS}$ is brought low, at which point the device moves to hold mode.

8.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

8.3 Feature Description

The serial interface timing diagram for the ADC is shown in Figure 2. $\overline{CS}$ is chip select, which initiates conversions on the ADC and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. SDATA is the serial data out pin, where a conversion result is found as a serial data stream.

Basic operation of the ADC begins with $\overline{CS}$ going low, which initiates a conversion process and data transfer. Subsequent rising and falling edges of SCLK will be labeled with reference to the falling edge of $\overline{CS}$; for example, "the third falling edge of SCLK" shall refer to the third falling edge of SCLK after $\overline{CS}$ goes low.

At the fall of $\overline{CS}$, the SDATA pin comes out of TRI-STATE, and the converter moves from track mode to hold mode. The input signal is sampled and held for conversion on the falling edge of $\overline{CS}$. The converter moves from hold mode to track mode on the 13th rising edge of SCLK (see Figure 2). It is at this point that the interval for the T_{ACQ} specification begins. At least 350ns must pass between the 13th rising edge of SCLK and the next falling edge of $\overline{CS}$. The SDATA pin will be placed back into TRI-STATE after the 16th falling edge of SCLK, or at the rising edge of $\overline{CS}$, whichever occurs first. After a conversion is completed, the quiet time t_{QUIET} must be satisfied before bringing $\overline{CS}$ low again to begin another conversion.

Sixteen SCLK cycles are required to read a complete sample from the ADC. The sample bits (including leading or trailing zeroes) are clocked out on falling edges of SCLK, and are intended to be clocked in by a receiver on subsequent falling edges of SCLK. The ADC will produce three leading zero bits on SDATA, followed by eight data bits, most significant first. After the data bits, the ADC will clock out four trailing zeros.

If $\overline{CS}$ goes low before the rising edge of SCLK, an additional (fourth) zero bit may be captured by the next falling edge of SCLK.

Feature Description (continued)

8.3.1 Determining Throughput

Throughput depends on the frequency of SCLK and how much time is allowed to elapse between the end of one conversion and the start of another. At the maximum specified SCLK frequency, the maximum ensured throughput is obtained by using a 20 SCLK frame. As shown in Figure 2, the minimum allowed time between $\overline{CS}$ falling edges is determined by 1) 12.5 SCLKs for Hold mode, 2) the larger of two quantities: either the minimum required time for Track mode (t_{ACQ}) or 2.5 SCLKs to finish reading the result and 3) 0, 1/2 or 1 SCLK padding to ensure an even number of SCLK cycles so there is a falling SCLK edge when $\overline{CS}$ next falls. For example, at the fastest rate for this family of parts, SCLK is 20MHz and 2.5 SCLKs are 125ns, so the minimum time between $\overline{CS}$ falling edges is calculated by:

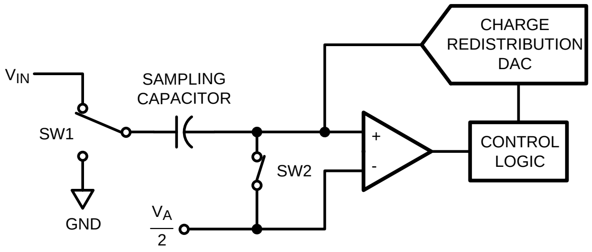
$$12.5*50ns + 350ns + 0.5*50ns = 1000ns \tag{1}$$

(12.5 SCLKs + t_{ACQ} + 1/2 SCLK) which corresponds to a maximum throughput of 1MSPS. At the slowest rate for this family, SCLK is 1MHz. Using a 20-cycle conversion frame as shown in Figure 2 yields a 20µs time between $\overline{CS}$ falling edges for a throughput of 50KSPS.

It is possible, however, to use fewer than 20 clock cycles provided the timing parameters are met. With a 1MHz SCLK, there are 2500ns in 2.5 SCLK cycles, which is greater than t_{ACQ}. After the last data bit has come out, the clock will need one full cycle to return to a falling edge. Thus the total time between falling edges of CS is 12.5*1µs +2.5*1µs +1*1µs=16µs which is a throughput of 62.5KSPS.

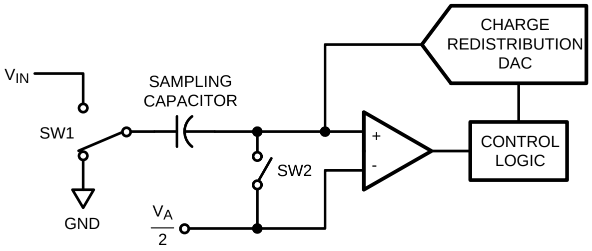
8.4 Device Functional Modes

Figure 18 shows the device in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The device moves from hold mode to track mode on the 13th rising edge of SCLK.



Copyright © 2017, Texas Instruments Incorporated

Figure 17. ADC081S101-MIL In Track Mode



Copyright © 2017, Texas Instruments Incorporated

Figure 18. ADC081S101-MIL In Hold Mode

8.4.1 ADC081S101-MIL Transfer Function

The output format of the ADC is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC is $V_A/256$. The ideal transfer characteristic is shown in Figure 19. The transition from an output code of 0000 0000 to a code of 0000 0001 is at 1/2 LSB, or a voltage of $V_A/512$. Other code transitions occur at steps of one LSB.

Device Functional Modes (continued)

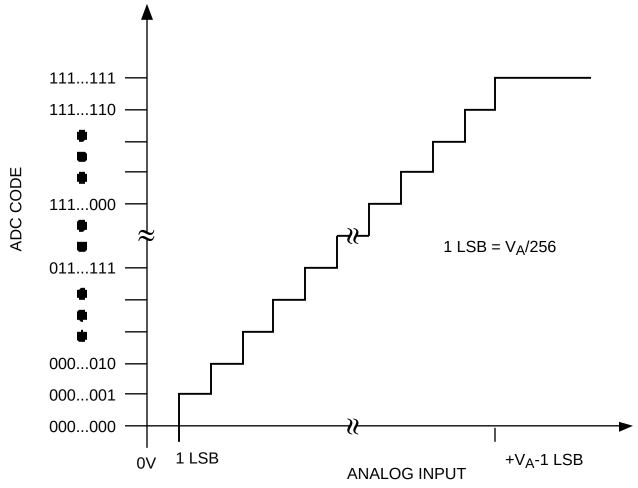


Figure 19. Ideal Transfer Characteristic

8.4.2 Modes Of Operation

The ADC has two possible modes of operation: normal mode, and shutdown mode. The ADC enters normal mode (and a conversion process is begun) when $\overline{\text{CS}}$ is pulled low. The device will enter shutdown mode if $\overline{\text{CS}}$ is pulled high before the tenth falling edge of SCLK after $\overline{\text{CS}}$ is pulled low, or will stay in normal mode if $\overline{\text{CS}}$ remains low. Once in shutdown mode, the device will stay there until $\overline{\text{CS}}$ is brought low again. By varying the ratio of time spent in the normal and shutdown modes, a system may trade-off throughput for power consumption, with a sample rate as low as zero.

8.4.2.1 Normal Mode

The fastest possible throughput is obtained by leaving the ADC in normal mode at all times, so there are no power-up delays. To keep the device in normal mode continuously, $\overline{\text{CS}}$ must be kept low until after the 10th falling edge of SCLK after the start of a conversion (remember that a conversion is initiated by bringing $\overline{\text{CS}}$ low).

If $\overline{\text{CS}}$ is brought high after the 10th falling edge, but before the 16th falling edge, the device will remain in normal mode, but the current conversion will be aborted, and SDATA will return to TRI-STATE (truncating the output word).

Sixteen SCLK cycles are required to read all of a conversion word from the device. After sixteen SCLK cycles have elapsed, $\overline{\text{CS}}$ may be idled either high or low until the next conversion. If $\overline{\text{CS}}$ is idled low, it must be brought high again before the start of the next conversion, which begins when $\overline{\text{CS}}$ is again brought low.

After sixteen SCLK cycles, SDATA returns to TRI-STATE. Another conversion may be started, after t_{QUIET} has elapsed, by bringing $\overline{\text{CS}}$ low again.

8.4.2.2 Shutdown Mode

Shutdown mode is appropriate for applications that either do not sample continuously, or it is acceptable to trade throughput for power consumption. When the ADC is in shutdown mode, all of the analog circuitry is turned off.

To enter shutdown mode, a conversion must be interrupted by bringing $\overline{\text{CS}}$ back high anytime between the second and tenth falling edges of SCLK, as shown in Figure 20. Once $\overline{\text{CS}}$ has been brought high in this manner, the device will enter shutdown mode; the current conversion will be aborted and SDATA will enter TRI-STATE. If $\overline{\text{CS}}$ is brought high before the second falling edge of SCLK, the device will not change mode; this is to avoid accidentally changing mode as a result of noise on the $\overline{\text{CS}}$ line.

Device Functional Modes (continued)

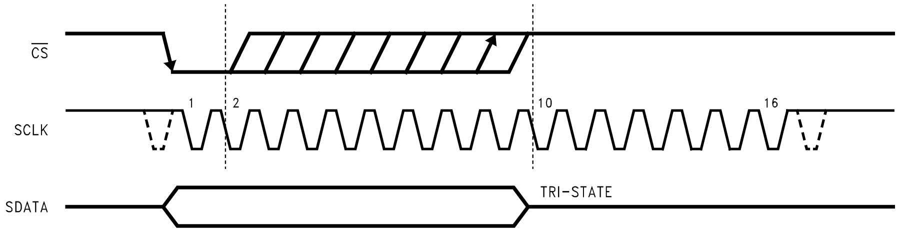


Figure 20. Entering Shutdown Mode

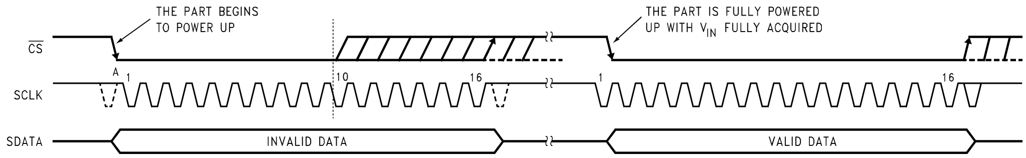


Figure 21. Entering Normal Mode

To exit shutdown mode, bring $\overline{CS}$ back low. Upon bringing $\overline{CS}$ low, the ADC will begin powering up (power-up time is specified in the Timing Requirements). This power-up delay results in the first conversion result being unusable. The second conversion performed after power-up, however, is valid, as shown in Figure 21.

If $\overline{CS}$ is brought back high before the 10th falling edge of SCLK, the device will return to shutdown mode. This is done to avoid accidentally entering normal mode as a result of noise on the $\overline{CS}$ line. To exit shutdown mode and remain in normal mode, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK. The ADC will be fully powered-up after 16 SCLK cycles.

9 Applications Information

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Analog Input

An equivalent circuit for the ADC's input channel is shown in Figure 22. Diodes D1 and D2 provide ESD protection for the analog inputs. At no time should any input go beyond (V_A + 300 mV) or (GND − 300 mV), as these ESD diodes will begin conducting, which could result in erratic operation. For this reason, the ESD diodes should not be used to clamp the input signal.

The capacitor C1 in Figure 22 has a typical value of 4 pF, and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track / hold switch, and is typically 500Ω. Capacitor C2 is the ADC sampling capacitor and is typically 26 pF. The ADC will deliver best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. This is especially important when using the ADC to sample AC signals. Also important when sampling dynamic signals is an anti-aliasing filter.

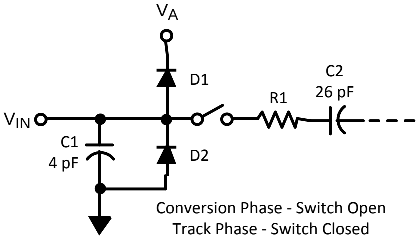


Figure 22. Equivalent Input Circuit

9.1.1 Digital Inputs And Outputs

The ADC digital inputs (SCLK and $\overline{CS}$) are not limited by the same absolute maximum ratings as the analog inputs. The digital input pins are instead limited to +5.25V with respect to GND, regardless of V_A, the supply voltage. This allows the ADC to be interfaced with a wide range of logic levels, independent of the supply voltage.

9.2 Typical Application Circuit

A typical application of the ADC is shown in Figure 23. Power is provided in this example by the TI LP2950 low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The power supply pin is bypassed with a capacitor network located close to the ADC. Because the reference for the ADC is the supply voltage, any noise on the supply will degrade device noise performance. To keep noise off the supply, use a dedicated linear regulator for this device, or provide sufficient decoupling from other circuitry to keep noise off the ADC supply pin. Because of the ADC's low power requirements, it is also possible to use a precision reference as a power supply to maximize performance. The four-wire interface is also shown connected to a microprocessor or DSP.

Typical Application Circuit (continued)

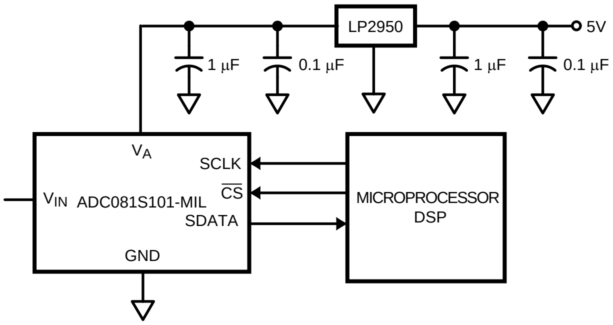


Figure 23. Typical Application Circuit

10 Power Supply Recommendations

The ADC takes time to power-up, either after first applying V_A, or after returning to normal mode from shutdown mode. This corresponds to one "dummy" conversion for any SCLK frequency within the specifications in this document. After this first dummy conversion, the ADC will perform conversions properly. Note that the t_{QUIET} time must still be included between the first dummy conversion and the second valid conversion.

When the V_A supply is first applied, the ADC may power up in either of the two modes: normal or shutdown. As such, one dummy conversion should be performed after start-up, as described in the previous paragraph. The part may then be placed into either normal mode or the shutdown mode, as described in *Normal Mode* and *Shutdown Mode*.

When the ADC is operated continuously in normal mode, the maximum ensured throughput is f_{SCLK} / 20 at the maximum specified f_{SCLK}. Throughput may be traded for power consumption by running f_{SCLK} at its maximum specified rate and performing fewer conversions per unit time, raising the ADC $\overline{CS}$ line after the 10th and before the 15th fall of SCLK of each conversion. A plot of typical power consumption versus throughput is shown in the *Typical Characteristics* section. To calculate the power consumption for a given throughput, multiply the fraction of time spent in the normal mode by the normal mode power consumption and add the fraction of time spent in shutdown mode multiplied by the shutdown mode power consumption. Note that the curve of power consumption vs. throughput is essentially linear. This is because the power consumption in the shutdown mode is so small that it can be ignored for all practical purposes.

10.1 Noise Considerations

The charging of any output load capacitance requires current from the power supply, V_A. The current pulses required from the supply to charge the output capacitance will cause voltage variations on the supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, which is resistive. Load discharge currents will cause "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger the output capacitance, the more current flows through the die substrate and the greater is the noise coupled into the analog channel, degrading noise performance.

To keep noise out of the power supply, keep the output load capacitance as small as practical. It is good practice to use a 100Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and improve noise performance.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

ACQUISITION TIME is the time required to acquire the input voltage. That is, it is time required for the hold capacitor to charge up to the input voltage. Acquisition time is measured backwards from the falling edge of $\overline{CS}$ when the signal is sampled and the part moves from track to hold. The start of the time interval that contains T_{ACQ} is the 13th rising edge of SCLK of the previous conversion when the part moves from hold to track. The user must ensure that the time between the 13th rising edge of SCLK and the falling edge of the next $\overline{CS}$ is not less than T_{ACQ} to meet performance specifications.

APERTURE DELAY is the time after the falling edge of $\overline{CS}$ when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC081S021 to convert the input voltage to a digital word. This is from the falling edge of $\overline{CS}$ when the input signal is sampled to the 16th falling edge of SCLK when the SDATA output goes into TRI-STATE.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC081S021 of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal (V_{REF} − 1 LSB), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC081S021 input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the sum of the power in both of the original frequencies. IMD is usually expressed in dB.

MISSING CODES are those output codes that never appear at the ADC081S021 outputs. The ADC081S021 is ensured not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (that is, GND + 1 LSB).

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of all of the other spectral components below half the clock frequency, including harmonics but excluding DC

Device Support (continued)

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB or dBc, of the RMS total of the first five harmonic components at the output to the RMS level of the input signal frequency as seen at the output. THD is calculated as

$$\mathrm{THD} = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^{2} + \cdots + A_{f6}^{2}}{A_{f1}^{2}}}$$

where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f6} are the RMS power in the first 5 harmonic frequencies.

THROUGHPUT TIME is the minimum time required between the start of two successive conversion. It is the acquisition time plus the conversion time.

TOTAL UNADJUSTED ERROR is the worst deviation found from the ideal transfer function. As such, it is a comprehensive specification which includes full scale error, linearity error, and offset error.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

LP295x-N Series of Adjustable Micropower Voltage Regulators SNVS764

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC081S101 MWC	Active	Production	WAFERSALE (YS) | 0	1 | OTHER	-	Call TI	Level-1-NA-UNLIM	-40 to 85	
ADC081S101-MWC.A	Active	Production	WAFERSALE (YS) | 0	1 | OTHER	-	Call TI	Level-1-NA-UNLIM	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025