**FEATURES**

- **24 BITS—NO MISSING CODES**
- **19 BITS EFFECTIVE RESOLUTION UP TO 40kHz DATA RATE**
- **LOW NOISE: 2.5ppm**
- **DIFFERENTIAL INPUTS**
- **INL: 0.0015% (max)**
- **EXTERNAL REFERENCE (0.5V to 5V)**
- **POWER-DOWN MODE**
- **SYNC MODE**

**APPLICATIONS**

- **CARDIAC DIAGNOSTICS**
- **DIRECT THERMOCOUPLE INTERFACES**
- **BLOOD ANALYSIS**
- **INFRARED PYROMETERS**
- **LIQUID/GAS CHROMATOGRAPHY**
- **PRECISION PROCESS CONTROL**

**DESCRIPTION**

The ADS1252 is a precision, wide dynamic range, delta-sigma, Analog-to-Digital (A/D) converter with 24-bit resolution operating from a single +5V supply. The delta-sigma architecture is used for wide dynamic range and to ensure 24 bits of no missing code performance. An effective resolution of 19 bits (2.5ppm of rms noise) is achieved for conversion rates up to 40kHz.

The ADS1252 is designed for high-resolution measurement applications in cardiac diagnostics, smart transmitters, industrial process control, weight scales, chromatography, and portable instrumentation. The converter includes a flexible, 2-wire synchronous serial interface for low-cost isolation.

The ADS1252 is a single-channel converter and is offered in an SO-8 package.
ABSOLUTE MAXIMUM RATINGS

Analog Input: Current ............................................. ±100mA, Momentary ±10mA, Continuous
Voltage .................................................. GND – 0.3V to VDD + 0.3V
VDD to GND .............................................................. –0.3V to 6V
VREF Voltage to GND .............................................. –0.3V to VDD + 0.3V
Digital Input Voltage to GND .................................... –0.3V to VDD + 0.3V
Digital Output Voltage to GND ................................... –0.3V to VDD + 0.3V
Lead Temperature (soldering, 10s) ...................... +300°C
Power Dissipation (any package) .............................. 500mW

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/OORDERING INFORMATION

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>PACKAGE-LEAD</th>
<th>PACKAGE DESIGNATOR</th>
<th>SPECIFIED TEMPERATURE RANGE</th>
<th>PACKAGE MARKING</th>
<th>ORDERING NUMBER</th>
<th>TRANSPORT MEDIA, QUANTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS1252</td>
<td>SO-8</td>
<td>D</td>
<td>–40°C to +85°C</td>
<td>ADS1252U</td>
<td>Rails, 100</td>
<td>Tape and Reel, 2500</td>
</tr>
</tbody>
</table>

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>PIN DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+VIN</td>
<td>Analog Input: Positive Input of the Differential Analog Input</td>
</tr>
<tr>
<td>2</td>
<td>-VIN</td>
<td>Analog Input: Negative Input of the Differential Analog Input</td>
</tr>
<tr>
<td>3</td>
<td>+VDD</td>
<td>Input: Power-Supply Voltage, +5V</td>
</tr>
<tr>
<td>4</td>
<td>CLK</td>
<td>Digital Input: Device System Clock. The system clock is in the form of a CMOS-compatible clock. This is a Schmitt-Trigger input.</td>
</tr>
<tr>
<td>5</td>
<td>DOUT/DRDY</td>
<td>Digital Output: Serial Data Output/Data Ready. A logic LOW on this output indicates that a new output word is available from the ADS1252 data output register. The serial data is clocked out of the serial data output shift register using SCLK.</td>
</tr>
<tr>
<td>6</td>
<td>SCLK</td>
<td>Digital Input: Serial Clock. The serial clock is in the form of a CMOS-compatible clock. The serial clock operates independently from the system clock, therefore, it is possible to run SCLK at a higher frequency than CLK. The normal state of SCLK is LOW. Holding SCLK HIGH will either initiate a modulator reset for synchronizing multiple converters or enter power-down mode. This is a Schmitt-Trigger input.</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>Input: Ground</td>
</tr>
<tr>
<td>8</td>
<td>VREF</td>
<td>Analog Input: Reference Voltage Input</td>
</tr>
</tbody>
</table>
# ELECTRICAL CHARACTERISTICS

All specifications at $T_{MIN}$ to $T_{MAX}$, $V_{DD} = +5V$, CLK = 16MHz, and $V_{REF} = 4.096V$, unless otherwise specified.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>ADS1252U</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ANALOG INPUT</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full-Scale Input Voltage</td>
<td>0</td>
<td>±$V_{REF}$</td>
<td>V</td>
</tr>
<tr>
<td>Absolute Input Voltage</td>
<td>−0.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Differential Input Impedance</td>
<td>+$V_{IN}$ or −$V_{IN}$ to GND</td>
<td>125</td>
<td>VDD</td>
</tr>
<tr>
<td>CLK = 3.84kHz</td>
<td>480</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>CLK = 1MHz</td>
<td>30</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>CLK = 16MHz</td>
<td>20</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>5</td>
<td>50</td>
<td>pF</td>
</tr>
<tr>
<td>Input Leakage</td>
<td>1</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td><strong>DYNAMIC CHARACTERISTICS</strong></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Data Rate</td>
<td>−3dB</td>
<td>9</td>
<td>41.7</td>
</tr>
<tr>
<td>Bandwidth</td>
<td></td>
<td></td>
<td>16</td>
</tr>
<tr>
<td>Serial Clock (SCLK)</td>
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<td></td>
<td>16</td>
</tr>
<tr>
<td>System Clock Input (CLK)</td>
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<td></td>
<td></td>
</tr>
<tr>
<td><strong>ACCURACY</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Integral Nonlinearity(1)</td>
<td>±0.0003</td>
<td>±0.0015</td>
<td>% of FSR</td>
</tr>
<tr>
<td>THD</td>
<td>1kHz Input; 0.1dB below FS</td>
<td>97</td>
<td>3.8</td>
</tr>
<tr>
<td>Noise</td>
<td>2.5</td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>Resolution</td>
<td>24</td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>No Missing Codes</td>
<td>24</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Common-Mode Rejection(2)</td>
<td>at DC</td>
<td>90</td>
<td>100</td>
</tr>
<tr>
<td>Gain Error</td>
<td>0.4</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Offset Error</td>
<td>±100</td>
<td>±200</td>
<td>ppm of FSR</td>
</tr>
<tr>
<td>Gain Sensitivity to $V_{REF}$</td>
<td>$V_{REF} = 4.096V, ±0.1V$</td>
<td>1:1</td>
<td></td>
</tr>
<tr>
<td>Power-Supply Rejection Ratio</td>
<td>60</td>
<td>80</td>
<td>dB</td>
</tr>
<tr>
<td><strong>PERFORMANCE OVER TEMPERATURE</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Drift</td>
<td></td>
<td></td>
<td>0.07</td>
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<tr>
<td>Gain Drift</td>
<td>CLK = 16MHz</td>
<td>7.5</td>
<td>ppm/°C</td>
</tr>
<tr>
<td>CLK = 14MHz</td>
<td>5.2</td>
<td>ppm/°C</td>
<td></td>
</tr>
<tr>
<td>CLK = 12MHz</td>
<td>3.9</td>
<td>ppm/°C</td>
<td></td>
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<tr>
<td>CLK &lt; 10MHz</td>
<td>3.4</td>
<td>ppm/°C</td>
<td></td>
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<td><strong>VOLTAGE REFERENCE</strong></td>
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<tr>
<td>$V_{REF}$</td>
<td>0.5</td>
<td>4.096</td>
<td></td>
</tr>
<tr>
<td>Load Current</td>
<td>220</td>
<td></td>
<td>VDD</td>
</tr>
<tr>
<td><strong>DIGITAL INPUT/OUTPUT</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Level: $V_{RH}$</td>
<td>+4.0</td>
<td>+$V_{DD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>−0.3</td>
<td>+0.8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>+4.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>ICH = −500μA</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>ICL = 500μA</td>
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</tr>
<tr>
<td>Input (SCLK, CLK) Hysteresis</td>
<td>0.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Format</td>
<td>Offset Binary Two’s Complement</td>
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</tr>
<tr>
<td><strong>POWER-SUPPLY REQUIREMENTS</strong></td>
<td></td>
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</tr>
<tr>
<td>Operation</td>
<td>$V_{DD} = +5VDC$</td>
<td>4.75</td>
<td>5</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td></td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>Operating Power</td>
<td></td>
<td>40</td>
<td>50</td>
</tr>
<tr>
<td>Power-Down Current</td>
<td></td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td><strong>TEMPERATURE RANGE</strong></td>
<td></td>
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</tr>
<tr>
<td>Operating</td>
<td></td>
<td></td>
<td>−40</td>
</tr>
<tr>
<td>Storage</td>
<td></td>
<td></td>
<td>−60</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Applies to full-differential signals.
2. The common-mode rejection test is performed with a 100mV differential input.
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ C$, $V_{DD} = +5$V, CLK = 16MHz, and $V_{REF} = 4.096$V, unless otherwise specified.

RMS NOISE vs DATA OUTPUT RATE

Data Output Rate (Hz)

Data Output Rate (Hz)

RMS NOISE vs TEMPERATURE

Temperature (°C)

Temperature (°C)

RMS NOISE vs $V_{REF}$ VOLTAGE

$V_{REF}$ (V)

$V_{REF}$ (V)

EFFECTIVE RESOLUTION vs DATA OUTPUT RATE

Effective Resolution (bits)

Effective Resolution (bits)
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $CLK = 16MHz$, and $V_{REF} = 4.096V$, unless otherwise specified.

- **RMS Noise vs Input Voltage**
  - **Y-axis:** RMS Noise (ppm of FS)
  - **X-axis:** Differential Input Voltage (V)

- **Effective Resolution vs $V_{REF}$**
  - **Y-axis:** Effective Resolution (Bits)
  - **X-axis:** $V_{REF}$ (V)

- **Integral Non-Linearity vs Temperature**
  - **Y-axis:** INL (ppm of FS)
  - **X-axis:** Temperature (°C)

- **Integral Non-Linearity vs Data Output Rate**
  - **Y-axis:** INL (ppm of FS)
  - **X-axis:** Data Output Rate (Hz)

- **Offset Drift vs Temperature**
  - **Y-axis:** Offset Drift (ppm of FS)
  - **X-axis:** Temperature (°C)

- **Gain Drift vs Temperature**
  - **Y-axis:** Drift (ppm)
  - **X-axis:** Temperature (°C)

- **RMS Noise vs Input Voltage**
  - **Y-axis:** RMS Noise (ppm of FS)
  - **X-axis:** Differential Input Voltage (V)

- **Gain Drift vs Temperature**
  - **Y-axis:** Drift (ppm)
  - **X-axis:** Temperature (°C)
TYPICAL CHARACTERISTICS (Cont.)

At \( T_A = +25^\circ C, V_{DD} = +5V, \) CLK = 16MHz, and \( V_{REF} = 4.096V, \) unless otherwise specified.
THEORY OF OPERATION

The ADS1252 is a precision, high-dynamic range, 24-bit, delta-sigma, A/D converter capable of achieving very high-resolution digital results at high data rates. The analog-input signal is sampled at a rate determined by the frequency of the system clock (CLK). The sampled analog input is modulated by the delta-sigma A/D modulator, which is followed by a digital filter. A Sinc⁵ digital low-pass filter processes the output of the delta-sigma modulator and writes the result into the data-output register. The DOUT/DRDY pin is pulled LOW, indicating that new data is available to be read by the external microcontroller/microprocessor. As shown in the block diagram, the main functional blocks of the ADS1252 are the 4th-order delta-sigma modulator, a digital filter, control logic, and a serial interface. Each of these functional blocks is described below.

ANALOG INPUT

The ADS1252 contains a fully differential analog input. In order to provide low system noise, common-mode rejection of 100dB, and excellent power-supply rejection, the design topology is based on a fully differential switched-capacitor architecture. The bipolar input voltage range is from $-4.096$ to $+4.096\text{V}$, when the reference input voltage equals $+4.096\text{V}$; the bipolar range is with respect to $-V_{IN}$, and not with respect to GND.

With regard to the analog input signal, the overall analog performance of the device is affected by three items. First, the input impedance can affect accuracy; therefore, if the source impedance of the input signal is significant, or if there is passive filtering prior to the ADS1252, a significant portion of the signal can be lost across this external impedance. The magnitude of the effect is dependent on the desired system performance. See application note Understanding the ADS1251, ADS1253, and ADS1254 Input Circuity (SBAA086), available for download from TI’s web site, www.ti.com.

Second, the current into or out of the analog inputs must be limited. Under no conditions should the current into or out of the analog inputs exceed 10mA.

Third, to prevent aliasing of the input signal, the bandwidth of the analog input signal must be band limited; the bandwidth is a function of the system clock frequency. With a system clock frequency of 16MHz, the data-output rate is 41.667kHz with a $-3\text{dB}$ frequency of 9kHz, where the $-3\text{dB}$ frequency scales with the system clock frequency.

To ensure the best linearity of the ADS1252, a fully differential signal is recommended.

BIPOLAR INPUT

The differential inputs of the ADS1252 are designed to accept differential signals; however, each analog input voltage must stay between $-0.3\text{V}$ and $V_{DD}$. With a reference voltage at less than half of $V_{DD}$, one input can be tied to the reference voltage, and the other input can range from 0V to $2\cdot V_{REF}$. By using a single op amp circuit featuring a single amplifier and four external resistors, the ADS1252 can be configured to accept bipolar inputs referenced to ground. The conventional $\pm 2.5\text{V}$, $\pm 5\text{V}$, and $\pm 10\text{V}$ input ranges can be interfaced to the ADS1252 using the resistor values shown in Figure 1.
DELTA-SIGMA MODULATOR
The ADS1252 operates from a nominal system clock frequency of 16MHz which is fixed in relation to the system clock frequency that is divided by 6 to derive the modulator frequency; therefore, with a system clock frequency of 16MHz, the modulator frequency is 2.667MHz. Furthermore, the oversampling ratio of the modulator is fixed in relation to the modulator frequency. The oversampling ratio of the modulator is 64, and with the modulator frequency running at 2.667MHz, the data rate is 41.667kHz; thus, using a slower system clock frequency will result in a lower data output rate, as shown in Table I.

### TABLE I. CLK Rate versus Data Output Rate.

<table>
<thead>
<tr>
<th>CLK (MHz)</th>
<th>DATA OUTPUT RATE (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16.000(1)</td>
<td>41 667</td>
</tr>
<tr>
<td>15.360(1)</td>
<td>40 000</td>
</tr>
<tr>
<td>15.000(1)</td>
<td>30 063</td>
</tr>
<tr>
<td>14.745600(1)</td>
<td>38 400</td>
</tr>
<tr>
<td>14.318180(1)</td>
<td>37 287</td>
</tr>
<tr>
<td>12.288000(1)</td>
<td>32 000</td>
</tr>
<tr>
<td>12.000000(1)</td>
<td>31 250</td>
</tr>
<tr>
<td>11.059220(1)</td>
<td>28 800</td>
</tr>
<tr>
<td>10.000000(1)</td>
<td>26 042</td>
</tr>
<tr>
<td>9.600000</td>
<td>25 000</td>
</tr>
<tr>
<td>7.372800(1)</td>
<td>19 200</td>
</tr>
<tr>
<td>6.144000(1)</td>
<td>16 000</td>
</tr>
<tr>
<td>6.000000(1)</td>
<td>15 625</td>
</tr>
<tr>
<td>4.915200(1)</td>
<td>12 800</td>
</tr>
<tr>
<td>3.686400(1)</td>
<td>9 600</td>
</tr>
<tr>
<td>3.072000(1)</td>
<td>8 000</td>
</tr>
<tr>
<td>2.457600(1)</td>
<td>6 400</td>
</tr>
<tr>
<td>1.843200(1)</td>
<td>4 800</td>
</tr>
<tr>
<td>0.921600(1)</td>
<td>2 400</td>
</tr>
<tr>
<td>0.460800</td>
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<tr>
<td>0.384000</td>
<td>1 000</td>
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<td>0.192000</td>
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<td>0.023040</td>
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<td>0.007680</td>
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<td>0.006400</td>
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<td>15</td>
</tr>
<tr>
<td>0.004800</td>
<td>12.50</td>
</tr>
<tr>
<td>0.003840</td>
<td>10</td>
</tr>
</tbody>
</table>

NOTE: (1) Standard Clock Oscillator.

REFERENCE INPUT
Reference input takes an average current of 220µA with a 16MHz system clock; this current will be proportional to the system clock. A buffered reference is recommended for ADS1252. The recommended reference circuit is shown in Figure 2.

Reference voltages higher than 4.096V will increase the full-scale range, whereas the absolute internal circuit noise of the converter remains the same. This will decrease the noise in terms of ppm of full scale, which increases the effective resolution (see the typical characteristic curve, RMS Noise vs $V_{REF}$).

DIGITAL FILTER
The digital filter of the ADS1252, referred to as a sinc⁵ filter, computes the digital result based on the most recent outputs from the delta-sigma modulator. At the most basic level, the digital filter can be thought of as simply averaging the modulator results in a weighted form and presenting this average as the digital output. The digital output rate, or data rate, scales directly with the system CLK frequency, this allows the data output rate to be changed over a very wide range (five orders of magnitude) by changing the system CLK frequency. However, it is important to note that the –3dB point of the filter is 0.216 times the data output rate, so the data output rate must allow for sufficient margin to prevent attenuation of the signal of interest.

As the conversion result is essentially an average, the data-output rate determines the location of the resulting notches in the digital filter (see Figure 3). Note that the first notch is located at the data-output rate frequency, and subsequent notches are located at integer multiples of the data-output rate to allow for rejection of not only the fundamental frequency, but also harmonic frequencies. In this manner, the data-output rate can be used to set specific notch frequencies in the digital filter response.
For example, if the rejection of power-line frequencies is desired, then the data-output rate can simply be set to the power-line frequency. For 50Hz rejection, the system CLK frequency must be 19.200kHz, and this will set the data-output rate to 50Hz (see Table I and Figure 4). For 60Hz rejection, the system CLK frequency must be 20.040kHz, and this will set the data-output rate to 60Hz (see Table I and Figure 5). If both 50Hz and 60Hz rejection is required, then the system CLK must be 3.840kHz; this will set the data-output rate to 10Hz and reject both 50Hz and 60Hz (see Table I and Figure 6).

There is an additional benefit in using a lower data-output rate: it provides better rejection of signals in the frequency band of interest. For example, with a 50Hz data-output rate, a significant signal at 75Hz can alias back into the passband at 25Hz; this is due to the fact that rejection at 75Hz must only be 66dB in the stopband—frequencies higher than the first-notch frequency (see Figure 4). However, setting the data-output rate to 10Hz will provide 135dB rejection at 75Hz (see Figure 6). A similar benefit is gained at frequencies near the data-output rate (see Figures 7, 8, 9, and 10). For example, with a 50Hz data-output rate, rejection at 55Hz may only be 105dB (see Figure 7); however, with a 10Hz data-output rate, rejection at 55Hz will be 122dB (see Figure 8).

If a slower data-output rate does not meet the system requirements, then the analog front end can be designed to provide the needed attenuation to prevent aliasing. Additionally, the data-output rate can be increased and additional digital filtering can be done in the processor or controller.

Application note SBAA103, A Spreadsheet to Calculate the Frequency Response of the ADS1250-54 (available for download at www.ti.com) provides a simple tool for calculating the ADS1250 frequency response for any CLK frequency.

The digital filter is described by the following transfer function:

$$H(f) = \left(\frac{\sin\left(\frac{\pi f \cdot 64}{\text{MOD}}\right)}{64 \cdot \sin\left(\frac{\pi f}{\text{MOD}}\right)}\right)^5$$

or

$$H(z) = \left(\frac{1 - z^{-64}}{64 \cdot (1 - z^{-1})}\right)^5$$

The digital filter requires five conversions to fully settle. The modulator has an oversampling ratio of 64; therefore, it requires $5 \cdot 64$, or 320 modulator results, or clocks, to fully settle. As the modulator clock is derived from the system clock (CLK) (modulator clock = CLK / 6), the number of system clocks required for the digital filter to fully settle is $5 \cdot 64 \cdot 6$, or 1920 CLKs. This means that any significant step change at the analog input requires five full conversions to settle. However, if the analog input change occurs asynchronously to the DOUT/DRDY pulse, then six conversions are required to ensure full settling.

**CONTROL LOGIC**

The control logic is used for communications and control of the ADS1252.

**Power-Up Sequence**

Prior to power-up, all digital and analog-input pins must be LOW. At the time of power-up, these signal inputs can be biased to a voltage other than 0V, however, they must never exceed $+V_{DD}$.

Once the ADS1252 powers up, the DOUT/DRDY line pulses LOW on the first conversion; this data is not valid. The sixth pulse of DOUT/DRDY is valid data from the analog input signal.

**DOUT/DRDY**

The DOUT/DRDY output signal alternates between two modes of operation. The first mode of operation is the Data Ready (DRDY) mode to indicate that new data has been loaded into the data-output register and is ready to be read. The second mode of operation is the Data Output (DOUT) mode and is used to serially shift data out of the Data Output Register (DOR). See Figure 11 for the time domain partitioning of the DRDY and DOUT function.

See Figure 12 for the basic timing of DOUT/DRDY. During the time defined by $t_2$, $t_3$, and $t_4$, the DOUT/DRDY pin functions in DRDY mode. The state of the DOUT/DRDY pin is HIGH prior to the internal transfer of new data to the DOR. The result of the A/D conversion is written...

FIGURE 4. Digital Filter Response (50Hz).

FIGURE 5. Digital Filter Response (60Hz).

FIGURE 6. Digital Filter Response (10Hz Multiples).

FIGURE 7. Expanded Digital Filter Response (50Hz with a 50Hz Notch).

FIGURE 8. Expanded Digital Filter Response (50Hz with a 10Hz Notch).
to the DOR from MSB to LSB in the time defined by $t_1$ (see Figures 11 and 12). The DOUT/DRDY line then drives the line LOW for the time defined by $t_2$, and then drives the line HIGH for the time defined by $t_3$ to indicate that new data is available to be read. At this point, the function of the DOUT/DRDY pin changes to DOUT mode, and data is shifted out on the pin after $t_2$. If the MSB is high (because of a negative result) the DOUT/DRDY signal will stay HIGH after the end of time $t_3$. The device communicating with the ADS1252 can provide SCLKs to the ADS1252 after the time defined by $t_6$. The normal mode of reading data from the ADS1252 is for the device reading the ADS1252 to latch the data on the rising edge of SCLK (since data is shifted out of the ADS1252 on the falling edge of SCLK). In order to retrieve valid data, the entire DOR must be read before the DOUT/DRDY pin reverts back to DRDY mode.

If SCLKs are not provided to the ADS1252 during the DOUT mode, the MSB of the DOR is present on the DOUT/DRDY line until the beginning of the time defined by $t_4$. If an incomplete read of the ADS1252 takes place in DOUT mode (that is, fewer than 24 SCLKs are provided), the state of the last bit read is present on the DOUT/DRDY line until the beginning of the time defined by $t_4$. If more than 24 SCLKs are provided during DOUT mode, the DOUT/DRDY line stays LOW until the beginning of the time defined by $t_4$.

The internal data pointer for shifting data out on DOUT/DRDY is reset on the falling edge of the time defined by $t_1$ and $t_4$. This ensures that the first bit of data shifted out of the ADS1252 after DRDY mode is always the MSB of new data.

**SYNCHRONIZING MULTIPLE CONVERTERS**

The normal state of SCLK is LOW; however, by holding SCLK HIGH, multiple ADS1252s can be synchronized. This is accomplished by holding SCLK HIGH for at least four, but less than 20, consecutive DOUT/DRDY cycles (see Figure 13). After the ADS1252 circuitry detects that SCLK has been held HIGH for four consecutive DOUT/DRDY cycles, the DOUT/DRDY pin pulses LOW for 3 CLK cycles and then held HIGH, and the modulator is held in a reset state. The modulator is released from reset and synchronization occurs on the falling edge of SCLK. It is important to note that prior to synchronization, the DOUT/DRDY pulse of multiple ADS1252s in the system can have a difference in timing up to one DRDY period. Therefore, to ensure synchronization, the SCLK must be held HIGH for at least five DRDY cycles. The first DOUT/DRDY pulse after the falling edge of SCLK occurs at $t_4$. Valid data is not present until the sixth DOUT/DRDY pulse.
POWER-DOWN MODE
The normal state of SCLK is LOW; however, by holding SCLK HIGH, the ADS1252 enters power-down mode. This is accomplished by holding SCLK HIGH for at least 20 consecutive DOUT/DRDY cycles (see Figure 14). After the ADS1252 circuitry detects that SCLK is held HIGH for four consecutive DOUT/DRDY cycles, the DOUT/DRDY pin pulses LOW for three CLK cycles, then held HIGH, and the modulator will be held in a reset state. If SCLK is held HIGH for an additional 16 DOUT/DRDY periods, the ADS1252 enters power-down mode and the part is released from power-down mode on the falling edge of SCLK. It is important to note that if the DOUT/DRDY pulse is held HIGH after four DOUT/DRDY cycles, but power-down mode is not entered for an additional 16 DOUT/DRDY periods. The first DOUT/DRDY pulse after the falling edge of SCLK occurs at t^1_16; however, subsequent DOUT/DRDY pulses occur normally. Valid data is not present until the sixth DOUT/DRDY pulse.

SERIAL INTERFACE
The ADS1252 includes a simple serial interface which can be connected to microcontrollers and digital signal processors in a variety of ways. Communications with the ADS1252 can commence on the first detection of the DOUT/DRDY pulse after power up, although data is valid until the sixth conversion.

It is important to note that the data from the ADS1252 is a 24-bit result transmitted MSB-first in Offset Binary Two’s Complement format, as shown in Table III.

The data must be clocked out before the ADS1252 enters DRDY mode to ensure receipt of valid data, as described in the DOUT/DRDY section of this data sheet.

<table>
<thead>
<tr>
<th><strong>DIFFERENTIAL VOLTAGE INPUT</strong></th>
<th><strong>DIGITAL OUTPUT (HEX)</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>+Full-Scale</td>
<td>7FFFFFF_H</td>
</tr>
<tr>
<td>Zero</td>
<td>0000000_H</td>
</tr>
<tr>
<td>–Full-Scale</td>
<td>8000000_H</td>
</tr>
</tbody>
</table>

TABLE III. ADS1252 Data Format (Offset Binary Two’s Complement).

<table>
<thead>
<tr>
<th><strong>TABLE II. Digital Timing.</strong></th>
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</thead>
<tbody>
<tr>
<td><strong>SYMBOL</strong></td>
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<td>t_DRDY</td>
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<tr>
<td>t_DRDY_1</td>
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<tr>
<td>t_DRDY_2</td>
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<tr>
<td>t_DRDY_3</td>
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<td>t_DRDY_4</td>
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<tr>
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<tr>
<td>t_DRDY_7</td>
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<tr>
<td>t_DRDY_8</td>
</tr>
<tr>
<td>t_DRDY_9</td>
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<td>t_DRDY_10</td>
</tr>
</tbody>
</table>

FIGURE 11. DOUT/DRDY Partitioning.
FIGURE 12. DOUT/DRDY Timing.

FIGURE 13. Synchronization Mode.

ISOLATION
The serial interface of the ADS1252 provides for simple isolation methods. The CLK signal can be local to the ADS1252, which then only requires two signals (SCLK and DOUT/DRDY) to be used for isolated data acquisition.

LAYOUT
POWER SUPPLY
The power supply should be well regulated and low noise. For designs requiring very high resolution from the ADS1252, power-supply rejection will be a concern. Avoid running digital lines under the device because they can couple noise onto the die. High-frequency noise can capacitively couple into the analog portion of the device and will alias back into the passband of the digital filter, affecting the conversion result.

GROUNDING
The analog and digital sections of the system design must be carefully and cleanly partitioned; each section must have its own ground plane with no overlap between them. GND must be connected to the analog ground plane, as well as all other analog grounds. Do not join the analog and digital ground planes on the board, but instead connect the two with a moderate signal trace. For multiple converters, connect the two ground planes at one location as central to all of the converters as possible. In some cases, experimentation is required to find the best point to connect the two planes together. The printed circuit board can be designed to provide different analog/digital ground connections via short jumpers; the initial prototype can be used to establish which connection works best.

DECOUPLING
Good decoupling practices must be used for the ADS1252 and for all components in the design. All decoupling capacitors, and specifically the 0.1μF ceramic capacitors, must be placed as close as possible to the pin being decoupled. A 1μF to 10μF capacitor, in parallel with a 0.1μF ceramic capacitor, must be used to decouple VDD to GND.

SYSTEM CONSIDERATIONS
The recommendations for power supplies and grounding change depending on the requirements and specific design of the overall system. Achieving 24 bits of noise performance is a great deal more difficult than achieving 12 bits of noise performance. In general, a system can be broken up into four different stages:

- Analog Processing
- Analog Portion of the ADS1252
- Digital Portion of the ADS1252
- Digital Processing

For the simplest system consisting of minimal analog signal processing (basic filtering and gain), a microcontroller, and one clock source, one can achieve high resolution by powering all components by a common power supply. In addition, all components can share a common ground plane; thus, there would be no distinctions between analog power and ground, and digital power and ground. The layout must still include a power plane, a ground plane, and careful decoupling. In a more extreme case, the design can include:

- Multiple ADS1252s
- Extensive Analog Signal Processing
- One or More Microcontrollers, Digital Signal Processors, or Microprocessors
- Many Different Clock Sources
- Interconnections to Various Other Systems

High resolution will be very difficult to achieve for this design. The approach would be to break the system into as many different parts as possible. For example, each ADS1252 may have its own analog processing front end.

DEFINITION OF TERMS
An attempt has been made to be consistent with the terminology used in this data sheet. In that regard, the definition of each term is given as follows:

Analog-Input Differential Voltage—for an analog signal that is fully differential, the voltage range can be compared to that of an instrumentation amplifier. For example, if both analog inputs of the ADS1252 are at 2.048V, the differential voltage is 0V; however, if one analog input is at 0V and the other analog input is at 4.096V, then the differential voltage magnitude is 4.096V. This is the case regardless of which input is at 0V and which is at 4.096V. The digital-output
result, however, is quite different. The analog-input differential voltage is given by the following equation:

\[ V_{IN} - (-V_{IN}) \]

A positive digital output is produced whenever the analog-input differential voltage is positive, whereas negative digital output is produced whenever the differential is negative. For example, a positive full-scale output is produced when the converter is configured with a 4.096V reference, and the analog-input differential is 4.096V, the negative full-scale output is produced when the differential voltage is –4.096V. In each case, the actual input voltages must remain within the –0.3V to +VDD range.

**Actual Analog-Input Voltage**—the voltage at any one analog input relative to GND.

**Full-Scale Range (FSR)**—as with most A/D converters, the full-scale range of the ADS1252 is defined as the input which produces the positive full-scale digital output minus the input which produces the negative full-scale digital output. For example, when the converter is configured with a 4.096V reference, the differential full-scale range is:

\[ [4.096V \text{ (positive full-scale)} - (-4.096V) \text{ (negative full-scale)}] = 8.192V \]

**Least Significant Bit (LSB) Weight**—this is the theoretical amount of voltage that the differential voltage at the analog input has to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

\[ \text{LSB Weight} = \frac{\text{Full-Scale Range}}{2^N} \]

where N is the number of bits in the digital output.

**Conversion Cycle**—as used here, a conversion cycle refers to the time period between DOUT/DRDY pulses.

**Effective Resolution (ER)**—of the ADS1252 in a particular configuration can be expressed in two different units: bits rms (referenced to output) and \( \mu \)Vrms (referenced to input). Computed directly from the converter output data, each is a statistical calculation based on a given number of results. Noise occurs randomly; the rms value represents a statistical measure which is one standard deviation. The ER in bits can be computed as follows:

\[ \text{ER in bits rms} = \frac{20 \log \left( \frac{2 \cdot V_{REF}}{\text{Vrms noise}} \right)}{6.02} \]

The \( 2 \cdot V_{REF} \) figure in each calculation represents the full-scale range of the ADS1252, this means that both units are absolute expressions of resolution—the performance in different configurations can be directly compared, regardless of the units.

**Noise Reduction**—for random noise, the ER can be improved with averaging. The result is the reduction in noise by the factor \( \sqrt{N} \), where N is the number of averages, as shown in Table IV; this can be used to achieve true 24-bit performance at a lower data rate. To achieve 24 bits of resolution, more than 24 bits must be accumulated. A 36-bit accumulator is required to achieve an ER of 24 bits. The following uses \( V_{REF} = 4.096V \), with the ADS1252 outputting data at 40kHz, a 4096 point average takes 102.4ms. The benefits of averaging is degraded if the input signal drifts during that 100ms.

<table>
<thead>
<tr>
<th>N (NUMBER OF AVERAGES)</th>
<th>NOISE REDUCTION FACTOR</th>
<th>ER IN ( \mu )Vrms</th>
<th>ER IN BITS rms</th>
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<tr>
<td>1</td>
<td>1</td>
<td>31.3( \mu )V</td>
<td>18</td>
</tr>
<tr>
<td>2</td>
<td>1.414</td>
<td>22.1( \mu )V</td>
<td>18.5</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>15.6( \mu )V</td>
<td>19</td>
</tr>
<tr>
<td>8</td>
<td>2.82</td>
<td>11.1( \mu )V</td>
<td>19.5</td>
</tr>
<tr>
<td>16</td>
<td>4</td>
<td>7.82( \mu )V</td>
<td>20</td>
</tr>
<tr>
<td>32</td>
<td>5.66</td>
<td>5.53( \mu )V</td>
<td>20.5</td>
</tr>
<tr>
<td>64</td>
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<td>3.91( \mu )V</td>
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</tr>
<tr>
<td>128</td>
<td>11.3</td>
<td>2.77( \mu )V</td>
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<tr>
<td>256</td>
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<td>1.96( \mu )V</td>
<td>22</td>
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<tr>
<td>512</td>
<td>22.6</td>
<td>1.38( \mu )V</td>
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<tr>
<td>1024</td>
<td>32</td>
<td>978nV</td>
<td>23</td>
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**TABLE IV. Averaging.**
## Revision History

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<th>PAGE</th>
<th>SECTION</th>
<th>DESCRIPTION</th>
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<td>D</td>
<td>11</td>
<td>DOUT/DRDY</td>
<td>Text changes to DOUT/DRDY section.</td>
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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
### PACKAGING INFORMATION

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<th>Package Qty</th>
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<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<td>ADS1252U</td>
<td>Samples</td>
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(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

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- **Green (RoHS & no Sb/Br)**: TI defines “Green” to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
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### TAPE AND REEL INFORMATION

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<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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*All dimensions are nominal.*
TAPE AND REEL BOX DIMENSIONS

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*All dimensions are nominal*
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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