12-BIT 4-CHANNEL SERIAL-OUTPUT SAMPLING ANALOG-TO-DIGITAL CONVERTER

FEATURES

• Qualified for Automotive Applications
• Single Supply: 2.7 V To 5 V
• Four-Channel Single-Ended Or Two-Channel Differential Input
• Up To 200-kHz Conversion Rate
• ±2 LSB Max INL and DNL
• No Missing Codes
• 71-dB Typ SINAD
• Serial Interface
• Alternate Source For MAX1247

DESCRIPTION

The ADS7841 is a 4-channel 12-bit sampling analog-to-digital converter (ADC) with a synchronous serial interface. The resolution is programmable to either 8 bits or 12 bits. Typical power dissipation is 2 mW at a 200-kHz throughput rate and a 5-V supply. The reference voltage \((V_{\text{REF}})\) can be varied between 100 mV and \(V_{\text{CC}}\), providing a corresponding input voltage range of 0 V to \(V_{\text{REF}}\). The device includes a shutdown mode that reduces power dissipation to under 15 μW. The ADS7841 is specified down to 2.7-V operation.

Low power, high speed, and on-board multiplexer make the ADS7841 ideal for battery-operated systems. The serial interface also provides low-cost isolation for remote data acquisition. The ADS7841 is available in a SSOP-16 package.
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>$T_A$</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>–40°C to 85°C</td>
<td>ADS7841EIDBQRQ1</td>
<td>S7841E</td>
</tr>
<tr>
<td>–40°C to 125°C</td>
<td>ADS7841ESQDBQRQ1</td>
<td>S7841S</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

### TERMINAL FUNCTIONS

<table>
<thead>
<tr>
<th>TERMINAL</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>1</td>
<td>Power supply</td>
</tr>
<tr>
<td>CH0</td>
<td>2</td>
<td>Analog input channel 0</td>
</tr>
<tr>
<td>CH1</td>
<td>3</td>
<td>Analog input channel 1</td>
</tr>
<tr>
<td>CH2</td>
<td>4</td>
<td>Analog input channel 2</td>
</tr>
<tr>
<td>CH3</td>
<td>5</td>
<td>Analog input channel 3</td>
</tr>
<tr>
<td>COM</td>
<td>6</td>
<td>Ground reference for analog inputs. Sets zero code voltage in single-ended mode. Connect this pin to ground or ground reference point.</td>
</tr>
<tr>
<td>SHDN</td>
<td>7</td>
<td>Shutdown. When low, the device enters a very low power shutdown mode.</td>
</tr>
<tr>
<td>VREF</td>
<td>8</td>
<td>Voltage reference</td>
</tr>
<tr>
<td>VCC</td>
<td>9</td>
<td>Power supply</td>
</tr>
<tr>
<td>GND</td>
<td>10</td>
<td>Ground</td>
</tr>
<tr>
<td>MODE</td>
<td>11</td>
<td>Conversion mode. When low, the device always performs a 12-bit conversion. When high, the resolution is set by the MODE bit in the CONTROL byte.</td>
</tr>
<tr>
<td>DOUT</td>
<td>12</td>
<td>Serial data output. Data is shifted on the falling edge of DCLK. This output is high-impedance when CS is high.</td>
</tr>
<tr>
<td>BUSY</td>
<td>13</td>
<td>Busy output. This output is high-impedance when CS is high.</td>
</tr>
<tr>
<td>DIN</td>
<td>14</td>
<td>Serial data input. If CS is low, data is latched on rising edge of DCLK.</td>
</tr>
<tr>
<td>CS</td>
<td>15</td>
<td>Chip select input. Controls conversion timing and enables the serial input/output register.</td>
</tr>
<tr>
<td>DCLK</td>
<td>16</td>
<td>External clock input. This clock runs the SAR conversion process and synchronizes serial data I/O.</td>
</tr>
</tbody>
</table>
### ABSOLUTE MAXIMUM RATINGS\(^{(1)}\)

Over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC}) Supply voltage</td>
<td>–0.3 V to 6 V</td>
</tr>
<tr>
<td>(V_{IN}) Input voltage</td>
<td>Analog inputs to GND: –0.3 V to ((V_{CC} + 0.3) V) Digital inputs to GND: –0.3 V to 6 V</td>
</tr>
<tr>
<td>(P_D) Power dissipation</td>
<td>250 mW</td>
</tr>
<tr>
<td>(T_J) Maximum virtual-junction temperature</td>
<td>150°C</td>
</tr>
<tr>
<td>(T_A) Operating free-air temperature range</td>
<td>ADS7841EIDBQRQ1: –40°C to 85°C ADS7841ESQDBQRQ1: –40°C to 125°C</td>
</tr>
<tr>
<td>(T_{stg}) Storage temperature range</td>
<td>–65°C to 150°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### ELECTROSTATIC DISCHARGE RATINGS

<table>
<thead>
<tr>
<th>ESD</th>
<th>RATING</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrostatic discharge rating</td>
<td>Human-Body Model (HBM) 2000 V</td>
</tr>
<tr>
<td></td>
<td>Machine Model (MM) 150 V</td>
</tr>
<tr>
<td></td>
<td>Charged-Device Model (CDM) 1000 V</td>
</tr>
</tbody>
</table>

### RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC}) Supply voltage</td>
<td>4.75</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>(V_{REF}) Reference voltage, (V_{REF}) terminal</td>
<td>0.1</td>
<td>(V_{CC})</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IN}) Input voltage, analog inputs</td>
<td>Differential, full-scale</td>
<td>0</td>
<td>(V_{REF})</td>
</tr>
<tr>
<td></td>
<td>Positive input</td>
<td>(V_{CC} = 5) V (nom)</td>
<td>–0.2</td>
</tr>
<tr>
<td></td>
<td>Negative input</td>
<td>(V_{CC} = 5) V (nom)</td>
<td>–0.2</td>
</tr>
<tr>
<td>(V_{IH}) High-level input voltage, digital inputs</td>
<td>(</td>
<td>I_{IH}</td>
<td>\leq 5) (\mu)A</td>
</tr>
<tr>
<td></td>
<td>(V_{CC} = 2.7) V (nom)</td>
<td>0.7</td>
<td>(V_{CC})</td>
</tr>
<tr>
<td>(V_{IL}) Low-level input voltage, digital inputs</td>
<td>(</td>
<td>I_{IL}</td>
<td>\leq 5) (\mu)A</td>
</tr>
<tr>
<td></td>
<td>(V_{CC} = 2.7) V (nom)</td>
<td>–0.3</td>
<td>0.8</td>
</tr>
<tr>
<td>(T_A) Operating free-air temperature</td>
<td>ADS7841EIDBQRQ1</td>
<td>–40</td>
<td>85</td>
</tr>
<tr>
<td></td>
<td>ADS7841ESQDBQRQ1</td>
<td>–40</td>
<td>125</td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS**

$V_{CC} = 5\, \text{V}$, $V_{REF} = 5\, \text{V}$, $f_{\text{SAMPLE}} = 200\, \text{kHz}$, $f_{CLK} = 16 \times f_{\text{SAMPLE}} = 3.2\, \text{MHz}$, over operating temperature $-40\, ^\circ\text{C}$ to $125\, ^\circ\text{C}$ (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Analog Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_I$ Input capacitance</td>
<td></td>
<td>25</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{leak}}$ Leakage current</td>
<td></td>
<td>200</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>System Performance</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resolution</td>
<td></td>
<td>12</td>
<td>bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>No missing codes</td>
<td></td>
<td>12</td>
<td>bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADS7841EIDBQRQ1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADS7841ESQDBQRQ1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\text{INL}$ Integral linearity error</td>
<td></td>
<td>$\pm 2$</td>
<td>LSB$^{(1)}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\text{DNL}$ Differential linearity error</td>
<td></td>
<td>$\pm 0.8$</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset error</td>
<td></td>
<td>$\pm 3$</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset error match</td>
<td></td>
<td>0.15</td>
<td>1 LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain error</td>
<td></td>
<td>$\pm 4$</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain error match</td>
<td></td>
<td>0.1</td>
<td>1 LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{n}}$ Noise</td>
<td></td>
<td>30</td>
<td>$\mu\text{V}_{\text{rms}}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PSRR</strong> Power-supply ripple rejection</td>
<td></td>
<td>70</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Sampling Dynamics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{\text{conv}}$ Conversion time</td>
<td></td>
<td>12</td>
<td>CLK cycle</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{\text{acq}}$ Acquisition time</td>
<td></td>
<td>3</td>
<td>CLK cycle</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Throughput rate</td>
<td></td>
<td>200</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{\text{settle}}$ Multiplexer settling time</td>
<td></td>
<td>500</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{\text{d}}$ Aperture delay</td>
<td></td>
<td>30</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{\text{jitter}}$ Aperture jitter</td>
<td></td>
<td>100</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Dynamic Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\text{THD}$ Total harmonic distortion$^{(2)}$</td>
<td></td>
<td>$V_{I_{\text{IN}}} = 5, \text{V}_{\text{pp}}$ at 10 kHz</td>
<td>$-78$</td>
<td>$-72$</td>
<td>dB</td>
</tr>
<tr>
<td>$\text{SINAD}$ Signal to noise + distortion ratio</td>
<td>$V_{I_{\text{IN}}} = 5, \text{V}_{\text{pp}}$ at 10 kHz</td>
<td>68</td>
<td>71</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$\text{Spurious-free dynamic range}$</td>
<td>$V_{I_{\text{IN}}} = 5, \text{V}_{\text{pp}}$ at 10 kHz</td>
<td>72</td>
<td>79</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$\text{Channel-to-channel isolation}$</td>
<td>$V_{I_{\text{IN}}} = 5, \text{V}_{\text{pp}}$ at 50 kHz</td>
<td>120</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Reference Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_I$ Resistance</td>
<td></td>
<td>5</td>
<td>GΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_I$ Input current</td>
<td></td>
<td>40</td>
<td>100</td>
<td>$\mu\text{A}$</td>
<td></td>
</tr>
<tr>
<td>DCLK static</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{SAMPLE}} = 12.5, \text{kHz}$</td>
<td></td>
<td>2.5</td>
<td>$\mu\text{A}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DCLK static</td>
<td></td>
<td>0.001</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Digital Input/Output</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OH}}$ High-level output voltage</td>
<td>$I_{\text{OH}} = -250, \mu\text{A}$</td>
<td>3.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OL}}$ Low-level output voltage</td>
<td>$I_{\text{OL}} = 250, \mu\text{A}$</td>
<td>0.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Power Supply</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_Q$ Quiescent current</td>
<td></td>
<td>550</td>
<td>900</td>
<td>$\mu\text{A}$</td>
<td></td>
</tr>
<tr>
<td>$f_{\text{SAMPLE}} = 12.5, \text{kHz}$</td>
<td></td>
<td>300</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power-down mode$^{(3)}$, $\overline{\text{CS}} = \overline{V_{CC}}$</td>
<td></td>
<td>3</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) LSB = least significant bit. With $V_{REF} = 5\, \text{V}$, one LSB is 1.22 mV.

(2) First five harmonics of the test frequency

(3) Auto power-down mode (PD1 = PD0 = 0) active or $\text{SHDN} = \overline{\text{GND}}$
### ELECTRICAL CHARACTERISTICS

$V_{CC} = 2.7 \ V$, $V_{REF} = 2.5 \ V$, $f_{SAMPLE} = 125 \ kHz$, $f_{CLK} = 16 \times f_{SAMPLE} = 2 \ MHz$, over operating temperature $-40^\circ C$ to $85^\circ C$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Analog Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_i$</td>
<td>Input capacitance</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$I_{\text{leak}}$</td>
<td>Leakage current</td>
<td></td>
<td></td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td><strong>System Performance</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Resolution</td>
<td>12</td>
<td></td>
<td></td>
<td>bits</td>
</tr>
<tr>
<td></td>
<td>No missing codes</td>
<td></td>
<td></td>
<td></td>
<td>12 bits</td>
</tr>
<tr>
<td></td>
<td>INL</td>
<td>Integral linearity error</td>
<td>$\pm 2$</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td></td>
<td>DNL</td>
<td>Differential linearity error</td>
<td>$\pm 0.8$</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td></td>
<td>Offset error</td>
<td>$\pm 3$</td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td></td>
<td>Offset error match</td>
<td></td>
<td></td>
<td>$0.15$</td>
<td>1 LSB</td>
</tr>
<tr>
<td></td>
<td>Gain error</td>
<td></td>
<td></td>
<td>$\pm 4$</td>
<td>LSB</td>
</tr>
<tr>
<td></td>
<td>Gain error match</td>
<td></td>
<td></td>
<td>$0.1$</td>
<td>1 LSB</td>
</tr>
<tr>
<td></td>
<td>$V_n$</td>
<td>Noise</td>
<td></td>
<td></td>
<td>$30$</td>
</tr>
<tr>
<td></td>
<td>PSRR</td>
<td>Power-supply ripple rejection</td>
<td></td>
<td></td>
<td>$70$</td>
</tr>
<tr>
<td><strong>Sampling Dynamics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{\text{conv}}$</td>
<td>Conversion time</td>
<td></td>
<td></td>
<td>$12$</td>
</tr>
<tr>
<td></td>
<td>$t_{\text{acq}}$</td>
<td>Acquisition time</td>
<td></td>
<td></td>
<td>$3$</td>
</tr>
<tr>
<td></td>
<td>Throughput rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{\text{settle}}$</td>
<td>Multiplexer settling time</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_d$</td>
<td>Aperture delay</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{\text{jitter}}$</td>
<td>Aperture jitter</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Dynamic Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>THD</td>
<td>Total harmonic distortion$^{(2)}$</td>
<td>$V_{IN} = 2.5 \ V_{\text{p-p}}$ at $10 \ kHz$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SINAD</td>
<td>Signal to noise + distortion ratio</td>
<td>$V_{IN} = 2.5 \ V_{\text{p-p}}$ at $10 \ kHz$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Spurious-free dynamic range</td>
<td>$V_{IN} = 2.5 \ V_{\text{p-p}}$ at $10 \ kHz$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Channel-to-channel isolation</td>
<td>$V_{IN} = 2.5 \ V_{\text{p-p}}$ at $50 \ kHz$</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Reference Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_i$</td>
<td>Resistance</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_i$</td>
<td>Input current</td>
<td>$DCLK$ static</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{\text{SAMPLE}} = 12.5 \ kHz$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$DCLK$ static</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Digital Input/Output</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{OH}$</td>
<td>High-level output voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{OL}$</td>
<td>Low-level output voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Power Supply</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_Q$</td>
<td>Quiescent current</td>
<td>$f_{\text{SAMPLE}} = 12.5 \ kHz$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Power-down mode$^{(3)}$, $CS = V_{CC}$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

(1) LSB = least significant bit. With $V_{REF} = 2.5 \ V$, one LSB is $0.61 \ mV$.  
(2) First five harmonics of the test frequency  
(3) Auto power-down mode (PD1 = PD0 = 0) active or SHDN = GND
TYPICAL CHARACTERISTICS, $V_{CC} = 5$ V

$V_{CC} = 5$ V, $T_A = 25^\circ$C, $V_{REF} = 5$ V, $f_{SAMPLE} = 200$ kHz, $f_{CLK} = 16 \times f_{SAMPLE} = 3.2$ MHz (unless otherwise noted)

FREQUENCY SPECTRUM
(4096 Point FFT; $f_{IN} = 1,123$Hz, $-0.2$dB)

Amplitude (dB)

0 25 50 75 100
Frequency (kHz)

FREQUENCY SPECTRUM
(4096 Point FFT; $f_{IN} = 10.3$kHz, $-0.2$dB)

Amplitude (dB)

0 25 50 75 100
Frequency (kHz)

SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY

SNR

74
73
72
71
70
69
68

68
69
70
71
72
73
74

Input Frequency (kHz)

SINAD

SPURIOUS-FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY

SFDR (dB)

85
80
75
70
65
–85
–80
–75
–70
–65

THD (dB)

–65
–70
–75
–80
–85

Input Frequency (kHz)

CHANGE IN SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE

Delta from 25°C (dB)

0.6
0.4
0.2
0.0
–0.2
–0.4
–0.6

Temperature (°C)

f_{IN} = 10kHz, $-0.2$dB

Amplitude (dB)

0
–20
–40
–60
–80
–100
–120

0
–20
–40
–60
–80
–100
–120

0
–20
–40
–60
–80
–100
–120

FREQUENCY SPECTRUM
(4096 Point FFT; $f_{IN} = 10.3$kHz, $-0.2$dB)

0
10025 75 50
Frequency (kHz)

Amplitude (dB)

0
–20
–40
–60
–80
–100
–120

0
10025 75 50
Frequency (kHz)

Amplitude (dB)

0
–20
–40
–60
–80
–100
–120

0
10025 75 50
Frequency (kHz)

Amplitude (dB)

0
–20
–40
–60
–80
–100
–120

0
10025 75 50
Frequency (kHz)
TYPICAL CHARACTERISTICS, \( V_{CC} = 2.7 \) V

\( V_{CC} = 2.7 \) V, \( T_A = 25^\circ C, \ V_{REF} = 2.5 \) V, \( f_{SAMPLE} = 125 \) kHz, \( f_{CLK} = 16 \times f_{SAMPLE} = 2 \) MHz (unless otherwise noted)

FREQUENCY SPECTRUM
(4096 Point FFT; \( f_{IN} = 1.129\)Hz, –0.2dB)

SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-(NOISE+DISTORTION) vs INPUT FREQUENCY

SNR and SINAD (dB)

0 62.5 15.6 46.9 62.5
Frequency (kHz)

Input Frequency (kHz)

Effective Number of Bits

0 62.5 15.6 46.9 62.5
Frequency (kHz)

Input Frequency (kHz)

Effective Number of Bits

0 62.5 15.6 46.9 62.5
Frequency (kHz)

Input Frequency (kHz)

Effective Number of Bits

0 62.5 15.6 46.9 62.5
Frequency (kHz)

Input Frequency (kHz)

Effective Number of Bits

0 62.5 15.6 46.9 62.5
Frequency (kHz)

Input Frequency (kHz)

Effective Number of Bits

0 62.5 15.6 46.9 62.5
Frequency (kHz)

Input Frequency (kHz)

Effective Number of Bits
TYPICAL CHARACTERISTICS, $V_{CC} = 2.7$ V (continued)

$V_{CC} = 2.7$ V, $T_A = 25^\circ$C, $V_{REF} = 2.5$ V, $f_{\text{SAMPLE}} = 125$ kHZ, $f_{\text{CLK}} = 16 \times f_{\text{SAMPLE}} = 2$ MHz (unless otherwise noted)

**SUPPLY CURRENT vs TEMPERATURE**

**POWER DOWN SUPPLY CURRENT vs TEMPERATURE**

**INTEGRAL LINEARITY ERROR vs CODE**

**DIFFERENTIAL LINEARITY ERROR vs CODE**

**CHANGE IN GAIN vs TEMPERATURE**

**CHANGE IN OFFSET vs TEMPERATURE**
TYPICAL CHARACTERISTICS, $V_{CC} = 2.7$ V (continued)

$V_{CC} = 2.7$ V, $T_A = 25^\circ$C, $V_{REF} = 2.5$ V, $f_{SAMPLE} = 125$ kHz, $f_{CLK} = 16 \times f_{SAMPLE} = 2$ MHz (unless otherwise noted)

**REFERENCE CURRENT vs SAMPLE RATE**

**REFERENCE CURRENT vs TEMPERATURE**

**SUPPLY CURRENT vs $V_{CC}$**

**MAXIMUM SAMPLE RATE vs $V_{CC}$**
The ADS7841 is a classic successive approximation register (SAR) ADC. The architecture is based on capacitive redistribution that inherently includes a sample-and-hold function. The converter is fabricated on a 0.6-μs CMOS process.

The basic operation of the ADS7841 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.7 V to 5.25 V. The external reference can be any voltage between 100 mV and $V_{CC}$. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS7841.

Analog Input

Figure 2 shows a block diagram of the input multiplexer on the ADS7841. The differential input of the converter is derived from one of the four inputs in reference to the COM pin or two of the four inputs. Table 1 and Table 2 show the relationship between the A2, A1, A0, and SGL/DIF control bits and the configuration of the analog multiplexer. The control bits are provided serially via the DIN pin, see the Digital Interface section of this data sheet for more details.
Table 1. Single-Ended Channel Selection (SGL/DIF high)

<table>
<thead>
<tr>
<th>A2</th>
<th>A1</th>
<th>A0</th>
<th>CH0</th>
<th>CH1</th>
<th>CH2</th>
<th>CH3</th>
<th>COM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>+IN</td>
<td></td>
<td></td>
<td></td>
<td>−IN</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
<td>+IN</td>
<td></td>
<td></td>
<td>−IN</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
<td>+IN</td>
<td></td>
<td></td>
<td>−IN</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td>+IN</td>
<td></td>
<td>−IN</td>
</tr>
</tbody>
</table>

Table 2. Differential Channel Control (SGL/DIF low)

<table>
<thead>
<tr>
<th>A2</th>
<th>A1</th>
<th>A0</th>
<th>CH0</th>
<th>CH1</th>
<th>CH2</th>
<th>CH3</th>
<th>COM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>+IN</td>
<td></td>
<td>−IN</td>
<td></td>
<td>−IN</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
<td>−IN</td>
<td>+IN</td>
<td></td>
<td>−IN</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td>+IN</td>
<td></td>
<td>−IN</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td>−IN</td>
<td></td>
<td>+IN</td>
</tr>
</tbody>
</table>

When the converter enters the hold mode, the voltage difference between the +IN and −IN inputs (as shown in Figure 2) is captured on the internal capacitor array. The voltage on the −IN input is limited between −0.2 V and 1.25 V, allowing the input to reject small signals that are common to both the +IN and −IN input. The +IN input has a range of −0.2 V to $V_{CC} + 0.2$ V.

The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25 pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

Reference Input

The external reference sets the analog input range. The ADS7841 operates with a reference in the range of 100 mV to $V_{CC}$. Keep in mind that the analog input is the difference between the +IN input and the −IN input, see Figure 2. For example, in the single-ended mode, a 1.25-V reference, and with the COM pin grounded, the selected input channel (CH0-CH3) digitizes a signal in the range of 0 V to 1.25 V. If the COM pin is connected to 0.5 V, the input range on the selected channel is 0.5 V to 1.75 V.

There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. Any offset or gain error inherent in the ADC appears to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2 LSBs with a 2.5-V reference, then it is typically 10 LSBs with a 0.5-V reference. In each case, the actual offset of the device is the same, 1.22 mV.

Likewise, the noise or uncertainty of the digitized output increases with lower LSB size. With a reference voltage of 100 mV, the LSB size is 24 μV. This level is below the internal noise of the device. As a result, the digital output code is not stable and varies around a mean value by a number of LSBs. The distribution of output codes is gaussian, and the noise can be reduced by simply averaging consecutive conversion results or applying a digital filter.

With a lower reference voltage, care should be taken to provide a clean layout including adequate bypassing, a clean (low-noise, low-ripple) power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter is also more sensitive to nearby digital signals and electromagnetic interference.

The voltage into the $V_{REF}$ input is not buffered and directly drives the Capacitor Digital-to-Analog Converter (CDAC) portion of the ADS7841. Typically, the input current is 13 μA with a 2.5-V reference. This value varies by microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period does not reduce overall current drain from the reference.
Digital Interface

Figure 3 shows the typical operation of the ADS7841's digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface (note that the digital inputs are over-voltage tolerant up to 5.5 V, regardless of \( V_{CC} \)). Each communication between the processor and the converter consists of eight clock cycles. One complete conversion can be accomplished with three serial communications, for a total of 24 clock cycles on the DCLK input.

![Timing Diagram](image)

A. 24 clock cycles per conversion, 8-bit bus interface. No DCLK delay required with dedicated serial port.

**Figure 3. Conversion Timing**

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer appropriately, it enters the acquisition (sample) mode. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the hold mode. The next twelve clock cycles accomplish the actual Analog-to-Digital conversion. A thirteenth clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT is low). These are ignored by the converter.

**Control Byte**

Also shown in Figure 3 is the placement and order of the control bits within the control byte. Table 3 and Table 4 give detailed information about these bits. The first bit, the 'S' bit, must always be high and indicates the start of the control byte. The ADS7841 ignores inputs on the DIN pin until the start bit is detected. The next three bits (A2-A0) select the active input channel or channels of the input multiplexer (see Table 1, Table 2, and Figure 2).

<table>
<thead>
<tr>
<th>Bit 7 (MSB)</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0 (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>A2</td>
<td>A1</td>
<td>A0</td>
<td>MODE</td>
<td>SGL/DIF</td>
<td>PD1</td>
<td>PD0</td>
</tr>
</tbody>
</table>

**Table 3. Order of Control Bits in Control Byte**

**Table 4. Descriptions of Control Bits Within Control Byte**

<table>
<thead>
<tr>
<th>BIT</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>S</td>
<td>Start bit. Control byte starts with first high bit on DIN. A new control byte can start every 15th clock cycle in 12-bit conversion mode or every 11th clock cycle in 8-bit conversion mode.</td>
</tr>
<tr>
<td>6-4</td>
<td>A2-A0</td>
<td>Channel select bits. Along with the SGL/DIF bit, these bits control the setting of the multiplexer input, see Table 1 and Table 2.</td>
</tr>
<tr>
<td>3</td>
<td>MODE</td>
<td>12-bit/8-bit conversion select bit. If the MODE pin is high, this bit controls the number of bits for the next conversion: 12-bits (low) or 8-bits (high). If the MODE pin is low, this bit has no function and the conversion is always 12 bits.</td>
</tr>
<tr>
<td>2</td>
<td>SGL/DIF</td>
<td>Single-ended/differential select bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input, see Table 1 and Table 2.</td>
</tr>
<tr>
<td>1-0</td>
<td>PD1-PD0</td>
<td>Power-down mode select bits. See Table 5 for details.</td>
</tr>
</tbody>
</table>
The MODE bit and the MODE pin work together to determine the number of bits for a given conversion. If the MODE pin is low, the converter always performs a 12-bit conversion regardless of the state of the MODE bit. If the MODE pin is high, then the MODE bit determines the number of bits for each conversion, either 12 bits (low) or 8 bits (high).

The SGL/DIF bit controls the multiplexer input mode: either single-ended (high) or differential (low). In single-ended mode, the selected input channel is referenced to the COM pin. In differential mode, the two selected inputs provide a differential input. See Table 1, Table 2, and Figure 2 for more information. The last two bits (PD1-PD0) select the powerdown mode, as shown in Table 5. If both inputs are high, the device is always powered up. If both inputs are low, the device enters a power-down mode between conversions. When a new conversion is initiated, the device resumes normal operation instantly—no delay is needed to allow the device to power up and the very first conversion is valid.

### Table 5. Power-Down Selection

<table>
<thead>
<tr>
<th>PD1</th>
<th>PD0</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Power-down between conversions. When each conversion is finished, the converter enters a low power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>No power-down between conversions, device always powered.</td>
</tr>
</tbody>
</table>

### 16 Clock Cycles Per Conversion

The control bits for conversion n+1 can be overlapped with conversion 'n' to allow for a conversion every 16 clock cycles, as shown in Figure 4. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer between the processor and the converter. This is possible provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that has been captured on the input sample-and-hold may droop enough to affect the conversion result. In addition, the ADS7841 is fully powered while other serial communications are taking place.

**Figure 4. Conversion Timing**
Digital Timing

Figure 5, Table 6, and Table 7 provide detailed timing for the digital interface of the ADS7841.

**Figure 5. Detailed Timing Diagram**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>DESCRIPTION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>tACQ</td>
<td>Acquisition time</td>
<td>1500</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDS</td>
<td>DIN valid prior to DCLK rising</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDH</td>
<td>DIN hold after DCLK high</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDO</td>
<td>DCLK falling to DOUT valid</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDV</td>
<td>CS falling to DOUT enabled</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tTR</td>
<td>CS rising to DOUT disabled</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCSS</td>
<td>CS falling to first DCLK rising</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCSH</td>
<td>CS rising to DCLK ignored</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCH</td>
<td>DCLK high</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCL</td>
<td>DCLK low</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tBD</td>
<td>DCLK falling to BUSY rising</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tBDSV</td>
<td>CS falling to BUSY enabled</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tSTR</td>
<td>CS rising to BUSY disabled</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Table 6. Timing Specifications, VCC = 2.7 V to 3.6 V, TA = –40°C to 85°C, CLoad = 50 pF**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>DESCRIPTION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>tACQ</td>
<td>Acquisition time</td>
<td>900</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDS</td>
<td>DIN valid prior to DCLK rising</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDH</td>
<td>DIN hold after DCLK high</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDO</td>
<td>DCLK falling to DOUT valid</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDV</td>
<td>CS falling to DOUT enabled</td>
<td>70</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tTR</td>
<td>CS rising to DOUT disabled</td>
<td>70</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCSS</td>
<td>CS falling to first DCLK rising</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCSH</td>
<td>CS rising to DCLK ignored</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCH</td>
<td>DCLK high</td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCL</td>
<td>DCLK low</td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tBD</td>
<td>DCLK falling to BUSY rising</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tBDSV</td>
<td>CS falling to BUSY enabled</td>
<td>70</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tSTR</td>
<td>CS rising to BUSY disabled</td>
<td>70</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Table 7. Timing Specifications, VCC = 4.75 V to 5.25 V, TA = –40°C to 85°C, CLoad = 50 pF**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>DESCRIPTION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>tACQ</td>
<td>Acquisition time</td>
<td>900</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDS</td>
<td>DIN valid prior to DCLK rising</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDH</td>
<td>DIN hold after DCLK high</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDO</td>
<td>DCLK falling to DOUT valid</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tDV</td>
<td>CS falling to DOUT enabled</td>
<td>70</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tTR</td>
<td>CS rising to DOUT disabled</td>
<td>70</td>
<td></td>
<td>ns</td>
</tr>
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<td>tCSS</td>
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<td>50</td>
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<td>ns</td>
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<td>tCSH</td>
<td>CS rising to DCLK ignored</td>
<td>0</td>
<td></td>
<td>ns</td>
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<tr>
<td>tCH</td>
<td>DCLK high</td>
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<td></td>
<td>ns</td>
</tr>
<tr>
<td>tCL</td>
<td>DCLK low</td>
<td>150</td>
<td></td>
<td>ns</td>
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<tr>
<td>tBD</td>
<td>DCLK falling to BUSY rising</td>
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<td>ns</td>
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<td>tBDSV</td>
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<td>70</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tSTR</td>
<td>CS rising to BUSY disabled</td>
<td>70</td>
<td></td>
<td>ns</td>
</tr>
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</table>
15 Clock Cycles Per Conversion

Figure 6 provides the fastest way to clock the ADS7841. This method does not work with the serial interface of most microcontrollers and digital signal processors as they are generally not capable of providing 15 clock cycles per serial transfer. However, this method could be used with field programmable gate arrays (FPGAs) or application specific integrated circuits (ASICs). Note that this effectively increases the maximum conversion rate of the converter beyond the values given in the specification tables, which assume 16 clock cycles per conversion.

Data Format

The ADS7841 output data is in straight binary format, as shown in Figure 7. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

8-Bit Conversion

The ADS7841 provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. This could be used in conjunction with serial interfaces that provide a 12-bit transfer or two conversions could be accomplished with three 8-bit transfers. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at a faster clock rate. This is because the internal settling time of the ADS7841 is not as critical, settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.
Power Dissipation

There are three power modes for the ADS7841: full power (PD1-PD0 = 11b), auto power-down (PD1-PD0 = 00b), and shutdown (SHDN low). The affects of these modes varies depending on how the ADS7841 is being operated. For example, at full conversion rate and 16 clocks per conversion, there is very little difference between full power mode and auto power-down. Likewise, if the device has entered auto power-down, a shutdown (SHDN low) does not lower power dissipation.

When operating at full-speed and 16-clocks per conversion (see Figure 4), the ADS7841 spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Thus, the difference between full power mode and auto power-down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion, but conversions are simply done less often, then the difference between the two modes is dramatic. Figure 8 shows the difference between reducing the DCLK frequency ("scaling" DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversions per second. In the later case, the converter spends an increasing percentage of its time in power-down mode (assuming the auto power-down mode is active).

A. Directly scaling the frequency of DCLK with sample rate or keeping DCLK at the maximum possible frequency

Figure 8. Supply Current vs Sample Rate

If DCLK is active and CS is low while the ADS7841 is in auto power-down mode, the device continues to dissipate some power in the digital logic. The power can be reduced to a minimum by keeping CS high. The differences in supply current for these two cases are shown in Figure 9.

A. Varied with state of CS

Figure 9. Supply Current vs Sample Rate
Operating the ADS7841 in auto power-down mode results in the lowest power dissipation, and there is no conversion time "penalty" on power-up. The very first conversion is valid. SHDN can be used to force an immediate power-down.

**PCB Layout**

For optimum performance, care should be taken with the physical layout of the ADS7841 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS7841 should be clean and well bypassed. A 0.1-μF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1-μF to 10-μF capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply.

The reference should be similarly bypassed with a 0.1-μF capacitor. Again, a series resistor and large capacitor can be used to low-pass filter the reference voltage. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation (the series resistor can help in this case). The ADS7841 draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of DCLK during a conversion).

The ADS7841 architecture offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. While high-frequency noise can be filtered out as discussed in the previous paragraph, voltage variation due to line frequency (50 Hz or 60 Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this is the "analog" ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.
## REVISION HISTORY

<table>
<thead>
<tr>
<th>Changes from Revision B (September, 2011) to Revision C</th>
<th>Page</th>
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<tr>
<td>• Deleted package column from Ordering Information table; changed top-side marking of ADS7841EIDBQRQ1 from ADS7841E to S7841E and changed top-side marking for ADS7841ESQDBQRQ1 from ADS7841S to S7841S.</td>
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## PACKAGING INFORMATION

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<th>Orderable Device</th>
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<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Top-Side Markings (4)</th>
<th>Samples</th>
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<td>Level-3-260C-168 HR</td>
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<td>-40 to 125</td>
<td>S7841S</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF ADS7841-Q1:**
Catalog: ADS7841

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width (W1)**

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Q1, Q2, Q3, Q4**: Pocket Quadrants
- **Sprocket Holes**: Orientation markers
- **User Direction of Feed**: Orientation of the tape

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
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<th>B0 (mm)</th>
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### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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</table>
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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