1 Features

- 1-MHz Sample Rate Serial Device
- 12-Bit Resolution
- Zero Latency
- 20-MHz Serial Interface
- Supply Range: 2.35 V to 5.25 V
- Typical Power Dissipation at 1 MSPS:
  - 3.9 mW at 3-V $V_{DD}$
  - 7.5 mW at 5-V $V_{DD}$
- INL ±1.25 LSB Maximum, ±0.65 LSB (Typical)
- DNL ±1 LSB Maximum, +0.4 / –0.65 LSB (Typical)
- Typical AC Performance:
  - 72.25-dB SINAD, –84-dB THD
- Unipolar Input Range: 0 V to $V_{DD}$
- Power Down Current: 1 µA
- Wide Input Bandwidth: 15 MHz at 3 dB
- 6-Pin SOT-23 and SC70 Packages

2 Applications

- Base Band Converters in Radio Communication
- Motor Current and Bus Voltage Sensors in Digital Drives
- Optical Networking (DWDM, MEMS Based Switching)
- Optical Sensors
- Battery-Powered Systems
- Medical Instrumentations
- High-Speed Data Acquisition Systems
- High-Speed Closed-Loop Systems

3 Description

The ADS7886 is a 12-bit, 1-MSPS analog-to-digital converter (ADC). The device includes a capacitor based SAR A/D converter with inherent sample and hold. The serial interface in each device is controlled by the CS and SCLK signals for glueless connections with microprocessors and DSPs. The input signal is sampled with the falling edge of CS, and SCLK is used for conversion and serial data output.

The device operates from a wide supply range from 2.35 V to 5.25 V. The low power consumption of the device makes it suitable for battery-powered applications. The device also includes a power down feature for power saving at lower conversion speeds.

The high level of the digital input to the device is not limited to device $V_{DD}$. This means the digital input can go as high as 5.25 V when device supply is 2.35 V. This feature is useful when digital signals are coming from other circuit with different supply levels. Also this relaxes restriction on power-up sequencing.

The ADS7886 is available in 6-pin SOT-23 and SC70 packages and is specified for operation from –40°C to 125°C.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS7886</td>
<td>SOT-23 (6)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
<tr>
<td></td>
<td>SC70 (6)</td>
<td>2.00 mm × 1.25 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2009) to Revision B Page
• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ......................................................... 1
• Deleted Package/Ordering Information table, see POA at the end of the datasheet. ................................................................. 1
• Changed $R_{\theta JA}$ values from: 295.2 °C/W to: 113.4 °C/W for DBV package ................................................................. 4
• Changed $R_{\theta JA}$ values from: 351.3 °C/W to: 149.6 °C/W for DCK package ................................................................. 4

Changes from Original (September 2005) to Revision A Page
• Added $V_{IH}$ information ................................................. 5
• Changed $V_{IH}$ information ............................................... 5
5 Device Comparison Table

Table 1. Micro-Power Miniature SAR Converter Family

<table>
<thead>
<tr>
<th>BIT</th>
<th>&lt; 300 KSPS</th>
<th>300 KSPS – 1.25 MSPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>12-Bit</td>
<td>ADS7866 (1.2 V_{DD} to 3.6 V_{DD})</td>
<td>ADS7886 (2.35 V_{DD} to 5.25 V_{DD})</td>
</tr>
<tr>
<td>10-Bit</td>
<td>ADS7867 (1.2 V_{DD} to 3.6 V_{DD})</td>
<td>ADS7887 (2.35 V_{DD} to 5.25 V_{DD})</td>
</tr>
<tr>
<td>8-Bit</td>
<td>ADS7888 (1.2 V_{DD} to 3.6 V_{DD})</td>
<td>ADS7888 (2.35 V_{DD} to 5.25 V_{DD})</td>
</tr>
</tbody>
</table>

6 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO.</td>
<td>NAME</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>V_{DD}</td>
<td>Power supply input also acts like a reference voltage to ADC.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground for power supply, all analog and digital signals are referred with respect to this pin.</td>
</tr>
<tr>
<td>3</td>
<td>VIN</td>
<td>Analog signal input</td>
</tr>
<tr>
<td>4</td>
<td>SCLK</td>
<td>Serial clock</td>
</tr>
<tr>
<td>5</td>
<td>SDO</td>
<td>Serial data out</td>
</tr>
<tr>
<td>6</td>
<td>CS</td>
<td>Chip select signal, active low</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(+\text{IN to AGND})</td>
<td>–0.3</td>
<td>(V_{DD}+0.3)</td>
<td>V</td>
</tr>
<tr>
<td>(+\text{V}_{DD}) to AGND</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Digital input voltage to GND</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Digital output to GND</td>
<td>–0.3</td>
<td>((V_{DD}+0.3))</td>
<td>V</td>
</tr>
<tr>
<td>Power dissipation, SOT-23 and SC70 packages</td>
<td>((T_J \text{ Max}–T_A)/R_{\theta JA})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead temperature, soldering</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vapor phase (60 s)</td>
<td>215</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Infrared (15 s)</td>
<td>220</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Junction temperature ((T_J \text{ Max}))</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature, (T_{\text{stg}})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{ESD}}) Electrostatic discharge</td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±3000</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±1000</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(T_A) Operating temperature</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>ADS7886</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{\theta JA}) Junction-to-ambient thermal resistance</td>
<td>113.4</td>
<td>149.6</td>
</tr>
<tr>
<td>(R_{\theta JC(top)}) Junction-to-case (top) thermal resistance</td>
<td>54.3</td>
<td>58.9</td>
</tr>
<tr>
<td>(R_{\theta JB}) Junction-to-board thermal resistance</td>
<td>35.3</td>
<td>41.9</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>4.6</td>
<td>1.5</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>35</td>
<td>41.3</td>
</tr>
<tr>
<td>(R_{\theta JC(bot)}) Junction-to-case (bottom) thermal resistance</td>
<td>n/a</td>
<td>n/a</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
7.5 Electrical Characteristics

+V_{DD} = 2.35 V to 5.25 V, T_{A} = –40°C to 125°C, f_{(sample)} = 1 MHz (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANALOG INPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full-scale input voltage span</td>
<td></td>
<td>0</td>
<td>V_{DD}</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Absolute input voltage range</td>
<td>+IN</td>
<td>–0.2</td>
<td>V_{DD}+0.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>C_{i}</td>
<td></td>
<td>21</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{iog}</td>
<td></td>
<td>40</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYSTEM PERFORMANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resolution</td>
<td></td>
<td>12</td>
<td>Bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>No missing codes</td>
<td></td>
<td>11</td>
<td>Bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INL</td>
<td></td>
<td>–1.25</td>
<td>±0.65</td>
<td>1.25</td>
<td>LSB</td>
</tr>
<tr>
<td>DNL</td>
<td></td>
<td>2</td>
<td></td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>E_{O}</td>
<td>V_{DD} = 2.35 V to 3.6 V</td>
<td>–2.5</td>
<td>±0.5</td>
<td>2.5</td>
<td>LSB</td>
</tr>
<tr>
<td>E_{O}</td>
<td>V_{DD} = 4.75 V to 5.25 V</td>
<td>–2</td>
<td>±0.5</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>E_{O}</td>
<td></td>
<td>–1.75</td>
<td>±0.5</td>
<td>1.75</td>
<td>LSB</td>
</tr>
<tr>
<td>SAMPLING DYNAMICS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conversion time</td>
<td>20-MHz SCLK</td>
<td>760</td>
<td>800</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Acquisition time</td>
<td></td>
<td>325</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Maximum throughput rate</td>
<td>20-MHz SCLK</td>
<td>1</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Aperture delay</td>
<td></td>
<td>5</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Step Response</td>
<td></td>
<td>160</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overvoltage recovery</td>
<td></td>
<td>160</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DYNAMIC CHARACTERISTICS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SNR</td>
<td>V_{DD} = 2.35 V to 3.6 V</td>
<td>69</td>
<td>71.25</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>SINAD</td>
<td>V_{DD} = 4.75 V to 5.25 V</td>
<td>70</td>
<td>72.25</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>THD</td>
<td>f_{i} = 100 kHz</td>
<td>–84</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>SFDR</td>
<td>f_{i} = 100 kHz</td>
<td>85.5</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Full power bandwidth</td>
<td>At –3 dB</td>
<td>15</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DIGITAL INPUT/OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic family — CMOS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{IH}</td>
<td>V_{DD} = 2.35 V to 3.6 V</td>
<td>1.8</td>
<td>5.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{IL}</td>
<td>V_{DD} = 3.6 V to 5.25 V</td>
<td>2.4</td>
<td>5.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{OH}</td>
<td>V_{DD} = 5 V</td>
<td></td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{OL}</td>
<td>V_{DD} = 3 V</td>
<td></td>
<td>0.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OH}</td>
<td>I_{(source)} = 200 µA</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{OL}</td>
<td>I_{(sink)} = 200 µA</td>
<td></td>
<td></td>
<td></td>
<td>0.4</td>
</tr>
</tbody>
</table>

(1) Ideal input span; does not include gain or offset error.
(2) See Figure 27 for details on the sampling circuit.
(3) LSB means least significant bit.
(4) Measured relative to an ideal full-scale input.
(5) Calculated on the first nine harmonics of the input frequency.
Electrical Characteristics (continued)

+V<sub>DD</sub> = 2.35 V to 5.25 V, T<sub>A</sub> = –40°C to 125°C, f<sub>(sample)</sub> = 1 MHz (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>+V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Supply voltage</td>
<td>2.35</td>
<td>3.3</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Supply current (normal mode)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 2.35 V to 3.6 V, 1-MHz throughput</td>
<td>1.3</td>
<td></td>
<td>1.5</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 4.75 V to 5.25 V, 1-MHz throughput</td>
<td>1.5</td>
<td></td>
<td>2</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 2.35 V to 3.6 V, static state</td>
<td></td>
<td></td>
<td>1.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 4.75 V to 5.25 V, static state</td>
<td></td>
<td></td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>Power down state supply current</td>
<td>SCLK off</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>SCLK on (20 MHz)</td>
<td></td>
<td></td>
<td></td>
<td>200 µA</td>
</tr>
<tr>
<td>Power dissipation at 1-MHz throughput</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3 V</td>
<td>3.9</td>
<td></td>
<td>4.5</td>
<td>mW</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5 V</td>
<td>7.5</td>
<td></td>
<td>10</td>
<td>mW</td>
</tr>
<tr>
<td>Power dissipation in static state</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3 V</td>
<td></td>
<td></td>
<td>3.3</td>
<td>mW</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5 V</td>
<td></td>
<td></td>
<td>7.5</td>
<td>mW</td>
</tr>
<tr>
<td>Power-up time</td>
<td></td>
<td></td>
<td></td>
<td>0.1</td>
<td>µs</td>
</tr>
<tr>
<td>Invalid conversions after power up or reset</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
7.6 Timing Requirements

All specifications typical at $T_A = -40^\circ C$ to 125$^\circ C$, $V_{DD} = 2.35$ V to 5.25 V (see Figure 1 and Figure 2) (unless otherwise specified)\(^{(1)}\).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{conv}$</td>
<td>Conversion time</td>
<td>$V_{DD} = 3$ V</td>
<td>$16 \times t_{SCLK}$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 5$ V</td>
<td>$16 \times t_{SCLK}$</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_q$</td>
<td>Minimum quiet time needed from bus 3-state to start of next conversion</td>
<td>$V_{DD} = 3$ V</td>
<td>40</td>
<td>40</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 5$ V</td>
<td>40</td>
<td>40</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{d1}$</td>
<td>Delay time, $\overline{CS}$ low to first data (0) out</td>
<td>$V_{DD} = 3$ V</td>
<td>15</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 5$ V</td>
<td>13</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
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<td>–2</td>
<td>5</td>
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\(^{(1)}\) 3-V Specifications apply from 2.35 V to 3.6 V, and 5-V specifications apply from 4.75 V to 5.25 V.

\(^{(2)}\) With 50-pf load.

---

**Figure 1. Interface Timing Diagram**
Figure 2. Entering Power Down Mode
### 7.7 Typical Characteristics

- **Figure 3. Supply Current vs Supply Voltage**
- **Figure 4. Supply Current vs SCLK Frequency**
- **Figure 5. Supply Current vs Sample Rate**
- **Figure 6. Analog Input Leakage Current vs Free-Air Temperature**
- **Figure 7. Signal-to-Noise Ratio vs Input Frequency**
- **Figure 8. Signal-to-Noise Ratio vs Supply Voltage**
Typical Characteristics (continued)

Figure 9. Signal-to-Noise Ratio vs Free-Air Temperature

Figure 10. Total Harmonic Distortion vs Input Frequency

Figure 11. Total Harmonic Distortion vs Supply Voltage

Figure 12. Total Harmonic Distortion vs Free-Air Temperature

Figure 13. Spurious Free Dynamic Range vs Input Frequency

Figure 14. Spurious Free Dynamic Range vs Supply Voltage
Typical Characteristics (continued)

Figure 15. Spurious Free Dynamic Range vs Supply Voltage

Figure 16. Offset Error vs Supply Voltage

Figure 17. Offset Error vs Free-Air Temperature

Figure 18. Gain Error vs Supply Voltage

Figure 19. Gain Error vs Free-Air Temperature

Figure 20. Differential Linearity Error vs Supply Voltage
Typical Characteristics (continued)

**Figure 21. Differential Nonlinearity vs Free-Air Temperature**

**Figure 22. Integral Nonlinearity vs Supply Voltage**

**Figure 23. Integral Nonlinearity vs Free-Air Temperature**

**Figure 24. DNL**

**Figure 25. INL**
Typical Characteristics (continued)

![Graph of FFT](image)

Figure 26. FFT

- $V_{DD} = 2.35\, V$
- $f_s = 1\, \text{MSPS}$
- $T_A = 25^\circ\, \text{C}$
- $f_1 = 100\, \text{kHz}$
- 8192 Points

```latex
V = 2.35\, V, \\
T = 1\, \text{MSPS}, \\
T_A = 25^\circ\, \text{C}, \\
f_1 = 100\, \text{kHz}, \\
8192\, \text{Points}
```
8 Detailed Description

8.1 Overview
The ADS7886 is 12-bit, 1-MSPS analog-to-digital converter (ADC). The device includes a capacitor-based SAR A/D converter with inherent sample and hold circuitry. The serial interface in device is controlled by the CS and SCLK signals for easy interface with microprocessors and DSPs. The input signal is sampled with the falling edge of CS, and SCLK is used for conversion and serial data output. The device operates from a wide supply range from 2.35 V to 5.25 V. The low power consumption of the device makes it suitable for battery-powered applications. The device also includes a power-saving, power-down feature which is useful when the device is operated at lower conversion speeds. The high level of the digital input to the device is not limited to device VDD. This means the digital input can go as high as 5.25 V when device supply is 2.35 V. This feature is useful when digital signals are coming from other circuit with different supply levels. This also relaxes the restrictions on power-up sequencing.

8.2 Functional Block Diagram

8.3 Feature Description

8.3.1 Driving the VIN and VDD Pins
The VIN input should be driven with a low impedance source. In most cases additional buffers are not required. In cases where the source impedance exceeds 200 Ω, using a buffer would help achieve the rated performance of the converter. The THS4031 is a good choice for the driver amplifier buffer.

The reference voltage for the A/D converter is derived from the supply voltage internally. The devices offer limited low-pass filtering functionality on-chip. The supply to these converters should be driven with a low impedance source and should be decoupled to the ground. A 1-µF storage capacitor and a 10-nF decoupling capacitor should be placed close to the device. Wide, low impedance traces should be used to connect the capacitor to the pins of the device. The ADS7886 draws very little current from the supply lines. The supply line can be driven by either:

- Directly from the system supply.
- A reference output from a low drift and low drop out reference voltage generator like REF3030 or REF3130. The ADS7886 operates from a wide range of supply voltages. The actual choice of the reference voltage generator would depend upon the system. Figure 33 shows one possible application circuit.
- A low-pass filtered system supply followed by a buffer, like the zero-drift OPA735, can also be used in cases where the system power supply is noisy. Care must be taken to ensure that the voltage at the VDD input does not exceed 7 V to avoid damage to the converter. This can be done easily using single supply CMOS amplifiers like the OPA735. Figure 34 shows one possible application circuit.
Feature Description (continued)

8.4 Device Functional Modes

8.4.1 Normal Operation

The cycle begins with the falling edge of CS. This point is indicated as a in Figure 1. With the falling edge of CS, the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains 4 leading zeros, followed by 12-bit data in MSB first format.

The falling edge of CS clocks out the first zero, and a zero is clocked out on every falling edge of the clock until the third edge. Data is in MSB first format with the MSB being clocked out on the 4th falling edge. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 16th falling edge of SCLK. The device enters the acquisition phase on the first rising edge of SCLK after the 13th falling edge. This point is indicated by b in Figure 1.

CS can be asserted (pulled high) after 16 clocks have elapsed. It is necessary not to start the next conversion by pulling CS low until the end of the quiet time \( t_{q} \) after SDO goes to 3-state. To continue normal operation, it is necessary that CS is not pulled high until point b. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle. (Also refer to power down mode for more details.) CS going high any time after the conversion start aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device \( V_{DD} \). This means the digital input can go as high as 5.25 V when the device supply is 2.35 V. This feature is useful when digital signals are coming from another circuit with different supply levels. Also, this relaxes the restriction on power up sequencing. However, the digital output levels \( V_{OH} \) and \( V_{OL} \) are governed by \( V_{DD} \) as listed in the Electrical Characteristics table.

8.4.2 Power Down Mode

The device enters power down mode if CS goes high anytime after the 2nd SCLK falling edge to before the 10th SCLK falling edge. Ongoing conversion stops and SDO goes to 3-state under this power down condition as shown in Figure 2.

A dummy cycle with CS low for more than 10 SCLK falling edges brings the device out of power down mode. For the device to come to the fully powered up condition it takes 1 \( \mu \)s. CS can be pulled high any time after the 10th falling edge as shown in Figure 28. It is not necessary to continue until the 16th clock if the next conversion starts 1 \( \mu \)s after CS going low of the dummy cycle and the quiet time \( t_{q} \) condition is met.

![Figure 27. Typical Equivalent Sampling Circuit](image)

![Figure 28. Exiting Power Down Mode](image)
### 9 Application and Implementation

**NOTE**
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 9.1 Application Information
The primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, reference driver circuit, and provides some application circuits designed for the ADS7886.

#### 9.2 Typical Application

![Typical Data Acquisition (DAQ) Circuit: Single-Supply DAQ](image)

**Figure 29.** Typical Data Acquisition (DAQ) Circuit: Single-Supply DAQ

**9.2.1 Design Requirements**
The goal of this application is to design a single-supply digital acquisition (DAQ) circuit based on the ADS7886 with SNR greater than 72.5 dB and THD less than –84 dB for input frequencies of 2 kHz to 100 kHz at a throughput of 1 MSPS.

**9.2.2 Detailed Design Procedure**
To achieve a SINAD of 61 dB, the operational amplifier must have high bandwidth to settle the input signal within the acquisition time of the ADC. The operational amplifier must have low noise to keep the total system noise below 20% of the input-referred noise of the ADC. For the application circuit shown in Figure 29, OPA365 is selected for its high bandwidth (50 MHz) and low noise (4.5 nV√Hz).

The reference voltage for the ADS7887 and ADS7888 A/D converters are derived from the supply voltage internally. The supply to these converters must be driven with a low impedance source and must be decoupled to the ground. To drive supply pin of ADS7887 ultra-low noise fast transient response low dropout voltage regulator TPS73201 is selected. Alternatively one can drive supply pin with low impedance voltage reference similar to REF3030.

For a step-by-step design procedure for low power, small form factor digital acquisition (DAQ) circuit based on similar SAR ADCs, see TI Precision Design, *Three 12-Bit Data Acquisition Reference Designs Optimized for Low Power and Ultra-Small Form Factor* (TIDU390).
9.2.3 Application Curves

Figure 30. Test Results for the ADS7886 and OPA365 for a 2-kHz Input

Figure 31. Test Results for the ADS7886 and OPA365 for a 100-kHz Input
10 Power Supply Recommendations

The reference voltage for the ADS7886 A/D converter is derived from the supply voltage internally. The supply to ADS7886 should be driven with a low impedance source and should be decoupled to the ground. Decouple the VDD with 1-µF ceramic decoupling capacitors, as shown in Figure 32. Always set the VDD supply to be greater than or equal to the maximum input signal to avoid saturation of codes.

![Figure 32. Supply/Reference Decoupling Capacitors](image)

Figure 32. Supply/Reference Decoupling Capacitors

![Figure 33. Using the REF3030 Reference](image)

Figure 33. Using the REF3030 Reference

![Figure 34. Buffering With the OPA735](image)

Figure 34. Buffering With the OPA735

11 Layout

11.1 Layout Guidelines

Figure 35 shows a board layout example for the ADS7886. Some of the key considerations are

1. Use a ground plane underneath the device and partition the PCB into analog and digital sections.
2. Avoid crossing digital lines with the analog signal path.
3. The power sources to the device must be clean and well-bypassed. Use 1-µF ceramic bypass capacitors in close proximity to the supply pin (VDD).
Layout Guidelines (continued)

4. Avoid placing vias between the VDD and bypass capacitors.
5. Connect ground pin to the ground plane using short, low-impedance path.
6. The fly-wheel RC filters are placed close to the device.

Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

11.2 Layout Example

![ADS7886 Layout Example](image-url)

Figure 35. ADS7886 Layout Example
12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- OPAx365 50-MHz, Zero-Crossover, Low-Distortion, High CMRR, RRI/O, Single-Supply Operational Amplifier (SBOS365)
- Cap-Free NMOS 250-mA Low Dropout Regulator With Reverse Current Protection (SGLS346)
- Three 12-Bit Data Acquisition Reference Designs Optimized for Low Power and Ultra-Small Form Factor (TIDU390)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community  TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support  TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

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(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

![Image of reel dimensions]

**Tape and Reel Information**

- **Device**: ADS7886SBDCKR
- **Package Type**: SC70
- **Drawing**: DCK
- **Pins**: 6
- **SPQ**: 3000
- **Reel Diameter**: 177.8 mm
- **Reel Width**: 9.7 mm
- **A0**: 2.3 mm
- **B0**: 2.52 mm
- **K0**: 1.2 mm
- **P1**: 4.0 mm
- **W**: 8.0 mm
- **Pin1 Quadrant**: Q3

**Device**: ADS7886SBDCKT

- **Package Type**: SC70
- **Drawing**: DCK
- **Pins**: 6
- **SPQ**: 250
- **Reel Diameter**: 177.8 mm
- **Reel Width**: 9.7 mm
- **A0**: 2.3 mm
- **B0**: 2.52 mm
- **K0**: 1.2 mm
- **P1**: 4.0 mm
- **W**: 8.0 mm
- **Pin1 Quadrant**: Q3

**Device**: ADS7886SDCKR

- **Package Type**: SC70
- **Drawing**: DCK
- **Pins**: 6
- **SPQ**: 3000
- **Reel Diameter**: 177.8 mm
- **Reel Width**: 9.7 mm
- **A0**: 2.3 mm
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- **W**: 8.0 mm
- **Pin1 Quadrant**: Q3

**Device**: ADS7886SDCKT

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- **A0**: 2.3 mm
- **B0**: 2.52 mm
- **K0**: 1.2 mm
- **P1**: 4.0 mm
- **W**: 8.0 mm
- **Pin1 Quadrant**: Q3

*All dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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<td>50.0</td>
</tr>
</tbody>
</table>
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.  
D. Falls within JEDEC MO-203 variation AB.
DCK (R-PDSO-G6)  PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness of .127mm (.005inch).

6x0,35
0,85
2,2

2x1,30
4x0,65

Solder Mask Opening

PbD Geometry

0,4
1,0
0,9

0,05
0,50

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7528 for other stencil recommendations.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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