**FEATURES**

- **HIGH SNR**: 49dB
- **INTERNAL OR EXTERNAL REFERENCE OPTION**
- **SINGLE-ENDED OR DIFFERENTIAL ANALOG INPUT**
- **PROGRAMMABLE INPUT RANGE**: 1Vp-p / 2Vp-p
- **LOW POWER**: 275mW
- **LOW DNL**: 0.35LSB
- **SINGLE +5V SUPPLY OPERATION**
- **SSOP-20 PACKAGE**

**APPLICATIONS**

- **MEDICAL IMAGING**
- **VIDEO DIGITIZING**
- **COMPUTER SCANNERS**
- **COMMUNICATIONS**
- **DISK-DRIVE CONTROL**

**DESCRIPTION**

The ADS831 is a pipeline, CMOS Analog-to-Digital (A/D) converter that operates from a single +5V power supply. This converter provides excellent performance with a single-ended input and can be operated with a differential input for added spurious performance. This high performance converter includes an 8-bit quantizer, high bandwidth track/hold, and a high accuracy internal reference. It also allows for the user to disable the internal reference and utilize external references. This external reference option provides excellent gain and offset matching when used in multi-channel applications or in applications where DC full scale range adjustment is required.

The ADS831 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for medical imaging, communications, video, and test instrumentation.

The ADS831 is specified at a maximum sampling frequency of 80MHz and a single-ended input range of 1.5V to 3.5V. The ADS831 is available in an SSOP-20 package and is pin-for-pin compatible with the 8-bit, 60MHz ADS830.
ABSOLUTE MAXIMUM RATINGS

+V S ................................................................. +6V
Analog Input .............................................. –0.3V to (+V S + 0.3V)
Logic Input .................................................. –0.3V to (+V S + 0.3V)
Case Temperature ......................................... +100°C
Junction Temperature .................................. +150°C
Storage Temperature ..................................... +150°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEMO BOARD ORDERING INFORMATION

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>DEMO BOARD</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS831</td>
<td>DEM-ADS831E</td>
</tr>
</tbody>
</table>

PACKAGE/ORDERING INFORMATION

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>PACKAGE</th>
<th>PACKAGE DRAWING NUMBER(1)</th>
<th>SPECIFIED TEMPERATURE RANGE</th>
<th>PACKAGE MARKING</th>
<th>ORDERING NUMBER</th>
<th>TRANSPORT MEDIA</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS831E</td>
<td>SSOP-20 (QSOP)</td>
<td>349</td>
<td>–40°C to +85°C</td>
<td>ADS831E</td>
<td>ADS831E</td>
<td>Rails</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ADS831E/1K</td>
<td>Tape and Reel</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of “ADS831E/1K” will get a single 1000-piece Tape and Reel.

ELECTRICAL CHARACTERISTICS

At T A = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 80MHz, and external reference, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>ADS831E</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>SPECIFIED TEMPERATURE RANGE</td>
<td>Ambient Air</td>
<td>–40 to +85</td>
</tr>
<tr>
<td>RESOLUTION</td>
<td>8 Guaranteed Bits</td>
<td></td>
</tr>
<tr>
<td>ANALOG INPUT</td>
<td>Standard Single-Ended Input Range</td>
<td>2Vp-p</td>
</tr>
<tr>
<td></td>
<td>Optional Single-Ended Input Range</td>
<td>1Vp-p</td>
</tr>
<tr>
<td></td>
<td>Common-Mode Voltage</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Optional Differential Input Range</td>
<td>2Vp-p</td>
</tr>
<tr>
<td></td>
<td>Analog Input Bias Current</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Track-Mode Input Bandwidth</td>
<td>–3dBFS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>300</td>
</tr>
</tbody>
</table>

CONVERSION CHARACTERISTICS

| Sample Rate | 10k     | 4  |
| Data Latency | 80M Samples/s |

DYNAMIC CHARACTERISTICS

Differential Linearity Error (largest code error)

f = 1MHz
f = 10MHz
No Missing Codes
Integral Nonlinearity Error, f = 1MHz
Spurious Free Dynamic Range(1)

f = 1MHz (~1dB input)

f = 10MHz (~1dB input)

Two-Tone Intermodulation Distortion(3)

f = 9.5MHz and 9.9MHz (~1dB each tone)

Signal-to-Noise Ratio (SNR)

f = 1MHz
f = 10MHz

Signal-to-(Noise + Distortion) (SINAD)

f = 1MHz
f = 10MHz

Effective Number of Bits(4), f = 1MHz

Output Noise

Input Tied to Common-Mode

Aperture Delay Time

Aperture Jitter

Overvoltage Recovery Time

Full-Scale Step Acquisition Time

Texas Instruments  ADS831  SBA087A
ELECTRICAL CHARACTERISTICS (Cont.)

At \( T_A = \) full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 80MHz, and external reference, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>ADS831E</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
</tr>
<tr>
<td>DIGITAL INPUTS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Family</td>
<td>Start Conversion</td>
<td>CMOS Compatible</td>
</tr>
<tr>
<td>Convert Command</td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>High Level Input Current(^{(5)}) ((V_{IN} = 5V))</td>
<td>+3.5</td>
<td>+1.0</td>
</tr>
<tr>
<td>Low Level Input Current ((V_{IN} = 0V))</td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Level Input Voltage</td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>Low Level Input Voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DIGITAL OUTPUTS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Family</td>
<td></td>
<td>CMOS/TTL Compatible</td>
</tr>
<tr>
<td>Logic Coding</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low Output Voltage ((I_{OL} = 50µA)) (V_{DRV} = 5V)</td>
<td>+0.1</td>
<td>+0.2</td>
</tr>
<tr>
<td>Low Output Voltage ((I_{OL} = 1.6mA)) (V_{DRV} = 5V)</td>
<td>+4.9</td>
<td>+4.8</td>
</tr>
<tr>
<td>High Output Voltage ((I_{OH} = 50µA)) (V_{DRV} = 3V)</td>
<td>+2.8</td>
<td>+2.0</td>
</tr>
<tr>
<td>High Output Voltage ((I_{OH} = 0.5mA)) (V_{DRV} = 3V)</td>
<td>+4.9</td>
<td>+4.8</td>
</tr>
<tr>
<td>Low Output Voltage ((I_{OL} = 50µA)) (V_{DRV} = 3V)</td>
<td>+2.8</td>
<td>+2.0</td>
</tr>
<tr>
<td>High Output Voltage ((I_{OH} = 0.5mA)) (V_{DRV} = 3V)</td>
<td>+4.9</td>
<td>+4.8</td>
</tr>
<tr>
<td>Output Capacitance</td>
<td></td>
<td>5</td>
</tr>
</tbody>
</table>

ACCURACY (Internal Reference, 2Vp-p, Unless Otherwise Noted)

<table>
<thead>
<tr>
<th></th>
<th>( f_s = 2.5\text{MHz} )</th>
<th>25°C</th>
<th>25°C</th>
<th>25°C</th>
<th>25°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zero Error (Referred to (–)FS)</td>
<td>( ±0.5 )</td>
<td>±53</td>
<td>±0.5</td>
<td>±50</td>
<td>ppm/C</td>
</tr>
<tr>
<td>Gain Error*</td>
<td>( ±75 )</td>
<td>±53</td>
<td>±75</td>
<td>±50</td>
<td>ppm/C</td>
</tr>
<tr>
<td>Gain Error Drift*</td>
<td>( ±75 )</td>
<td>±53</td>
<td>±75</td>
<td>±50</td>
<td>ppm/C</td>
</tr>
<tr>
<td>Power Supply Rejection of Gain</td>
<td>( 3.0\text{V} )</td>
<td>±10</td>
<td>±100</td>
<td>±100</td>
<td>mV</td>
</tr>
<tr>
<td>Internal REF Tolerance</td>
<td>( 2.0\text{V} )</td>
<td>±10</td>
<td>±100</td>
<td>±100</td>
<td>mV</td>
</tr>
<tr>
<td>External REF Voltage Range</td>
<td>( \text{REFB} + 0.8 )</td>
<td>±10</td>
<td>±100</td>
<td>±100</td>
<td>mV</td>
</tr>
<tr>
<td>External REF Voltage Range</td>
<td>( 1.25 )</td>
<td>3.0</td>
<td>( V_{REF} – 1.25 )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Reference Input Resistance</td>
<td>( 0.8 )</td>
<td>2.0</td>
<td>REF ( – 0.8 )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Resistance to REF</td>
<td>REFT to REF</td>
<td>800</td>
<td>800</td>
<td>800</td>
<td>Ω</td>
</tr>
</tbody>
</table>

POWER SUPPLY REQUIREMENTS

<table>
<thead>
<tr>
<th></th>
<th>( +V_{S} )</th>
<th>( +I_{S} )</th>
<th>( \Delta V_{S} )</th>
<th>( %V_{S} )</th>
<th>( %V_{S} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage: ( +V_{S} )</td>
<td>( +4.75 )</td>
<td>58</td>
<td>70</td>
<td>mA</td>
<td>mA</td>
</tr>
<tr>
<td>Supply Current: ( +I_{S} )</td>
<td>( 350 )</td>
<td>285</td>
<td>285</td>
<td>mW</td>
<td>mW</td>
</tr>
<tr>
<td>Power Dissipation: ( V_{DRV} = 5V )</td>
<td>( 290 )</td>
<td>275</td>
<td>275</td>
<td>mW</td>
<td>mW</td>
</tr>
<tr>
<td>( V_{DRV} = 3V )</td>
<td>( 310 )</td>
<td>310</td>
<td>310</td>
<td>mW</td>
<td>mW</td>
</tr>
<tr>
<td>( V_{DRV} = 5V )</td>
<td>( 3	ext{V} )</td>
<td>3	ext{V}</td>
<td>3	ext{V}</td>
<td>mW</td>
<td>mW</td>
</tr>
<tr>
<td>( \Delta V_{S} )</td>
<td>( ±150 )</td>
<td>±150</td>
<td>±150</td>
<td>mW</td>
<td>mW</td>
</tr>
<tr>
<td>Thermal Resistance, ( \theta_{JA} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSOP-20</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NOTES:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full Scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by ( (\text{SINAD} – 1.76) /6.02 ). (5) A 50kΩ pull-down resistor is inserted internally. (6) Excludes internal reference.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**TIMING DIAGRAM**

- **tCONV**: Convert Clock Period
- **tL**: Clock Pulse Low
- **tH**: Clock Pulse High
- **tD**: Aperture Delay
- **t1**: Data Hold Time, \( C_L = 0 \text{pF} \)
- **t2**: New Data Delay Time, \( C_L = 15 \text{pF} \) max

**SYMBOL**

- **tCONV**: Convert Clock Period
- **tL**: Clock Pulse Low
- **tH**: Clock Pulse High
- **tD**: Aperture Delay
- **t1**: Data Hold Time, \( C_L = 0 \text{pF} \)
- **t2**: New Data Delay Time, \( C_L = 15 \text{pF} \) max

**TIMING SPECIFICATIONS**

- **tCONV**: 12.5 to 100 \( \mu \)s
- **tL**: 5.8 to 6.25 ns
- **tH**: 5.8 to 6.25 ns
- **tD**: 3 ns
- **t1**: 3.9 ms
- **t2**: 5.9 to 12 ns

**PIN DESCRIPTIONS**

- **PIN**: 1
  - **DESIGNATOR**: GND
  - **DESCRIPTION**: Ground
- **PIN**: 2
  - **DESIGNATOR**: Bit 1
  - **DESCRIPTION**: Data Bit 1 (D7) (MSB)
- **PIN**: 3
  - **DESIGNATOR**: Bit 2
  - **DESCRIPTION**: Data Bit 2 (D6)
- **PIN**: 4
  - **DESIGNATOR**: Bit 3
  - **DESCRIPTION**: Data Bit 3 (D5)
- **PIN**: 5
  - **DESIGNATOR**: Bit 4
  - **DESCRIPTION**: Data Bit 4 (D4)
- **PIN**: 6
  - **DESIGNATOR**: Bit 5
  - **DESCRIPTION**: Data Bit 5 (D3)
- **PIN**: 7
  - **DESIGNATOR**: Bit 6
  - **DESCRIPTION**: Data Bit 6 (D2)
- **PIN**: 8
  - **DESIGNATOR**: Bit 7
  - **DESCRIPTION**: Data Bit 7 (D1)
- **PIN**: 9
  - **DESIGNATOR**: Bit 8
  - **DESCRIPTION**: Data Bit 8 (D0) (LSB)
- **PIN**: 10
  - **DESIGNATOR**: CLK
  - **DESCRIPTION**: Convert Clock
- **PIN**: 11
  - **DESIGNATOR**: RSEL
  - **DESCRIPTION**: Input Range Select: HI = 2V; LO = 1V
- **PIN**: 12
  - **DESIGNATOR**: INT/EXT
  - **DESCRIPTION**: Reference Select: HI = External; LO = Internal
- **PIN**: 13
  - **DESIGNATOR**: REFT
  - **DESCRIPTION**: Top Reference
- **PIN**: 14
  - **DESIGNATOR**: REFB
  - **DESCRIPTION**: Bottom Reference
- **PIN**: 15
  - **DESIGNATOR**: CM
  - **DESCRIPTION**: Common-Mode Voltage Output
- **PIN**: 16
  - **DESIGNATOR**: IN
  - **DESCRIPTION**: Complementary Input
- **PIN**: 17
  - **DESIGNATOR**: Analog Input
- **PIN**: 18
  - **DESIGNATOR**: GND
  - **DESCRIPTION**: Ground
- **PIN**: 19
  - **DESIGNATOR**: +VSS
  - **DESCRIPTION**: +5V Supply
- **PIN**: 20
  - **DESIGNATOR**: VDRV
  - **DESCRIPTION**: Output Logic Driver Supply Voltage
TYPICAL CHARACTERISTICS
At $T_a$ = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 80MHz, and external reference, unless otherwise noted.
TYPICAL CHARACTERISTICS (Cont.)

At $T_A$ = full specified temperature range, single-ended input range = 1.5V to 3.5V, sampling rate = 80MHz, and external reference, unless otherwise noted.
APPLICATION INFORMATION

THEORY OF OPERATION

The ADS831 is a high-speed CMOS A/D converter which employs a pipelined converter architecture consisting of 6 internal stages. Each stage feeds its data into the digital error correction logic ensuring excellent differential linearity and no missing codes at the 8-bit level. The output data becomes valid on the rising clock edge (see Timing Diagram). The pipeline architecture results in a data latency of 4 clock cycles.

The analog input of the ADS831 is a differential track and hold, as shown in Figure 1. The differential topology along with tightly matched capacitors produce a high level of ac performance while sampling at very high rates.

The ADS831 allows its analog inputs to be driven either single-ended or differentially. The typical configuration for the ADS831 is for the single-ended mode in which the input track and hold performs a single-ended to differential conversion of the analog input signal.

Both inputs (IN, IN) require external biasing using a common-mode voltage that is typically at the mid-supply level (+Vs/2).

The following application discussion focuses on the single-ended configuration. Typically, its implementation is easier to achieve and the rated specifications for the ADS831 are characterized using the single-ended mode of operation.

DRIVING THE ANALOG INPUT

The ADS831 achieves excellent ac performance either in the single-ended or differential mode of operation. The selection for the optimum interface configuration will depend on the individual application requirements and system structure. For example, communication applications often process a band of frequencies that does not include DC, whereas in imaging applications, the previously restored DC level must be maintained correctly up to the A/D converter. Features on the ADS831, such as the input range select (RSEL pin) or the option for an external reference, provide the needed flexibility to accommodate a wide range of applications. In any case, the ADS831 should be configured such that the application objectives are met while observing the headroom requirements of the driving amplifier in order to yield the best overall performance.

INPUT CONFIGURATIONS

AC-Coupled, Single-Supply Interface

Figure 2 shows the typical circuit for an ac-coupled analog input configuration of the ADS831 where all components are powered from a single +5V supply.

With the RSEL pin connected HIGH, the full scale input range is set to 2Vp-p. In this configuration, the top and bottom references (REFT, REFB) provide an output voltage of +3.0V and +2.0V, respectively. Two resistors (2 x 1kΩ) are used to create a common-mode voltage (V_CM) of approximately +2.5V to bias the inputs of the driving amplifier. Using the OPA681 on a single +5V supply, its ideal common-mode point is +2.5V. This coincides with the recommended common-mode input level for the ADS831 thus, obviating the need for a coupling capacitor between the amplifier and the converter. Even though the OPA681 has an ac gain of +2, the dc gain is only +1 due to the blocking capacitor at resistor RG.

The addition of a small series resistor (R_S) between the output of the op amp and the input of the ADS831 will be beneficial in almost all interface configurations. This will de-couple the op amp’s output from the capacitive load and avoid gain peaking, which can result in increased noise. For best spurious and distortion performance, the resistor value should be kept below 750Ω. The series resistor in combination with the 47pF capacitor establishes a passive low-pass filter limiting the bandwidth for the wideband noise thus help improving the SNR performance.

AC-Coupled, Dual Supply Interface

The circuit provided in Figure 3 shows typical connections for the analog input in case the selected amplifier operates on dual supplies. This will de-couple the op amp’s output from the capacitive load and avoid gain peaking, which can result in increased noise. For best spurious and distortion performance, the resistor value should be kept below 750Ω. The series resistor in combination with the 47pF capacitor establishes a passive low-pass filter limiting the bandwidth for the wideband noise thus help improving the SNR performance.

FIGURE 1. Simplified Circuit of Input Track and Hold with Timing Diagram.
For applications requiring the driving amplifier to provide a signal amplification with a gain $\geq 5$, consider using uncompensated voltage feedback op amps, such as the OPA643, or current feedback op amps OPA681 and OPA658.

**DC-Coupled with Level Shift**

Several applications may require that the bandwidth of the signal path includes DC, in which case the signal has to be DC-coupled to the A/D converter. In order to accomplish this, the interface circuit has to provide a DC level shift to the analog input signal. The circuit shown in Figure 4 employs a dual op amp, A1, to drive the input of the ADS831 and level shift the signal to be compatible with the selected input range. With the RSEL pin tied to the supply and the INT/EXT pin to ground, the ADS831 is configured for a 2Vp-p input range and uses the internal references. The complementary input ($\overline{\text{IN}}$) may be appropriately biased using the $+2.5V$ common-mode voltage available at the CM pin. One-half of the amplifier (OPA2681) buffers the REFB pin and drives the voltage divider $R_1$, $R_2$. Because of the op amp’s noise gain of $+2V/V$, assuming $R_F = R_{IN}$, the common-mode voltage ($V_{CM}$) has to be rescaled to $+1.25V$, resulting in the correct DC level of $+2.5V$ for the signal input (IN). Any DC voltage differences between the IN and $\overline{\text{IN}}$ inputs of the ADS831 effectively produce an offset, which can be corrected for by adjusting the resistor values of the divider, $R_1$ and $R_2$. The selection criteria for a suitable op amp should include the supply voltage, input bias current, output voltage swing, distortion, and noise specification. Note that in this example the overall signal phase is inverted. To re-establish the original signal polarity, it is always possible to interchange the IN and $\overline{\text{IN}}$ connections.
SINGLE ENDED-TO-DIFFERENTIAL CONFIGURATION
(Transformer Coupled)

If the application requires a signal conversion from a single-ended source to feed the ADS831 differentially, a RF transformer might be a good solution. The selected transformer must have a center tap in order to apply the common-mode DC voltage necessary to bias the converter inputs. AC grounding the center tap will generate the differential signal swing across the secondary winding. Consider a step-up transformer to take advantage of a signal amplification without the introduction of another noise source. Furthermore, the reduced signal swing from the source may lead to an improved distortion performance.

The differential input configuration may provide a noticeable advantage of achieving good SFDR performance over a wide range of input frequencies. In this mode both inputs of the ADS831 see closely matched impedances, and the differential signal swing is reduced to half of the swing required for single-ended drive. Figure 5 shows the schematic for the suggested transformer coupled interface circuit. The component values of the R-C lowpass may be optimized depending on the desired roll-off frequency. The resistor across the secondary side (R_{T}) should be calculated using the equation \( R_T = n^2 \times R_S \) to match the source impedance (R_{G}) for good power transfer and VSWR.

REFERENCE OPERATION

Figure 6 depicts the simplified model of the internal reference circuit. The internal blocks are the bandgap voltage reference, the drivers for the top and bottom reference, and

![Diagram](image-url)
the resistive reference ladder. The bandgap reference circuit includes logic functions that allow to set the analog input swing of the ADS831 to either a 1Vp-p or 2Vp-p full-scale range simply by tying the RSEL pin to a LOW or HIGH potential, respectively. While operating the ADS831 in the external reference mode, the buffer amplifiers for REFT and REFB are disconnected from the reference ladder.

As shown, the ADS831 has internal 50kΩ pull-up resistors at the Range Select pin (RSEL) and Reference Select pin (INT/EXT). Leaving those pins open configures the ADS831 for a 2Vp-p input range and external reference operation. Setting the ADS831 up for internal reference mode requires to bring the INT/EXT pin LOW.

The reference buffers can be utilized to supply up to 1mA (sink and source) to external circuitry. To ensure proper operation with any reference configurations, it is necessary to provide solid bypassing at the reference pins in order to keep the clock feedthrough to a minimum (Figure 6). All bypassing capacitors should be located as close to their respective pins as possible.

FIGURE 7. Alternative Circuit to Generate Common-Mode Voltage.

The common-mode voltage available at the CM pin may be used as a bias voltage to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this node, which is not buffered and has a high impedance. An alternative way of generating a common-mode voltage is given in Figure 7. Here, two external precision resistors (1% tolerance or better) are located between the top and bottom reference pins. The common-mode voltage, CMV, will appear at the midpoint.

EXTERNAL REFERENCE OPERATION

For even more design flexibility, the internal reference can be disabled and an external reference voltage be used. The utilization of an external reference may be considered for applications requiring higher accuracy, improved temperature performance, or a wide adjustment range of the converter’s full-scale range. Especially in multichannel applications, the use of a common external reference has the benefit of obtaining better matching of the full-scale range between converters.

The external references can vary as long as the value of the external top reference REFT\textsubscript{EXT} stays within the range of \((V_S - 1.25V)\) and \((REFB + 0.8V)\), and the external bottom reference REFB\textsubscript{EXT} stays within 1.25V and \((REFT - 0.8V)\), as shown in Figure 8.

The full-scale input signal range (FSR) of the ADS831 is determined by the voltage difference across the reference pins REFT and REFB (FSR = REFT − REFB), while the common-mode voltage is defined by CMV = (REFT + REFB)/2. In order to maintain good ac performance, it is recommended that the typical common-mode voltage be kept at +2.5V while setting the external reference voltages. It is possible, however, to deviate from this common-mode level without significantly impacting the performance. In particular, DC-coupled applications may benefit from a lower CMV as it increases the signal headroom of the

driving amplifier. The internal reference ladder has a nominal impedance of 800Ω. Depending on the selected reference voltages, the required drive current will vary accordingly and the external reference circuitry should be designed to supply the maximum required current.

DIGITAL INPUTS AND OUTPUTS
Clock Input Requirements
Clock jitter is critical to the SNR performance of high speed, high resolution Analog to Digital Converters. It leads to aperture jitter (tA) which adds noise to the signal being converted. The ADS831 samples the input signal on the rising edge of the CLK input. Therefore, this edge should have the lowest possible jitter. The jitter noise contribution to total SNR is given by the following equation. If this value is near your system requirements, input clock jitter must be reduced.

\[ \text{Jitter SNR} = 20 \log \frac{1}{2 \pi f_{IN} t_A} \text{ rms signal to rms noise} \]

Where: \( f_{IN} \) is Input Signal Frequency
\( t_A \) is rms Clock Jitter

Particularly in undersampling applications, special consideration should be given to clock jitter. The clock input should be treated as an analog input in order to achieve the highest level of performance. Any overshoot or undershoot of the clock signal may cause degradation of the performance. When digitizing at high sampling rates, the clock should have a 50% duty cycle (tH = tL), along with fast rise and fall times of 2ns or less.

Digital Outputs
The output data format of the ADS831 is in positive Straight Offset Binary code, see Table I. This format can easily be converted into the Two’s Binary Complement code by inverting the MSB.

<table>
<thead>
<tr>
<th>SINGLE-ENDED INPUT (2Vp-p) ((IN = CMV))</th>
<th>STRAIGHT OFFSET BINARY ((SOB))</th>
</tr>
</thead>
<tbody>
<tr>
<td>+FS (IN = +3.5V)</td>
<td>1111 1111</td>
</tr>
<tr>
<td>+1/2 FS</td>
<td>1100 0000</td>
</tr>
<tr>
<td>+1LSB</td>
<td>1000 0001</td>
</tr>
<tr>
<td>Bipolar Zero (IN = 2.5V)</td>
<td>1000 0000</td>
</tr>
<tr>
<td>-1LSB</td>
<td>0111 1111</td>
</tr>
<tr>
<td>-1/2 FS</td>
<td>0100 0000</td>
</tr>
<tr>
<td>-FS (IN = +1.5V)</td>
<td>0000 0000</td>
</tr>
</tbody>
</table>

TABLE I. Coding Table for the ADS831.

It is recommended to keep the capacitive loading on the data lines as low as possible (≤ 15pF). Higher capacitive loading will cause larger dynamic currents as the digital outputs are changing. Those high current surges can feed back to the analog portion of the ADS831 and affect the performance. If necessary, external buffers or latches close to the converter’s output pins may be used to minimize the capacitive loading. They also provide the added benefit of isolating the ADS831 from any digital noise activities on the bus coupling back high frequency noise.

Digital Output Driver (VDRV)
The ADS831 features a dedicated supply pin for the output logic drivers, VDRV, which is not internally connected to the other supply pins. Setting the voltage at VDRV to ±5V or ±3V the ADS831 produces corresponding logic levels and can directly interface to the selected logic family. The output stages are designed to supply sufficient current to drive a variety of logic families. However, it is recommended to use the ADS831 with ±3V logic supply. This will lower the power dissipation in the output stages due to the lower output swing and reduce current glitches on the supply line which may affect the ac performance of the converter. In some applications, it might be advantageous to decouple the VDRV pin with additional capacitors or a pi-filter.

GROUNDING AND DECOUPLING
Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high frequency designs. Multilayer PC boards are recommended for best performance since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc. The ADS831 should be treated as an analog component. Whenever possible, the supply pins should be powered by the analog supply. This will ensure the most consistent results since digital supply lines often carry high levels of noise which otherwise would be coupled into the converter and degrade the achievable performance. All ground connections on the ADS831 are internally joined together, obviating the design of split ground planes. The ground pins (1, 18) should directly connect to an analog ground plane which covers the PC board area around the converter. While designing the layout, it is important to keep the analog signal traces separated from any digital lines to prevent noise coupling onto the analog signal path. Because of its high sampling rate, the ADS831 generates high frequency current transients and noise (clock feedthrough) that are fed back into the supply and reference lines. This requires that all supply and reference pins are sufficiently bypassed. Figure 9 shows the recommended decoupling scheme for the ADS831. In most cases, 0.1µF ceramic chip capacitors at each pin are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close to the supply pins as possible. In addition, a larger bipolar capacitor (1µF to 22µF) should be placed on the PC board in proximity of the converter circuit.

![Figure 9. Recommended Bypassing for the Supply Pins.](image-url)
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS831E</td>
<td>ACTIVE</td>
<td>SSOP</td>
<td>DBQ</td>
<td>20</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>ADS831E</td>
<td>Ads831e</td>
</tr>
<tr>
<td>ADS831E/2K5</td>
<td>ACTIVE</td>
<td>SSOP</td>
<td>DBQ</td>
<td>20</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>ADS831E</td>
<td>Ads831e</td>
</tr>
</tbody>
</table>

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(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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Addendum-Page 1
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### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### REEL DIMENSIONS

- Reel Diameter
- Reel Width (W1)

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#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- Sprocket Holes
- User Direction of Feed
- Pocket Quadrants

---

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS831E/2K5</td>
<td>SSOP</td>
<td>DBQ</td>
<td>20</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>9.0</td>
<td>2.1</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

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www.ti.com 26-Feb-2019
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS831E/2K5</td>
<td>SSOP</td>
<td>DBQ</td>
<td>20</td>
<td>2500</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
</tbody>
</table>
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