20 MHz, Second-Order, Isolated Delta-Sigma Modulator for Current-Shunt Measurement

Check for Samples: AMC1204-Q1

**FEATURES**

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- ±250-mV Input Voltage Range Optimized for Shunt Resistors
- Certified Digital Isolation:
  - CSA, IEC60747-5-2, and UL1577 Approved
  - Isolation Voltage: 4250 V
  - Working Voltage: 1200 V
  - Transient Immunity: 15 kV/µs
- Long Isolation Barrier Lifetime (see Application Report SLLA197)
- High Electromagnetic Field Immunity (see Application Note SLLA181A)
- Excellent DC Precision:
  - INL: ±8 LSB (max)
  - Gain Error: ±2.5% (max)
- External Clock Input for Easier Synchronization
- Fully Specified Over the Extended Automotive Temperature Range

**APPLICATION**

- Shunt Resistor Based Current Sensing in:
  - Motor Control
  - Inverter Applications
  - Uninterruptible Power Supplies

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**DESCRIPTION**

The AMC1204-Q1 is a 1-bit digital output, isolated delta-sigma (ΔΣ) modulators that can be clocked at up to 20 MHz. The digital isolation of the modulator output is provided by a silicon dioxide (SiO2) barrier that is highly resistant to magnetic interference. This barrier has been certified to provide basic galvanic isolation of up to 4250 Vpeak according to UL1577, IEC60747-5-2, and CSA standards or specifications.

The AMC1204-Q1 provides a single-chip solution for measuring the small signal of a shunt resistor across an isolated barrier. These types of resistors are typically used to sense currents in motor control inverters, green energy generation systems, and other industrial applications. The AMC1204-Q1 differential inputs easily connect to the shunt resistor or other low-level signal sources. An internal reference eliminates the need for external components. When used with an appropriate external digital filter, an effective number of bits (ENOB) of 14 is achieved at a data rate of 78 kSPS.

A 5-V analog supply (AVDD) is used by the modulator while the isolated digital interface operates from a 3-V, 3.3-V, or 5-V supply (DVDD). The AMC1204-Q1 is available in SO-16 (DW) packages and are specified from –40°C to 125°C.
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

<table>
<thead>
<tr>
<th>ORDERABLE</th>
<th>MODULATOR CLOCK (MHz)</th>
<th>DIGITAL SUPPLY</th>
<th>CLOCK SOURCE</th>
<th>GAIN ERROR (%)</th>
<th>THD (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMC1204QDWRQ1</td>
<td>20</td>
<td>3 V, 3.3 V, or 5 V</td>
<td>External</td>
<td>±8</td>
<td>±2.5</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com

ABSOLUTE MAXIMUM RATINGS(1)

Over the operating ambient temperature range, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, AVDD to AGND or DVDD to DGND</td>
<td>−0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Analog input voltage at VINP, VINN</td>
<td>AGND − 0.5</td>
<td>AVDD + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>Digital input voltage at CLKIN</td>
<td>DGND − 0.3</td>
<td>DVDD + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Input current to any pin except supply pins</td>
<td>−10</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Maximum virtual junction temperature, TJ</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Operating ambient temperature range, TOA</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Electrostatic discharge (ESD), all pins</td>
<td>−2000</td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>Human body model (HBM) AEC-Q100 Classification Level H2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Charged device model (CDM) AEC-Q100 Classification Level C3B</td>
<td>−750</td>
<td>750</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>AMC1204-Q1 DW (16 PINS)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \theta_{JA} )</td>
<td>Junction-to-ambient thermal resistance</td>
<td>78.5</td>
</tr>
<tr>
<td>( \theta_{Jc} )</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>41.3</td>
</tr>
<tr>
<td>( \theta_{JB} )</td>
<td>Junction-to-board thermal resistance</td>
<td>50.2</td>
</tr>
<tr>
<td>( \psi_{JT} )</td>
<td>Junction-to-top characterization parameter</td>
<td>11.5</td>
</tr>
<tr>
<td>( \psi_{JB} )</td>
<td>Junction-to-board characterization parameter</td>
<td>41.2</td>
</tr>
<tr>
<td>( \theta_{JC} )</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>n/a</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
REGULATORY INFORMATION

<table>
<thead>
<tr>
<th>VDE/IEC</th>
<th>CSA</th>
<th>UL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Certified according to IEC 60747-5-2</td>
<td>Approved under CSA component acceptance notice</td>
<td>Recognized under 1577 component recognition program</td>
</tr>
<tr>
<td>File number: 40016131</td>
<td>File number: 2350550</td>
<td>File number: E181974</td>
</tr>
</tbody>
</table>

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O circuitry can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

The safety-limiting constraint is the operating virtual junction temperature range specified in the Absolute Maximum Ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determine the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Information table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_S$</td>
<td>Safety input, output, or supply current</td>
<td>10</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_C$</td>
<td>Maximum case temperature</td>
<td>150</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

IEC 61000-4-5 RATINGS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IOSM}$</td>
<td>Surge immunity 1.2/50 μs voltage surge and 8/20 μs current surge</td>
<td>±6000</td>
<td>V</td>
</tr>
</tbody>
</table>

IEC 60664-1 RATINGS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>SPECIFICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic isolation group</td>
<td>Material group</td>
<td>II</td>
</tr>
<tr>
<td>Installation classification</td>
<td>Rated mains voltage $\leq 150 V_{RMS}$</td>
<td>I-IV</td>
</tr>
<tr>
<td></td>
<td>Rated mains voltage $&lt; 300 V_{RMS}$</td>
<td>I-IV</td>
</tr>
<tr>
<td></td>
<td>Rated mains voltage $&lt; 400 V_{RMS}$</td>
<td>I-III</td>
</tr>
<tr>
<td></td>
<td>Rated mains voltage $&lt; 600 V_{RMS}$</td>
<td>I-III</td>
</tr>
</tbody>
</table>
### ISOLATION CHARACTERISTICS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IORM}$</td>
<td>Maximum working insulation voltage per IEC</td>
<td>1200</td>
<td>$V_{PEAK}$</td>
</tr>
<tr>
<td>$V_{PD(t)}$</td>
<td>Partial discharge test voltage per IEC</td>
<td>2250</td>
<td>$V_{PEAK}$</td>
</tr>
<tr>
<td>$V_{IOTM}$</td>
<td>Transient overvoltage</td>
<td>4250</td>
<td>$V_{PEAK}$</td>
</tr>
<tr>
<td>$R_s$</td>
<td>Isolation resistance</td>
<td>5100</td>
<td>$V_{PEAK}$</td>
</tr>
<tr>
<td>PD</td>
<td>Pollution degree</td>
<td>$&gt; 10^9$</td>
<td>$\Omega$</td>
</tr>
</tbody>
</table>

### ISOLATOR CHARACTERISTICS (1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>L(I01)</td>
<td>Minimum air gap (clearance)</td>
<td>7.9</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>L(I02)</td>
<td>Minimum external tracking (creepage)</td>
<td>7.9</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>CTI</td>
<td>Tracking resistance (comparative tracking index)</td>
<td>&gt; 400</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Minimum internal gap (internal clearance)</td>
<td>0.014</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>$R_{IO}$</td>
<td>Isolation resistance</td>
<td>$&gt; 10^{12}$</td>
<td></td>
<td></td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$C_{IO}$</td>
<td>Barrier capacitance input to output</td>
<td>$V_i = 0.8 \ V_{pp}$ at 1 MHz</td>
<td>1.2</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_{I}$</td>
<td>Input capacitance to ground</td>
<td>$V_i = 0.8 \ V_{pp}$ at 1 MHz</td>
<td>3</td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of a specific application. Care should be taken to maintain the creepage and clearance distance of the board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal according to the measurement techniques shown in the Isolation Glossary section. Techniques such as inserting grooves and/or ribs on the PCB are used to help increase these specifications.
ELECTRICAL CHARACTERISTICS

All minimum/maximum specifications at $T_A = -40^\circ C$ to 125$^\circ C$, AVDD = 4.5 V to 5.5 V, DVDD = 2.7 V to 5.5 V, VINP = $-250$ mV to 250 mV, VINN = 0 V, and sinc$^3$ filter with OSR = 256, unless otherwise noted. Typical values are at $T_A = 25^\circ C$, AVDD = 5 V, and DVDD = 3.3 V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>AMC1204-Q1</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_A$</td>
<td>Specified ambient temperature range</td>
<td>–40 125 $^\circ C$</td>
</tr>
</tbody>
</table>

### RESOLUTION

- **Resolution**: 16 Bits

### DC ACCURACY

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>INL</td>
<td>$T_A = -40^\circ C$ to 85$^\circ C$</td>
<td>–8</td>
<td>±2</td>
<td>8</td>
<td>LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>$T_A = -40^\circ C$ to 125$^\circ C$</td>
<td>–16</td>
<td>±8</td>
<td>16</td>
<td>LSB</td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>–1</td>
<td>±0.1</td>
<td>1</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$G_{ERR}$</td>
<td>–2.5</td>
<td>±0.5</td>
<td>2.5</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

### ANALOG INPUTS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSR</td>
<td>VINP – VINN</td>
<td>±320</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CM}$</td>
<td>–160</td>
<td>AVDD</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_I$</td>
<td>VINP or VINN</td>
<td>7</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{ID}$</td>
<td>VINP – VINN = ±250 mV</td>
<td>12.5</td>
<td>kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>VINP – VINN = ±320 mV</td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>$V_N$ from 0 V to 5 V at 0 Hz</td>
<td>108</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMTI</td>
<td>$V_N$ from 0 V to 5 V at 100 kHz</td>
<td>114</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### EXTERNAL CLOCK

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{CLKIN}$</td>
<td>Clock period</td>
<td>45.5</td>
<td>50</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>$f_{CLKIN}$</td>
<td>Input clock frequency</td>
<td>5</td>
<td>20</td>
<td>22</td>
<td>MHz</td>
</tr>
<tr>
<td>$D_{VCLKIN}$</td>
<td>Duty cycle</td>
<td>50</td>
<td>60</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

### AC ACCURACY

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINAD</td>
<td>$f_N = 1$ kHz, $T_A = -40^\circ C$ to 105$^\circ C$</td>
<td>70</td>
<td>87</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>SNR</td>
<td>$f_N = 1$ kHz, $T_A = -40^\circ C$ to 125$^\circ C$</td>
<td>69</td>
<td>87</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>THD</td>
<td>$f_N = 1$ kHz, $T_A = -40^\circ C$ to 105$^\circ C$</td>
<td>83</td>
<td>88</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>SFDR</td>
<td>$f_N = 1$ kHz, $T_A = -40^\circ C$ to 105$^\circ C$</td>
<td>72</td>
<td>96</td>
<td>dB</td>
<td></td>
</tr>
</tbody>
</table>

### DIGITAL INPUTS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IN}$</td>
<td>$V_N = DVDD$ to $DGND$</td>
<td>–10</td>
<td>10</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$C_{IP}$</td>
<td>–</td>
<td>5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified 500 mV input range.
(2) Ensured by design.
(3) Maximum values, including temperature drift, are ensured over the full specified temperature range.
ELECTRICAL CHARACTERISTICS (continued)

All minimum/maximum specifications at $T_A = -40^\circ C$ to $125^\circ C$, $AVDD = 4.5$ V to $5.5$ V, $DVDD = 2.7$ V to $5.5$ V, $VINP = -250$ mV to $250$ mV, $VINN = 0$ V, and sinc$^3$ filter with OSR = 256, unless otherwise noted. Typical values are at $T_A = 25^\circ C$, $AVDD = 5$ V, and $DVDD = 3.3$ V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>AMC1204-Q1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>LVCMOS logic family</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$ High-level input voltage</td>
<td>$DVDD = 2.7$ V to $3.6$ V</td>
<td>2</td>
</tr>
<tr>
<td>$V_{IL}$ Low-level input voltage</td>
<td>$DVDD = 2.7$ V to $3.6$ V</td>
<td>$-0.3$</td>
</tr>
<tr>
<td>DIGITAL OUTPUTS(2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{OUT}$ Output capacitance</td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>$C_{LOAD}$ Load capacitance</td>
<td></td>
<td>30</td>
</tr>
<tr>
<td>CMOS logic family</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$ High-level output voltage</td>
<td>$DVDD = 4.5$ V, $I_{OH} = -100$ µA</td>
<td>4.4</td>
</tr>
<tr>
<td>$V_{OL}$ Low-level output voltage</td>
<td>$DVDD = 4.5$ V, $I_{OL} = 100$ µA</td>
<td>0.5</td>
</tr>
<tr>
<td>LVCMOS logic family</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$ High-level output voltage</td>
<td>$I_{OH} = 20$ µA</td>
<td>$DVDD - 0.1$</td>
</tr>
<tr>
<td> </td>
<td>$I_{OH} = -4$ mA, $2.7$ V $\leq DVDD \leq 3.6$ V</td>
<td>$DVDD - 0.4$</td>
</tr>
<tr>
<td> </td>
<td>$I_{OH} = -4$ mA, $4.5$ V $\leq DVDD \leq 5.5$ V</td>
<td>$DVDD - 0.8$</td>
</tr>
<tr>
<td>$V_{OL}$ Low-level output voltage</td>
<td>$I_{OL} = 20$ µA</td>
<td>0.1</td>
</tr>
<tr>
<td> </td>
<td>$I_{OL} = 4$ mA</td>
<td>0.4</td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$AVDD$ High-side supply voltage</td>
<td></td>
<td>4.5</td>
</tr>
<tr>
<td>$DVDD$ Controller-side supply voltage</td>
<td></td>
<td>2.7</td>
</tr>
<tr>
<td>$I_{AVDD}$ High-side supply current</td>
<td>$4.5$ V $\leq AVDD \leq 5.5$ V</td>
<td>11</td>
</tr>
<tr>
<td>$I_{DVDD}$ Controller-side supply current</td>
<td>$2.7$ V $\leq DVDD \leq 3.6$ V</td>
<td>2</td>
</tr>
<tr>
<td> </td>
<td>$4.5$ V $\leq DVDD \leq 5.5$ V</td>
<td>2.8</td>
</tr>
<tr>
<td>$P_D$ Power dissipation</td>
<td>$AVDD = 5.5$ V, $DVDD = 3.6$ V</td>
<td>61.6</td>
</tr>
</tbody>
</table>
PIN CONFIGURATION

DW PACKAGE
SO-16
(TOP VIEW)

AVDD 1
VINP 2
VINN 3
AGND 4
NC(1) 5
NC 6
NC 7
AGND 8
16 DGND
15 NC
14 DVDD
13 CLKIN
12 NC
11 DATA
10 NC
9 DGND

(1) NC = no internal connection.

PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>PIN NO.</th>
<th>FUNCTION</th>
<th>DESCRIPTION</th>
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<tbody>
<tr>
<td>AVDD</td>
<td>1</td>
<td>Power</td>
<td>High-side power supply</td>
</tr>
<tr>
<td>VINP</td>
<td>2</td>
<td>Analog input</td>
<td>Noninverting analog input</td>
</tr>
<tr>
<td>VINN</td>
<td>3</td>
<td>Analog input</td>
<td>Inverting analog input</td>
</tr>
<tr>
<td>AGND</td>
<td>4, 8(1)</td>
<td>Power</td>
<td>High-side ground</td>
</tr>
<tr>
<td>DGND</td>
<td>9, 16</td>
<td>Power</td>
<td>Controller-side ground</td>
</tr>
<tr>
<td>DATA</td>
<td>11</td>
<td>Digital output</td>
<td>Modulator data output</td>
</tr>
<tr>
<td>CLKIN</td>
<td>13</td>
<td>Digital input</td>
<td>Modulator clock input</td>
</tr>
<tr>
<td>DVDD</td>
<td>14</td>
<td>Power</td>
<td>Controller-side power supply</td>
</tr>
<tr>
<td>NC</td>
<td>5, 6, 7, 10, 12, 15</td>
<td>—</td>
<td>No internal connection; can be tied to any potential or left unconnected</td>
</tr>
</tbody>
</table>

(1) Both pins are connected internally via a low-impedance path; thus, only one of the pins must be tied to the ground plane.

TIMING INFORMATION

Figure 1. Modulator Output Timing

TIMING CHARACTERISTICS FOR Figure 1

Over recommended ranges of supply voltage and operating free-air temperature, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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<tr>
<td>tCLK</td>
<td>45.5</td>
<td>50</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>tHIGH</td>
<td>20</td>
<td>25</td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>tLOW</td>
<td>20</td>
<td>25</td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>tD</td>
<td>2</td>
<td>15</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>
TYPICAL CHARACTERISTICS
At AVDD = 5 V, DVDD = 3.3 V, VINP = −250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

**INTEGRAL NONLINEARITY vs INPUT SIGNAL AMPLITUDE**

**INTEGRAL NONLINEARITY vs TEMPERATURE**

**OFFSET ERROR vs ANALOG SUPPLY VOLTAGE**

**OFFSET ERROR vs TEMPERATURE**

**OFFSET ERROR vs CLOCK FREQUENCY**

**OFFSET ERROR vs CLOCK DUTY CYCLE**
TYPICAL CHARACTERISTICS (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = -250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

Figure 8. GAIN ERROR vs ANALOG SUPPLY VOLTAGE

Figure 9. GAIN ERROR vs TEMPERATURE

Figure 10. GAIN ERROR vs CLOCK FREQUENCY

Figure 11. GAIN ERROR vs CLOCK DUTY CYCLE

Figure 12. POWER-SUPPLY REJECTION RATIO vs FREQUENCY

Figure 13. COMMON-MODE REJECTION RATIO vs INPUT SIGNAL FREQUENCY
TYPICAL CHARACTERISTICS (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc³ filter with OSR = 256, unless otherwise noted.

**SINAD AND SNR vs ANALOG SUPPLY VOLTAGE**

![Figure 14.](image)

**SINAD AND SNR vs TEMPERATURE**

![Figure 15.](image)

**SINAD AND SNR vs INPUT SIGNAL FREQUENCY**

![Figure 16.](image)

**SINAD AND SNR vs INPUT SIGNAL AMPLITUDE**

![Figure 17.](image)

**SINAD AND SNR vs CLOCK FREQUENCY**

![Figure 18.](image)

**SINAD AND SNR vs CLOCK DUTY CYCLE**

![Figure 19.](image)
TYPICAL CHARACTERISTICS (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

TOTAL HARMONIC DISTORTION vs ANALOG SUPPLY VOLTAGE

ANALOG SUPPLY VOLTAGE (V) vs THD (dB)

TOTAL HARMONIC DISTORTION vs TEMPERATURE

Figure 20.

Figure 21.

TOTAL HARMONIC DISTORTION vs INPUT SIGNAL FREQUENCY

INPUT SIGNAL FREQUENCY (kHz) vs THD (dB)

TOTAL HARMONIC DISTORTION vs INPUT SIGNAL AMPLITUDE

INPUT SIGNAL AMPLITUDE (mVpp) vs THD (dB)

Figure 22.

Figure 23.

TOTAL HARMONIC DISTORTION vs CLOCK FREQUENCY

CLOCK FREQUENCY (MHz) vs THD (dB)

TOTAL HARMONIC DISTORTION vs CLOCK DUTY CYCLE

CLOCK DUTY CYCLE (%) vs THD (dB)

Figure 24.

Figure 25.
TYPICAL CHARACTERISTICS (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = −250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

**SPURIOUS-FREE DYNAMIC RANGE vs ANALOG SUPPLY VOLTAGE**

![AVDD vs SFDR](image)

**SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE**

![Temperature vs SFDR](image)

**SPURIOUS-FREE DYNAMIC RANGE vs INPUT SIGNAL FREQUENCY**

![Input Frequency vs SFDR](image)

**SPURIOUS-FREE DYNAMIC RANGE vs INPUT SIGNAL AMPLITUDE**

![Input Amplitude vs SFDR](image)

**SPURIOUS-FREE DYNAMIC RANGE vs CLOCK FREQUENCY**

![Clock Frequency vs SFDR](image)

**SPURIOUS-FREE DYNAMIC RANGE vs CLOCK DUTY CYCLE**

![Clock Duty Cycle vs SFDR](image)
TYPICAL CHARACTERISTICS (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted.

---

**Figure 32.** FREQUENCY SPECTRUM  
(4096 point FFT, f\_IN = 1 kHz, 056 V\_pp)

**Figure 33.** FREQUENCY SPECTRUM  
(4096 point FFT, f\_IN = 5 kHz, 056 V\_pp)

**Figure 34.** ANALOG SUPPLY CURRENT vs ANALOG SUPPLY VOLTAGE

**Figure 35.** ANALOG SUPPLY CURRENT vs TEMPERATURE

**Figure 36.** ANALOG SUPPLY CURRENT vs CLOCK FREQUENCY

**Figure 37.** DIGITAL SUPPLY CURRENT vs DIGITAL SUPPLY VOLTAGE (3 V)
TYPICAL CHARACTERISTICS (continued)

At AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc³ filter with OSR = 256, unless otherwise noted.

**DIGITAL SUPPLY CURRENT vs DIGITAL SUPPLY VOLTAGE (5 V)**

![Graph 1: Digital Supply Current vs Digital Supply Voltage](image1)

**DIGITAL SUPPLY CURRENT vs TEMPERATURE**

![Graph 2: Digital Supply Current vs Temperature](image2)

**DIGITAL SUPPLY CURRENT vs CLOCK FREQUENCY**

![Graph 3: Digital Supply Current vs Clock Frequency](image3)
GENERAL DESCRIPTION

The AMC1204-Q1 is a single-channel, second-order, delta-sigma (ΔΣ) modulators designed for medium- to high-resolution analog-to-digital conversions. The isolated output of the converter (DATA) provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage.

Figure 41 shows a detailed block diagram of the AMC1204-Q1. The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. The SiO₂-based capacitive isolation barrier supports a high level of magnetic field immunity as described in the application report ISO72x Digital Isolator Magnetic-Field Immunity (SLLA181A, available for download at www.ti.com). The external clock input simplifies the synchronization of multiple current sense channels on system level. The extended frequency range of up to 20 MHz supports higher performance levels compared to the other solutions available on the market.

Figure 41. Detailed Block Diagram
THEORY OF OPERATION

The differential analog input of the AMC1204-Q1 is implemented with a switched-capacitor circuit. This switched-capacitor circuit implements a second-order modulator stage that digitizes the input signal into a 1-bit output stream. The externally-provided clock source at the CLKin pin is used by the capacitor circuit and the modulator and should be in the range of 5 MHz to 22 MHz. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream, accurately representing the analog input voltage over time, appears at the output of the converter at the DATA pin.

ANALOG INPUT

The AMC1204-Q1 measures the differential input signal $V_{IN} = (VINP - VINN)$ against the internal reference of 2.5 V using internal capacitors that are continuously charged and discharged. Figure 42 shows the simplified schematic of the ADC input circuitry; the right side of Figure 42 illustrates the input circuitry with the capacitors and switches replaced by an equivalent circuit.

In Figure 42, the $S_1$ switches close during the input sampling phase. With the $S_1$ switches closed, $C_{DIFF}$ charges to the voltage difference across VINP and VINN. For the discharge phase, both $S_1$ switches open first and then both $S_2$ switches close. $C_{DIFF}$ discharges approximately to AGND + 0.8 V during this phase. This two-phase sample/discharge cycle repeats with a period of $t_{CLKIN} = 1/f_{CLKIN}$. $f_{CLKIN}$ is the operating frequency of the modulator. The capacitors $C_{IP}$ and $C_{IN}$ are of parasitic nature and caused by bonding wires and the internal ESD protection structure.

*Figure 42. Equivalent Analog Input Circuit*

The input impedance becomes a consideration in designs with high input signal source impedance. This high impedance may cause degradation in gain, linearity, and THD. The importance of this effect, however, depends on the desired system performance. This input stage provides the mechanism to achieve low system noise, high common-mode rejection (105 dB), and excellent power-supply rejection.

There are two restrictions on the analog input signals VINP and VINN. First, if the input voltage exceeds the range AGND – 0.5 V to AVDD + 0.3 V, the input current must be limited to 10 mA because the input protection diodes on the front end of the converter begin to turn on. In addition, the linearity and the noise performance of the device are ensured only when the differential analog input voltage remains within ±250 mV.
MODULATOR

The modulator topology of the AMC1204-Q1 is fundamentally a second-order, switched-capacitor, ΔΣ modulator, such as the one conceptualized in Figure 43. The analog input voltage ($X_{in}$) and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage ($X_2$) at the input of the first integrator or modulator stage. The output of the first integrator is further differentiated with the DAC output; the resulting voltage ($X_3$) feeds the input of the second integrator stage. When the value of the integrated signal ($X_4$) at the output of the second stage equals the comparator reference voltage, the output of the comparator switches from high to low, or vice versa, depending on its previous state. In this case, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage ($X_6$), causing the integrators to progress in the opposite direction, while forcing the value of the integrator output to track the average of the input.

![Figure 43. Block Diagram of a Second-Order Modulator](image)

The modulator shifts the quantization noise to high frequencies, as shown in Figure 44; therefore, a low-pass digital filter should be used at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). A digital signal processor (DSP), microcontroller (μC), or field programmable gate array (FPGA) can be used to implement the filter. Another option is to use a suitable application-specific device such as the AMC1210, a four-channel digital sinc-filter.

![Figure 44. Quantization Noise Shaping](image)
DIGITAL OUTPUT

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time and low 50% of the time. A differential input of 250 mV produces a stream of ones and zeros that are high 78.1% of the time. A differential input of –250 mV produces a stream of ones and zeros that are high 21.9% of the time. This is also the specified linear input range of the modulator with the performance as specified in this data sheet. The range between 250 mV and 320 mV (absolute values) is the non-linear range of the modulator. The output of the modulator clips with a stream of only zeros with an input less than or equal to –320 mV or with a stream of only ones with an input greater than or equal to 320 mV. The input voltage versus the output modulator signal is shown in Figure 45.

The system clock of the AMC1204-Q1 is typically 20 MHz and is provided externally at the CLkin pin. The data are synchronously provided at 20 MHz at the DATA output pin. The data are changing at the falling edge of CLkin; for more details see the Timing Information section.

FILTER USAGE

The modulator generates a bit stream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, built with minimal effort and hardware, is a sinc^3-type filter, as shown in Equation 1:

\[ H(z) = \left( \frac{1 - z^{-\text{OSR}}}{1 - z^{-1}} \right)^3 \]  

(1)

This filter provides the best output performance at the lowest hardware size (count of digital gates). For an oversampling rate (OSR) in the range of 16 to 256, this filter is a good choice. All the characterization in this document is also done with a sinc^3 filter with OSR = 256 and an output word width of 16 bits.

![Figure 45. Analog Input versus AMC1204-Q1 Modulator Output](image-url)
In a sinc\textsuperscript{3} filter response (shown in Figure 46 and Figure 47), the location of the first notch occurs at the frequency of output data rate f_{DATA} = f_{CLK}/OSR. The –3 dB point is located at half the Nyquist frequency or f_{DATA}/4. For some applications, it may be necessary to use another filter type with different frequency response. Performance can be improved, for example, by using a cascaded filter structure. The first decimation stage could be built of a sinc\textsuperscript{3} filter with a low OSR and the second stage using a high-order filter.

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. Figure 48 illustrates the ENOB of the AMC1204-Q1 with different oversampling ratios. In this data sheet, this number is calculated from SNR using Equation 2:

\[ \text{SNR} = 1.76 \text{dB} + 6.02 \text{dB} \times \text{ENOB} \]  

(2)

In motor control applications, a very fast response time for overcurrent detection is required. The time for fully settling the filter depends on its order; that is, a sinc\textsuperscript{3} filter requires three data clocks for full settling (with f_{DATA} = f_{CLK}/OSR). Therefore, for overcurrent protection, filter types other than sinc\textsuperscript{3} might be a better choice; an alternative is the sinc\textsuperscript{2} filter. Figure 49 compares the settling times of different filter orders with sincfast being a modified sinc\textsuperscript{2} filter with behavior as shown in Equation 3.

\[ H(z) = \frac{1 - z^{-\text{OSR}}}{1 - z^{-1}} (1 + z^{-\text{OSR}}) \]  

(3)

Figure 46. Frequency Response of the Sinc\textsuperscript{3} Filter

Figure 47. Pole Response of the Sinc\textsuperscript{3} Filter

Figure 48. Measured Effective Number of Bits versus Oversampling Ratio

Figure 49. Measured Effective Number of Bits versus Settling Time
An example code for an implementation of a sinc³ filter in an FPGA follows. For more information, see the application note *Combining ADS1202 with FPGA Digital Filter for Current Measurement in Motor Control Applications (SBAA094)*, available for download at www.ti.com.

```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity FLT is
  port(RESN, MOUT, MCLK, CNR : in std_logic;
       CN5 : out std_logic_vector(23 downto 0));
end FLT;

architecture RTL of FLT is
  signal DN0, DN1, DN3, DN5 : std_logic_vector(23 downto 0);
  signal CN1, CN2, CN3, CN4 : std_logic_vector(23 downto 0);
  signal DELTA1 : std_logic_vector(23 downto 0);

begin
  process(MCLK, RESn)
  begin
    if RESn = '0' then
      DELTA1 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      if MOUT = '1' then
        DELTA1 <= DELTA1 + 1;
      end if;
    end if;
  end process;

  process(RESN, MCLK)
  begin
    if RESN = '0' then
      CN1 <= (others => '0');
      CN2 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      CN1 <= CN1 + DELTA1;
      CN2 <= CN2 + CN1;
    end if;
  end process;

  process(RESN, CNR)
  begin
    if RESN = '0' then
      DN0 <= (others => '0');
      DN1 <= (others => '0');
      DN3 <= (others => '0');
      DN5 <= (others => '0');
    elsif CNR'event and CNR = '1' then
      DN0 <= CN2;
      DN1 <= DN0;
      DN3 <= CN3;
      DN5 <= CN4;
    end if;
  end process;

  CN3 <= DN0 - DN1;
  CN4 <= CN3 - DN3;
  CN5 <= CN4 - DN5;
end RTL;
```
A typical operation of the AMC1204-Q1 in a motor control application is shown in Figure 50. Measurement of the motor phase current is done via the shunt resistor $R_{\text{SHUNT}}$ (in this case, a two-terminal shunt). For better performance, the differential signal is filtered using RC filters (components $R_2$, $R_3$, and $C_2$). Optionally, $C_3$ and $C_4$ can be used to reduce charge dumping from the inputs. In this case, care should be taken when choosing the quality of these capacitors—mismatch in values of these capacitors leads to a common-mode error at the input of the modulator.

The high-side power supply (AVDD) for the AMC1204-Q1 is derived from the power supply of the upper gate driver. For lowest cost, a zener diode can be used to limit the voltage to 5 V ±10%. A decoupling capacitor of 0.1 μF is recommended for filtering this power-supply path. This capacitor ($C_1$ in Figure 50) should be placed as close as possible to the AVDD pin for best performance. If better filtering is required, an additional 1 μF to 10 μF capacitor can be used. The floating ground reference AGND is derived from the end of the shunt resistor, which is connected to the negative input (VINN) of the AMC1204-Q1. If a four-terminal shunt is used, the inputs of AMC1204-Q1 are connected to the inner leads, while AGND is connected to one of the outer leads of the shunt. Both digital signals, CLKIN and DATA, can be directly connected to a digital filter (for example, the AMC1210); see Figure 51.

(1) Place $C_1$ close to the AMC1204-Q1.

Figure 50. Typical Application Diagram
Figure 51 shows an example of two AMC1204-Q1 devices and one ADS1209 (a dual-channel, 10 MHz, non-isolated modulator) connected to an AMC1210, building the entire analog front-end of a resolver-based motor control application.

For detailed information on the ADS1209 and AMC1210, visit the respective device product folders at www.ti.com.

![Diagram of Resolver-Based Motor Control Analog Front-End](image-url)
A layout recommendation showing the critical placement of the decoupling capacitor on the high-side and placement of the other components required by the AMC1204-Q1 is presented in Figure 52.
ISOLATION GLOSSARY

**Creepage Distance:** The shortest path between two conductive input to output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.

**Clearance:** The shortest distance between two conductive input to output leads measured through air (line of sight).

**Input-to-Output Barrier Capacitance:** The total capacitance between all input terminals connected together, and all output terminals connected together.

**Input-to-Output Barrier Resistance:** The total resistance between all input terminals connected together, and all output terminals connected together.

**Primary Circuit:** An internal circuit directly connected to an external supply mains or other equivalent source that supplies the primary circuit electric power.

**Secondary Circuit:** A circuit with no direct connection to primary power that derives its power from a separate isolated source.

**Comparative Tracking Index (CTI):** CTI is an index used for electrical insulating materials. It is defined as the numerical value of the voltage that causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface. The higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as tracking.

**Insulation:**

*Operational insulation*—Insulation needed for the correct operation of the equipment.

*Basic insulation*—Insulation to provide basic protection against electric shock.

*Supplementary insulation*—Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

*Double insulation*—Insulation comprising both basic and supplementary insulation.

*Reinforced insulation*—A single insulation system that provides a degree of protection against electric shock equivalent to double insulation.
Pollution Degree:

Pollution Degree 1—No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence on device performance.

Pollution Degree 2—Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation is to be expected.

Pollution Degree 3—Conductive pollution, or dry nonconductive pollution that becomes conductive because of condensation, occurs. Condensation is to be expected.

Pollution Degree 4—Continuous conductivity occurs as a result of conductive dust, rain, or other wet conditions.

Installation Category:

Overvoltage Category—This section is directed at insulation coordination by identifying the transient overvoltages that may occur, and by assigning four different levels as indicated in IEC 60664.

1. Signal Level: Special equipment or parts of equipment.
2. Local Level: Portable equipment, etc.
4. Primary Supply Level: Overhead lines, cable systems.

Each category should be subject to smaller transients than the previous category.
## REVISION HISTORY

<table>
<thead>
<tr>
<th>Changes from Revision A (October, 2012) to Revision B</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed $V_{PEAK}$ from 4000 to 4250.</td>
<td>1</td>
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<tr>
<td>• Changed $V_{PEAK}$ from 4000 to 4250.</td>
<td>1</td>
</tr>
<tr>
<td>• Changed $V_{IOTM}$ with $t = 60$ s (qualification test) test condition from 4000 to 4250.</td>
<td>4</td>
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<tr>
<td>• Changed $V_{IOTM}$ with $t = 1$ s (100% production test) test condition from 4000 to 5100.</td>
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### PACKAGING INFORMATION

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<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Top-Side Markings</th>
<th>Samples</th>
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<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>16</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>AMC1204Q</td>
<td></td>
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</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI’s terms “Lead-Free” or “Pb-Free” mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF AMC1204-Q1:**

- Catalog: AMC1204
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
### TAPE AND REEL INFORMATION

**Device** | **Package Type** | **Package Drawing** | **Pins** | **SPQ** | **Reel Diameter (mm)** | **Reel Width W1 (mm)** | **A0 (mm)** | **B0 (mm)** | **K0 (mm)** | **P1 (mm)** | **W (mm)** | **Pin1 Quadrant**
--- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | ---
AMC1204QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1

*All dimensions are nominal.*

**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Sprocket Holes**
- **User Direction of Feed**
- **Pocket Quadrants**

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### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMC1204QDWRQ1</td>
<td>SOIC</td>
<td>DW</td>
<td>16</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.
EXAMPLE BOARD LAYOUT

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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