Features

➤ Fast charge of nickel cadmium or nickel-metal hydride batteries
➤ Direct LED output displays charge status
➤ Fast-charge termination by ∆V, maximum voltage, maximum temperature, and maximum time
➤ Internal band-gap voltage reference
➤ Selectable pulse-trickle charge rates
➤ Low-power mode
➤ 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2002C Fast-Charge IC is a low-cost CMOS battery-charge controller providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the bq2002C to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002C integrates fast charge with pulsed-trickle control in a single IC for charging one or more NiCd or NiMH battery cells.

Fast charge is initiated on application of the charging supply or battery replacement. For safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits.

Fast charge is terminated by any of the following:

■ Peak voltage detection (PVD)
■ Negative delta voltage (¬∆V)
■ Maximum voltage
■ Maximum temperature
■ Maximum time

After fast charge, the bq2002C pulse-trickles the battery per the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002C may also be placed in low-standby-power mode to reduce system power consumption.

Pin Connections

- TM  Timer mode select input
- LED  Charging status output
- BAT  Battery voltage input
- VSS  System ground
- CC   Charge control output
- TS   Temperature sense input
- VCC  Supply voltage input
- INH  Charge inhibit input
- CC   Charge control output

Pin Names

SLUS136 - AUGUST 2011
Pin Descriptions

**TM**  
Timer mode input  
A three-level input that controls the settings for the fast charge safety timer, voltage termination mode, pulse-trickle, and voltage hold-off time.

**LED**  
Charging output status  
Open-drain output that indicates the charging status.

**BAT**  
Battery input voltage  
The battery voltage sense input. The input to this pin is created by a high-impedance resistor divider network connected between the positive and negative terminals of the battery.

**Vss**  
System ground

**TS**  
Temperature sense input  
Input for an external battery temperature monitoring thermistor.

**Vcc**  
Supply voltage input  
5.0V ±20% power input.

**INH**  
Charge inhibit input  
When high, INH suspends the fast charge in progress. When returned low, the IC resumes operation at the point where initially suspended.

**CC**  
Charge control output  
An open-drain output used to control the charging current to the battery. CC switching to high impedance (Z) enables charging current to flow, and low to inhibit charging current. CC is modulated to provide pulse trickle.

Functional Description

Figure 2 shows a state diagram and Figure 3 shows a block diagram of the bq2002C.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of

$$\frac{R_{B1}}{R_{B2}} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, R1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1 MΩ.

A ground-referenced negative temperature coefficient thermistor placed near the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between Vcc and Vss. See Figure 1.

**Figure 1. Voltage and Temperature Monitoring and TM Pin Configuration**
Chip on VCC ≥ 4.0V

Battery Voltage too High?

VBAT ≥ 2V

Battery Voltage too Low?

VBAT < 2V

0.84V < VBAT

VTS > VCC/2

Battery Temperature?

VTS ≤ VCC/2

Charge Pending

Fast LED = Low

VBAT ≤ 0.84V

VBAT < 2V and VTS > VCC/2

VBAT > 2V or VTS < VCC/2 or PVD or -V or Maximum Time Out

Trickle LED = Flash

VBAT > 0.84V

VBAT > 2V and VTS > VCC/2

VBAT > 2V

VBAT < 0.84V

0.84V < VBAT

VBAT > 2V

VBAT < 2V

Figure 2. State Diagram

Figure 3. Block Diagram
Starting A Charge Cycle

Either of two events starts a charge cycle (see Figure 4):
1. Application of power to VCC or
2. Voltage at the BAT pin falling through the maximum cell voltage VMCV where
   $$\text{VMCV} = 2V \pm 5\%$$

If the battery is within the configured temperature and voltage limits, the IC begins fast charge. The valid battery voltage range is
   $$\text{VLBAT} < \text{VBAT} < \text{VMCV},$$
where
   $$\text{VLBAT} = 0.175 \times \text{VCC} \pm 20\%$$

The valid temperature range is
   $$\text{VTS} > \text{VHTF},$$
where
   $$\text{VHTF} = 0.6 \times \text{VCC} \pm 5\%.$$  

If VBAT \leq VLBAT or VTS \leq VHTF, the IC enters the charge-pending state. In this state pulse trickle charge is applied to the battery and the LED flashes until the voltage and temperature come into the allowed fast charge range or VBAT rises above VMCV. Anytime VBAT \geq VMCV, the IC enters the Charge Complete/Battery Absent state. In this state the LED is off and trickle charge is applied to the battery until the next new charge cycle begins.

Fast charge continues until termination by one or more of the five possible termination conditions:
- Peak voltage detection (PVD)
- Negative delta voltage (-\Delta V)
- Maximum voltage
- Maximum temperature
- Maximum time

<table>
<thead>
<tr>
<th>Corresponding Fast-Charge Rate</th>
<th>TM</th>
<th>Termination</th>
<th>Typical Fast-Charge Time Limits (minutes)</th>
<th>Typical PVD and -\Delta V Hold-Off Time (seconds)</th>
<th>Pulse-Trickle Rate</th>
<th>Pulse-Trickle Pulse Width (ms)</th>
<th>Maximum Synchronized Sampling Period (seconds)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C/2 Mid</td>
<td>PVD</td>
<td>160</td>
<td>300</td>
<td>C/32</td>
<td>73</td>
<td>18.7</td>
<td></td>
</tr>
<tr>
<td>1C Low</td>
<td>PVD</td>
<td>80</td>
<td>150</td>
<td>C/32</td>
<td>37</td>
<td>18.7</td>
<td></td>
</tr>
<tr>
<td>2C High</td>
<td>-\Delta V</td>
<td>40</td>
<td>75</td>
<td>C/32</td>
<td>18</td>
<td>9.4</td>
<td></td>
</tr>
</tbody>
</table>

Notes: Typical conditions = 25°C, VCC = 5.0V
Mid = 0.5 * VCC \pm 0.5V
Tolerance on all timing is \pm 12%.
PVD and -ΔV Termination

There are two modes for voltage termination, depending on the state of TM. For -ΔV (TM = high), if \( V_{BAT} \) is lower than any previously measured value by 12mV ±3mV, fast charge is terminated. For PVD (TM = low or mid), a decrease of 2.5mV ±2.5mV terminates fast charge. The PVD and -ΔV tests are valid in the range 1V < \( V_{BAT} < 2V \).

Synchronized Voltage Sampling

Voltage sampling at the BAT pin for PVD and -ΔV termination may be synchronized to an external stimulus using the INH input. Low-high-low input pulses between 100ns and 3.5ms in width must be applied at the INH pin with a frequency greater than the “maximum synchronized sampling period” set by the state of the TM pin as shown in Table 1. Voltage is sampled on the falling edge of such pulses. If the time between pulses is greater than the synchronizing period, voltage sampling “free-runs” at once every 17 seconds. A sample is taken by averaging together voltage measurements taken 57µs apart. The IC takes 32 measurements in PVD mode and 16 measurements in -ΔV mode. The resulting sample periods (9.17 and 18.18ms, respectively) filter out harmonics centered around 55 and 109Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50 or 60Hz AC sources. If the INH input remains high for more than 12ms, the voltage sample history kept by the IC and used for PVD and -ΔV termination decisions is erased and a new history is started. Such a reset is required when transitioning from free-running to synchronized voltage sampling. The response of the IC to pulses less than 100ns in width or between 3.5ms and 12ms is indeterminate. The tolerance on all timing is ±12%.

Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off time, the PVD and -ΔV terminations are disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. Maximum voltage and temperature terminations are not affected by the hold-off period.

Maximum Voltage, Temperature, and Time

Any time the voltage on the BAT pin exceeds the maximum cell voltage, \( V_{MCV} \), fast charge is terminated. Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold \( V_{TCO} \), where

\[
V_{TCO} = 0.5 \times V_{CC} \pm 5\%.
\]

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase. There is no time limit on the trickle-charge phase.

Pulse-Trickle Charge

Pulse-trickle is used to compensate for self-discharge while the battery is idle in the charger. The battery is pulse-trickle charged by driving the CC pin active once per second for the period specified in Table 1. This results in a trickle rate of C/32.

TM Pin

The TM pin is a three-level pin used to select the charge timer, voltage termination mode, trickle rate, and voltage hold-off period options. Table 1 describes the states selected by the TM pin. The mid-level selection input is developed by a resistor divider between \( V_{CC} \) and ground that fixes the voltage on TM at \( V_{CC}/2 \pm 0.5V \). See Figure 4.

Charge Status Indication

A fast charge in progress is uniquely indicated when the LED pin goes low. In the charge pending state, the LED pin is driven low for 500ms, then to high-Z for 500ms. The LED pin is driven to the high-Z state for all other conditions. Figure 2 outlines the state of the LED pin during charge.

Charge Inhibit

Fast charge may be inhibited by using the INH pin. When high, INH suspends all fast charge activity and the internal charge timer. INH freezes the current state of LED until inhibit is removed. Temperature monitoring is not affected by the INH pin. During charge inhibit, the bq2002C continues to pulse-trickle charge the battery per the TM selection. When INH returns low, charge control and the charge timer resume from the point where INH became active.

Low-Power Mode

The IC enters a low-power state when \( V_{BAT} \) is driven above the power-down threshold \( (V_{PD}) \) where:

\[
V_{PD} = V_{CC} \times (1V \pm 0.5V)
\]

Both the CC pin and the LED are driven to the high-Z state. The operating current is reduced to less than 1µA in this mode. When \( V_{BAT} \) returns to a value below \( V_{PD} \), the IC pulse-trickle charges until the next new charge cycle begins.
### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>VCC relative to VSS</td>
<td>-0.3</td>
<td>+7.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VT</td>
<td>DC voltage applied on any pin excluding VCC relative to VSS</td>
<td>-0.3</td>
<td>+7.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>TOPR</td>
<td>Operating ambient temperature</td>
<td>0</td>
<td>+70</td>
<td>°C</td>
<td>Commercial</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage temperature</td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>TSOLDER</td>
<td>Soldering temperature</td>
<td>-</td>
<td>+260</td>
<td>°C</td>
<td>10 sec max.</td>
</tr>
<tr>
<td>TBIAS</td>
<td>Temperature under bias</td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

### DC Thresholds \( (T_A = 0 \text{ to } 70\,\text{°C}; \ V_{CC} \pm 20\%) \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Rating</th>
<th>Tolerance</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTCO</td>
<td>Temperature cutoff</td>
<td>(0.5 \times V_{CC})</td>
<td>±5%</td>
<td>V</td>
<td>(V_{TS} \leq V_{TCO}) inhibits/terminates fast charge</td>
</tr>
<tr>
<td>VHTF</td>
<td>High-temperature fault</td>
<td>(0.6 \times V_{CC})</td>
<td>±5%</td>
<td>V</td>
<td>(V_{TS} \leq V_{HTF}) inhibits fast charge start</td>
</tr>
<tr>
<td>VMCV</td>
<td>Maximum cell voltage</td>
<td>2</td>
<td>±5%</td>
<td>V</td>
<td>(V_{BAT} \geq V_{MCV}) inhibits/terminates fast charge</td>
</tr>
<tr>
<td>VLBAT</td>
<td>Minimum cell voltage</td>
<td>(0.175 \times V_{CC})</td>
<td>±20%</td>
<td>V</td>
<td>(V_{BAT} \leq V_{LBAT}) inhibits fast charge</td>
</tr>
<tr>
<td>-ΔV</td>
<td>BAT input change for -ΔV detection</td>
<td>-12</td>
<td>±3</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>PVD</td>
<td>BAT input change for PVD detection</td>
<td>-2.5</td>
<td>±2.5</td>
<td>mV</td>
<td></td>
</tr>
</tbody>
</table>
# Recommended DC Operating Conditions (TA = 0 to 70°C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply voltage</td>
<td>4.0</td>
<td>5.0</td>
<td>6.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VDET</td>
<td>-Δ, PVD detect voltage</td>
<td>1</td>
<td>-</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VBAT</td>
<td>Battery input</td>
<td>0</td>
<td>-</td>
<td>VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VTS</td>
<td>Thermistor input</td>
<td>0.5</td>
<td>-</td>
<td>VCC</td>
<td>V</td>
<td>VTS &lt;0.5V prohibited</td>
</tr>
<tr>
<td>VIH</td>
<td>Logic input high</td>
<td>0.5</td>
<td>-</td>
<td>-</td>
<td>V</td>
<td>INH</td>
</tr>
<tr>
<td>VIM</td>
<td>Logic input mid</td>
<td>VCC - 0.5</td>
<td>-</td>
<td>VCC/2 + 0.5</td>
<td>V</td>
<td>TM</td>
</tr>
<tr>
<td>VIL</td>
<td>Logic input low</td>
<td>-</td>
<td>-</td>
<td>0.1</td>
<td>V</td>
<td>INH</td>
</tr>
<tr>
<td>VOL</td>
<td>Logic output low</td>
<td>-</td>
<td>-</td>
<td>0.8</td>
<td>V</td>
<td>LED, CC, IOL =10mA</td>
</tr>
<tr>
<td>VPD</td>
<td>Power down</td>
<td>VCC - 1.5</td>
<td>-</td>
<td>VCC - 0.5</td>
<td>V</td>
<td>VBAT ≥ VPD max. powers down bq2002C, VBAT &lt; VPD min. = normal operation.</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply current</td>
<td>-</td>
<td>-</td>
<td>500</td>
<td>µA</td>
<td>Outputs unloaded, VCC = 5.1V</td>
</tr>
<tr>
<td>ISB</td>
<td>Standby current</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>µA</td>
<td>VCC = 5.1V, VBAT = VPD</td>
</tr>
<tr>
<td>IOL</td>
<td>LED, CC sink</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>mA</td>
<td>@VOL = VSS +0.8V</td>
</tr>
<tr>
<td>IL</td>
<td>Input leakage</td>
<td>-</td>
<td>-</td>
<td>±1</td>
<td>µA</td>
<td>INH, CC, V = VSS to VCC</td>
</tr>
<tr>
<td>IOZ</td>
<td>Output leakage in high-Z state</td>
<td>-5</td>
<td>-</td>
<td>-</td>
<td>µA</td>
<td>LED, CC</td>
</tr>
</tbody>
</table>

**Note:** All voltages relative to VSS.
## Impedance

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{BAT}$</td>
<td>Battery input impedance</td>
<td>50</td>
<td>-</td>
<td>-</td>
<td>Ω</td>
</tr>
<tr>
<td>$R_{TS}$</td>
<td>TS input impedance</td>
<td>50</td>
<td>-</td>
<td>-</td>
<td>Ω</td>
</tr>
</tbody>
</table>

## Timing  \( (T_A = 0 \text{ to } +70^\circ\text{C}; \ V_{CC} \pm 10\%) \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>$d_{FCV}$</td>
<td>Time base variation</td>
<td>-12</td>
<td>-</td>
<td>12</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** Typical is at $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$. 
8-Pin DIP (PN)

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Inches</th>
<th>Millimeters</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.160</td>
<td>4.06</td>
</tr>
<tr>
<td></td>
<td>0.180</td>
<td>4.57</td>
</tr>
<tr>
<td>A1</td>
<td>0.015</td>
<td>0.38</td>
</tr>
<tr>
<td></td>
<td>0.040</td>
<td>1.02</td>
</tr>
<tr>
<td>B</td>
<td>0.015</td>
<td>0.38</td>
</tr>
<tr>
<td></td>
<td>0.022</td>
<td>0.56</td>
</tr>
<tr>
<td>B1</td>
<td>0.055</td>
<td>1.40</td>
</tr>
<tr>
<td></td>
<td>0.065</td>
<td>1.65</td>
</tr>
<tr>
<td>C</td>
<td>0.008</td>
<td>0.20</td>
</tr>
<tr>
<td></td>
<td>0.013</td>
<td>0.33</td>
</tr>
<tr>
<td>D</td>
<td>0.350</td>
<td>8.89</td>
</tr>
<tr>
<td></td>
<td>0.380</td>
<td>9.65</td>
</tr>
<tr>
<td>E</td>
<td>0.300</td>
<td>7.62</td>
</tr>
<tr>
<td></td>
<td>0.325</td>
<td>8.26</td>
</tr>
<tr>
<td>E1</td>
<td>0.230</td>
<td>5.84</td>
</tr>
<tr>
<td></td>
<td>0.280</td>
<td>7.11</td>
</tr>
<tr>
<td>e</td>
<td>0.300</td>
<td>7.62</td>
</tr>
<tr>
<td></td>
<td>0.370</td>
<td>9.40</td>
</tr>
<tr>
<td>G</td>
<td>0.090</td>
<td>2.29</td>
</tr>
<tr>
<td></td>
<td>0.110</td>
<td>2.79</td>
</tr>
<tr>
<td>L</td>
<td>0.115</td>
<td>2.92</td>
</tr>
<tr>
<td></td>
<td>0.150</td>
<td>3.81</td>
</tr>
<tr>
<td>S</td>
<td>0.020</td>
<td>0.51</td>
</tr>
<tr>
<td></td>
<td>0.040</td>
<td>1.02</td>
</tr>
</tbody>
</table>

8-Pin PN (0.300” DIP)
8-Pin SOIC Narrow (SN)

8-Pin SN (0.150" SOIC)

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Inches</th>
<th>Millimeters</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.060</td>
<td>1.52</td>
</tr>
<tr>
<td></td>
<td>0.070</td>
<td>1.78</td>
</tr>
<tr>
<td>A1</td>
<td>0.004</td>
<td>0.10</td>
</tr>
<tr>
<td></td>
<td>0.010</td>
<td>0.25</td>
</tr>
<tr>
<td>B</td>
<td>0.013</td>
<td>0.33</td>
</tr>
<tr>
<td></td>
<td>0.020</td>
<td>0.51</td>
</tr>
<tr>
<td>C</td>
<td>0.007</td>
<td>0.18</td>
</tr>
<tr>
<td></td>
<td>0.010</td>
<td>0.25</td>
</tr>
<tr>
<td>D</td>
<td>0.185</td>
<td>4.70</td>
</tr>
<tr>
<td></td>
<td>0.200</td>
<td>5.08</td>
</tr>
<tr>
<td>E</td>
<td>0.150</td>
<td>3.81</td>
</tr>
<tr>
<td></td>
<td>0.160</td>
<td>4.06</td>
</tr>
<tr>
<td>e</td>
<td>0.045</td>
<td>1.14</td>
</tr>
<tr>
<td></td>
<td>0.055</td>
<td>1.40</td>
</tr>
<tr>
<td>H</td>
<td>0.225</td>
<td>5.72</td>
</tr>
<tr>
<td></td>
<td>0.245</td>
<td>6.22</td>
</tr>
<tr>
<td>L</td>
<td>0.015</td>
<td>0.38</td>
</tr>
<tr>
<td></td>
<td>0.035</td>
<td>0.89</td>
</tr>
</tbody>
</table>
Data Sheet Revision History

<table>
<thead>
<tr>
<th>Change No.</th>
<th>Page No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>All</td>
<td>Revised format and outline of this data sheet</td>
</tr>
<tr>
<td>2</td>
<td>5</td>
<td>Removed &quot;top-off&quot;</td>
</tr>
</tbody>
</table>

Note: Change 1 = Sept. 1997 B changes from Dec. 1995.
Note: Change 2 = July 2011

Ordering Information

bq2002C

Package Option:
PN – 8-pin plastic DIP
SN – 8-pin narrow SOIC

Device:
bq2002C Fast-Charge IC
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>BQ2002CPN</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td>2002CPN</td>
<td>Samples</td>
</tr>
<tr>
<td>BQ2002CPNE4</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td>2002CPN</td>
<td>Samples</td>
</tr>
<tr>
<td>BQ2002CSN</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>2002C</td>
<td>Samples</td>
</tr>
<tr>
<td>BQ2002CSNTR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>2002C</td>
<td>Samples</td>
</tr>
<tr>
<td>BQ2002CSNTRG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>2002C</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE**: Product device recommended for new designs.

**LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
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**TAPE AND REEL INFORMATION**

**TAPE DIMENSIONS**

<table>
<thead>
<tr>
<th>A0</th>
<th>Dimension designed to accommodate the component width</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

**REEL DIMENSIONS**

- Reel Diameter
- Reel Width (W1)

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Sprocket Holes
- User Direction of Feed
- Pocket Quadrants

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>BQ2002CSNTR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BQ2002CSNTR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>340.5</td>
<td>338.1</td>
<td>20.6</td>
</tr>
</tbody>
</table>
NOTES:

A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS–012 variation AA.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
P (R-PDIP-T8)  PLASTIC DUAL-IN-LINE PACKAGE

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
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