FEATURES

- Qualified for Automotive Applications
- Ideal For Highly Efficient Charger Designs For Single-, Two-, or Three-Cell Li-Ion and Li-Polymer Battery Packs
- Also for LiFePO₄ Battery (see Using bq24105 to Charge LiFePO₄ Battery)
- Integrated Synchronous Fixed-Frequency PWM Controller Operating at 1.1 MHz With 0% to 100% Duty Cycle
- Integrated Power FETs For Up To 2-A Charge Rate
- High-Accuracy Voltage and Current Regulation
- Stand-Alone (Built-In Charge Management and Control) Version
- Status Outputs For LED or Host Processor Interface Indicates Charge-In-Progress, Charge Completion, Fault, and AC-Adapter Present Conditions
- 20-V Maximum Voltage Rating on IN and OUT Pins
- High-Side Battery Current Sensing
- Battery Temperature Monitoring
- Automatic Sleep Mode for Low Power Consumption
- Reverse Leakage Protection Prevents Battery Drainage
- Thermal Shutdown and Protection
- Built-In Battery Detection
- Available in 20-Pin, 3.5 mm × 4.5 mm, QFN Package

DESCRIPTION

The bqSWITCHER™ series are highly integrated Li-ion and Li-polymer switch-mode charge management devices targeted at a wide range of portable applications. The bqSWITCHER™ series offers integrated synchronous PWM controller and power FETs, high-accuracy current and voltage regulation, charge preconditioning, charge status, and charge termination, in a small, thermally enhanced QFN package.

The bqSWITCHER charges the battery in three phases: conditioning, constant current, and constant voltage. Charge is terminated based on user-selectable minimum current level. A programmable charge timer provides a safety backup for charge termination. The bqSWITCHER automatically restarts the charge cycle if the battery voltage falls below an internal threshold. The bqSWITCHER automatically enters sleep mode when V\text{CC} supply is removed.
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>( T_A )</th>
<th>PACKAGE</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40°C to 85°C</td>
<td>QFN – RHL</td>
<td>Reel of 3000</td>
<td>BQ24105IRHLRQ1</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>( V_{SS} ) (unless otherwise noted)</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage range (with respect to ( V_{SS} ))</td>
<td>IN, VCC</td>
<td>4.35</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage range (with respect to ( V_{SS} ) and PGND)</td>
<td>STAT1, STAT2, PG, CE, SNS, BAT, OUT</td>
<td>-0.3 V to 20 V</td>
<td>-0.7 V to 20 V</td>
<td>V</td>
</tr>
<tr>
<td>Voltage difference between SNS and BAT inputs (( V_{SNS} - V_{BAT} ))</td>
<td></td>
<td>( \pm 1 ) V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output sink</td>
<td>STAT1, STAT2, PG</td>
<td>10 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output current (average)</td>
<td>OUT</td>
<td>2.2 A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_A )</td>
<td>Operating free-air temperature range</td>
<td>-40°C to 85°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_J )</td>
<td>Junction temperature range</td>
<td>-40°C to 125°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_{stg} )</td>
<td>Storage temperature</td>
<td>-65°C to 150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds</td>
<td></td>
<td>300°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### PACKAGE DISSIPATION RATINGS

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>( \theta_JA )</th>
<th>( \theta_JC )</th>
<th>POWER RATING</th>
<th>DERATING FACTOR ABOVE ( T_A = 40^\circ C )</th>
</tr>
</thead>
<tbody>
<tr>
<td>RHL(1)</td>
<td>46.87°C/W</td>
<td>2.5°C/W</td>
<td>1.81 W</td>
<td>0.021 W/°C</td>
</tr>
</tbody>
</table>

(1) This data is based on using the JEDEC High-K board, and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2x3 via matrix.

### RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, ( V_{CC} ) and IN (Tie together)</td>
<td>4.35(1)</td>
<td>16(2)</td>
<td>V</td>
</tr>
<tr>
<td>Operating junction temperature range, ( T_J )</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) The IC continues to operate below \( V_{min} \), to 3.5 V, but the specifications are not tested and not specified.

(2) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the IN or OUT pins. A tight layout minimizes switching noise.

### ELECTRICAL CHARACTERISTICS

\( T_J = 0°C \) to 125°C and recommended supply voltage range (unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Currents</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS (continued)

**T<sub>J</sub> = 0°C to 125°C and recommended supply voltage range (unless otherwise stated)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I&lt;sub&gt;VCC&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; supply current</td>
<td>10</td>
<td>5</td>
<td>315</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; &gt; V&lt;sub&gt;CC&lt;/sub&gt;(min), PWM switching</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; &gt; V&lt;sub&gt;CC&lt;/sub&gt;(min), PWM NOT switching</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;SLP&lt;/sub&gt;</td>
<td>Battery discharge sleep current, (SNS, BAT, OUT, FB pins)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0°C ≤ T&lt;sub&gt;J&lt;/sub&gt; ≤ 65°C, V&lt;sub&gt;BAT&lt;/sub&gt; = 4.2 V, V&lt;sub&gt;CC&lt;/sub&gt; &lt; V&lt;sub&gt;SLP&lt;/sub&gt; or V&lt;sub&gt;CC&lt;/sub&gt; &gt; V&lt;sub&gt;SLP&lt;/sub&gt; but not in charge</td>
<td>3.5</td>
<td>5.5</td>
<td>7.7</td>
<td>µA</td>
</tr>
<tr>
<td>V&lt;sub&gt;IBAT&lt;/sub&gt;</td>
<td>Feedback regulation REF for bq24105 (W/FB)</td>
<td>2.1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>I&lt;sub&gt;IBAT&lt;/sub&gt; = 25 nA typical into pin</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;REG&lt;/sub&gt;</td>
<td>Voltage regulated across R&lt;sub&gt;SNS&lt;/sub&gt; Accuracy</td>
<td>150</td>
<td>2000</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>V&lt;sub&gt;TERM&lt;/sub&gt;</td>
<td>Charge current termination detection range</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;IBAT&lt;/sub&gt; &gt; V&lt;sub&gt;TERM&lt;/sub&gt;</td>
<td>15</td>
<td>200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>K&lt;sub&gt;TERM&lt;/sub&gt;</td>
<td>Termination current set factor</td>
<td>1000</td>
<td></td>
<td>V/A</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;TERM&lt;/sub&gt;</td>
<td>Charger termination accuracy</td>
<td>V&lt;sub&gt;IBAT&lt;/sub&gt; &gt; V&lt;sub&gt;TERM&lt;/sub&gt;</td>
<td>1000</td>
<td></td>
<td>V/A</td>
</tr>
<tr>
<td>t&lt;sub&gt;TERM&lt;/sub&gt;</td>
<td>Deglitch time for charge termination</td>
<td>Both rising and falling, 2-mV overdrive t&lt;sub&gt;RISE&lt;/sub&gt;, t&lt;sub&gt;FALL&lt;/sub&gt; = 100 ns</td>
<td>20</td>
<td>30</td>
<td>40</td>
</tr>
</tbody>
</table>

**Voltage Regulation**

- **Battery discharge sleep current**, (SNS, BAT, OUT, FB pins):
  - 0°C ≤ T<sub>J</sub> ≤ 65°C, V<sub>BAT</sub> = 8.4 V, V<sub>CC</sub> < V<sub>(SLP)</sub> or V<sub>CC</sub> > V<sub>(SLP)</sub> but not in charge
  - 0°C ≤ T<sub>J</sub> ≤ 65°C, V<sub>BAT</sub> = 12.6 V, V<sub>CC</sub> < V<sub>(SLP)</sub> or V<sub>CC</sub> > V<sub>(SLP)</sub> but not in charge

**Current Regulation - Fast Charge**

- **Output current range of converter**: 150 mA to 2000 mA
- **Programmed Where**: 5 kΩ ≤ R<sub>SET1</sub> ≤ 10 kΩ, Select R<sub>SET1</sub> to program V<sub>IREG</sub>, V<sub>IREG(measured)</sub> = I<sub>OCHARGE</sub> + R<sub>SNS</sub> (–10% to 10% excludes errors due to R<sub>SET1</sub> and R<sub>SNS</sub> tolerances)

**Precharge and Short-Circuit Current Regulation**

- **Precharge to fast-charge transition voltage threshold, BAT, bq24100/03/03A/04/05/08/09 ICs only**: 68% V<sub>TERM</sub>
- **Deglitch time for precharge to fast charge transition**: Rising voltage: t<sub>RISE</sub>, t<sub>FALL</sub> = 100 ns, 2-mV overdrive
- **Precharge range**: V<sub>IBAT</sub> < V<sub>LOWV</sub>, t < t<sub>PRECHG</sub>
- **Precharge set voltage, ISET2**: V<sub>IBAT</sub> < V<sub>LOWV</sub>, t < t<sub>PRECHG</sub>
- **Precharge current set factor**: 1000 V/A

**Temperature Comparator and VTSB Bias Regulator**

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### ELECTRICAL CHARACTERISTICS (continued)

**T<sub>J</sub> = 0°C to 125°C and recommended supply voltage range (unless otherwise stated)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>%LTF</td>
<td>Cold temperature threshold, TS, % of bias</td>
<td>72.8%</td>
<td>73.5%</td>
<td>74.2%</td>
<td></td>
</tr>
<tr>
<td>%HTF</td>
<td>Hot temperature threshold, TS, % of bias</td>
<td>33.7%</td>
<td>34.4%</td>
<td>35.1%</td>
<td></td>
</tr>
<tr>
<td>%TCO</td>
<td>Cutoff temperature threshold, TS, % of bias</td>
<td>28.7%</td>
<td>29.3%</td>
<td>29.9%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>LTF hysteresis</td>
<td>0.5%</td>
<td>1%</td>
<td>1.5%</td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;0p,TS&lt;/sub&gt;</td>
<td>Deglitch time for temperature fault, TS</td>
<td>20</td>
<td>30</td>
<td>40</td>
<td>ms</td>
</tr>
<tr>
<td>V&lt;sub&gt;DIVTSB&lt;/sub&gt;</td>
<td>TS bias output voltage</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; &gt; V&lt;sub&gt;IN(min)&lt;/sub&gt;, I&lt;sub&gt;VT&lt;/sub&gt; = 10 mA, 0.1 µF ≤ C&lt;sub&gt;DIVTSB&lt;/sub&gt; ≤ 1 µF</td>
<td>3.15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;DIVTSB&lt;/sub&gt;</td>
<td>TS bias voltage regulation accuracy</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; &gt; V&lt;sub&gt;IN(min)&lt;/sub&gt;, I&lt;sub&gt;VT&lt;/sub&gt; = 10 mA, 0.1 µF ≤ C&lt;sub&gt;DIVTSB&lt;/sub&gt; ≤ 1 µF</td>
<td>-10%</td>
<td>10%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Battery Recharge Threshold</td>
<td>V&lt;sub&gt;RCH&lt;/sub&gt;</td>
<td>75</td>
<td>100</td>
<td>125</td>
<td>mV/cell</td>
</tr>
<tr>
<td></td>
<td>Recharge threshold voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;0p,RCH&lt;/sub&gt;</td>
<td>Deglitch time</td>
<td>20</td>
<td>30</td>
<td>40</td>
<td>ms</td>
</tr>
<tr>
<td>V&lt;sub&gt;DIVSTAT&lt;/sub&gt;</td>
<td>Low-level output saturation voltage, STATx</td>
<td>I&lt;sub&gt;D&lt;/sub&gt; = 5 mA</td>
<td></td>
<td>0.5V</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;DIVPG&lt;/sub&gt;</td>
<td>Low-level output saturation voltage, PG</td>
<td>I&lt;sub&gt;D&lt;/sub&gt; = 10 mA</td>
<td></td>
<td>0.1V</td>
<td></td>
</tr>
<tr>
<td>CE Input</td>
<td>V&lt;sub&gt;L&lt;/sub&gt;</td>
<td>I&lt;sub&gt;L&lt;/sub&gt; = 5 µA</td>
<td>0</td>
<td>0.4V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;H&lt;/sub&gt;</td>
<td>I&lt;sub&gt;H&lt;/sub&gt; = 20 µA</td>
<td>1.3</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>TTC Input</td>
<td>t&lt;sub&gt;PRECHG&lt;/sub&gt;</td>
<td>1440</td>
<td>1800</td>
<td>2160</td>
<td>s</td>
</tr>
<tr>
<td></td>
<td>Precharge timer</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;CHARGE&lt;/sub&gt;</td>
<td>Programmable charge timer range</td>
<td>I&lt;sub&gt;(CHG)&lt;/sub&gt; = C&lt;sub&gt;(TTC)&lt;/sub&gt; × K&lt;sub&gt;(TTC)&lt;/sub&gt;</td>
<td>25</td>
<td>572</td>
<td>minutes</td>
</tr>
<tr>
<td></td>
<td>Charge timer accuracy</td>
<td>0.01 µF ≤ C&lt;sub&gt;(TTC)&lt;/sub&gt; ≤ 0.18 µF</td>
<td>-10%</td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>K&lt;sub&gt;(TTC)&lt;/sub&gt;</td>
<td>Timer multiplier</td>
<td>2.6</td>
<td></td>
<td></td>
<td>min/nF</td>
</tr>
<tr>
<td>C&lt;sub&gt;(TTC)&lt;/sub&gt;</td>
<td>Charge time capacitor range</td>
<td>0.01</td>
<td>0.22</td>
<td>µF</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;(TTC, EN)&lt;/sub&gt;</td>
<td>TTC enable threshold voltage</td>
<td></td>
<td></td>
<td>200</td>
<td>mV</td>
</tr>
</tbody>
</table>

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### ELECTRICAL CHARACTERISTICS (continued)

**T<sub>J</sub> = 0°C to 125°C and recommended supply voltage range (unless otherwise stated)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Sleep Comparator</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;SLP-ENT&lt;/sub&gt; Sleep-mode entry threshold</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; ≤ V&lt;sub&gt;IBAT&lt;/sub&gt;, for 1 or 2 cells</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; ≤ V&lt;sub&gt;IBAT&lt;/sub&gt; +5 mV</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; ≤ V&lt;sub&gt;IBAT&lt;/sub&gt; +75 mV</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;SLP-EXIT&lt;/sub&gt; Sleep-mode exit hysteresis,</td>
<td>2.3 V ≤ V&lt;sub&gt;OUT&lt;/sub&gt; ≤ V&lt;sub&gt;REG&lt;/sub&gt;</td>
<td>40</td>
<td>160</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;SLP&lt;/sub&gt; Deglitch time for sleep mode</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 1 kΩ</td>
<td>5</td>
<td>μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;UVLO-ON&lt;/sub&gt; IC active threshold voltage</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; rising</td>
<td>3.15</td>
<td>3.30</td>
<td>3.50</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;UVLO&lt;/sub&gt; IC active threshold voltage</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; falling</td>
<td>120</td>
<td>150</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td><strong>PWM</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal P-channel MOSFET on-resistance</td>
<td>7 V ≤ V&lt;sub&gt;CC&lt;/sub&gt; ≤ V&lt;sub&gt;CC(max)&lt;/sub&gt;</td>
<td>400</td>
<td>mΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal N-channel MOSFET on-resistance</td>
<td>4.5 V ≤ V&lt;sub&gt;CC&lt;/sub&gt; ≤ 7 V</td>
<td>500</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal N-channel MOSFET on-resistance</td>
<td>4.5 V ≤ V&lt;sub&gt;CC&lt;/sub&gt; ≤ 7 V</td>
<td>130</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;OSC&lt;/sub&gt; Oscillator frequency</td>
<td></td>
<td>1.1</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D&lt;sub&gt;MAX&lt;/sub&gt; Maximum duty cycle</td>
<td></td>
<td></td>
<td>100%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D&lt;sub&gt;MN&lt;/sub&gt; Minimum duty cycle</td>
<td></td>
<td></td>
<td>0%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;FALL&lt;/sub&gt; Switching delay time (turn on)</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 1 kΩ</td>
<td>20</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;S&lt;/sub&gt; Minumum synchronous FET on time</td>
<td></td>
<td>60</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Synchronous FET minimum current-off threshold</td>
<td>(2)</td>
<td>50</td>
<td>400</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td><strong>Battery Detection</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;Detect&lt;/sub&gt; Battery detection current during time-out fault</td>
<td>V&lt;sub&gt;IBAT&lt;/sub&gt; &lt; V&lt;sub&gt;REG&lt;/sub&gt; – V&lt;sub&gt;RC&lt;/sub&gt;</td>
<td>2</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;BAT&lt;/sub&gt; Discharge current</td>
<td>V&lt;sub&gt;SHORT&lt;/sub&gt; &lt; V&lt;sub&gt;IBAT&lt;/sub&gt; &lt; V&lt;sub&gt;REG&lt;/sub&gt; – V&lt;sub&gt;RC&lt;/sub&gt;</td>
<td>400</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;BAT&lt;/sub&gt; Discharge time</td>
<td>V&lt;sub&gt;SHORT&lt;/sub&gt; &lt; V&lt;sub&gt;IBAT&lt;/sub&gt; &lt; V&lt;sub&gt;REG&lt;/sub&gt; – V&lt;sub&gt;RC&lt;/sub&gt;</td>
<td>1</td>
<td>s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;WAKE&lt;/sub&gt; Wake current</td>
<td>V&lt;sub&gt;SHORT&lt;/sub&gt; &lt; V&lt;sub&gt;IBAT&lt;/sub&gt; &lt; V&lt;sub&gt;REG&lt;/sub&gt; – V&lt;sub&gt;RC&lt;/sub&gt;</td>
<td>2</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;WAKE&lt;/sub&gt; Wake time</td>
<td>V&lt;sub&gt;SHORT&lt;/sub&gt; &lt; V&lt;sub&gt;IBAT&lt;/sub&gt; &lt; V&lt;sub&gt;REG&lt;/sub&gt; – V&lt;sub&gt;RC&lt;/sub&gt;</td>
<td>0.5</td>
<td>s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;BAT&lt;/sub&gt; Termination discharge current</td>
<td>Begins after termination detected, V&lt;sub&gt;IBAT&lt;/sub&gt; ≤ V&lt;sub&gt;REG&lt;/sub&gt;</td>
<td>400</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;BAT&lt;/sub&gt; Termination time</td>
<td></td>
<td>262</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Output Capacitor</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;OUT&lt;/sub&gt; Required output ceramic capacitor range from SNS to PGND, between inductor and R&lt;sub&gt;SNS&lt;/sub&gt;</td>
<td>4.7</td>
<td>10</td>
<td>47</td>
<td>μF</td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;SNS&lt;/sub&gt; Required SNS capacitor (ceramic) at SNS pin</td>
<td></td>
<td>0.1</td>
<td>μF</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Protection</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;OVP&lt;/sub&gt; OVP threshold voltage</td>
<td>Threshold over V&lt;sub&gt;REG&lt;/sub&gt; to turn off P-channel MOSFET, STAT1, and STAT2 during charge or termination states</td>
<td>110</td>
<td>117</td>
<td>121</td>
<td>%V&lt;sub&gt;REG&lt;/sub&gt;</td>
</tr>
<tr>
<td>I&lt;sub&gt;LIM&lt;/sub&gt; Cycle-by-cycle current limit</td>
<td></td>
<td>2.6</td>
<td>3.6</td>
<td>4.5</td>
<td>A</td>
</tr>
<tr>
<td>I&lt;sub&gt;SHORT&lt;/sub&gt; Short-circuit voltage threshold, BAT</td>
<td>V&lt;sub&gt;IBAT&lt;/sub&gt; falling</td>
<td>1.95</td>
<td>2</td>
<td>2.05</td>
<td>V/cell</td>
</tr>
<tr>
<td>I&lt;sub&gt;SHORT&lt;/sub&gt; Short-circuit current</td>
<td>V&lt;sub&gt;IBAT&lt;/sub&gt; ≤ V&lt;sub&gt;SHORT&lt;/sub&gt;</td>
<td>35</td>
<td>65</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>T&lt;sub&gt;SHUTDOWN&lt;/sub&gt; Thermal trip</td>
<td></td>
<td>165</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal hysteresis</td>
<td></td>
<td>10</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) For bq24105 and bq24115 only. R<sub>N</sub> is connected between IN and PGND pins and needed to ensure sleep entry.
(2) N-channel always turns on for ~60 ns and then turns off if current is too low.
<table>
<thead>
<tr>
<th>TERMINAL</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>BAT</td>
<td>14</td>
<td>Battery voltage sense input. Bypass it with a 0.1 ( \mu )F capacitor to PGND if there are long inductive leads to battery.</td>
</tr>
<tr>
<td>CE</td>
<td>16</td>
<td>Charger enable input. This active low input, if set high, suspends charge and places the device in the low-power sleep mode. Do not pull up this input to VTSB.</td>
</tr>
<tr>
<td>FB</td>
<td>13</td>
<td>Output voltage analog feedback adjustment. Connect the output of a resistive voltage divider powered from the battery terminals to this node to adjust the output battery voltage regulation.</td>
</tr>
<tr>
<td>IN</td>
<td>3, 4</td>
<td>Charger input voltage.</td>
</tr>
<tr>
<td>ISET1</td>
<td>8</td>
<td>Charger current set point 1 (fast charge). Use a resistor to ground to set this value.</td>
</tr>
<tr>
<td>ISET2</td>
<td>9</td>
<td>Charger current set point 2 (precharge and termination), set by a resistor connected to ground.</td>
</tr>
<tr>
<td>OUT</td>
<td>1, 20</td>
<td>Charge current output inductor connection. Connect a zener TVS diode between OUT pin and PGND pin to clamp the voltage spike to protect the power MOSFETs during abnormal conditions.</td>
</tr>
<tr>
<td>PG</td>
<td>5</td>
<td>Power-good status output (open drain). The transistor turns on when a valid ( V_{CC} ) is detected. It is turned off in the sleep mode. PG can be used to drive a LED or communicate with a host processor.</td>
</tr>
<tr>
<td>PGND</td>
<td>17, 18</td>
<td>Power ground input</td>
</tr>
<tr>
<td>SNS</td>
<td>15</td>
<td>Charge current-sense input. Battery current is sensed via the voltage drop developed on this pin by an external sense resistor in series with the battery pack. A 0.1- ( \mu )F capacitor to PGND is required.</td>
</tr>
<tr>
<td>STAT1</td>
<td>2</td>
<td>Charge status 1 (open-drain output). When the transistor turns on indicates charge in process. When it is off and with the condition of STAT2 indicates various charger conditions (see Table 1).</td>
</tr>
<tr>
<td>STAT2</td>
<td>19</td>
<td>Charge status 2 (open-drain output). When the transistor turns on indicates charge is done. When it is off and with the condition of STAT1 indicates various charger conditions (see Table 1).</td>
</tr>
<tr>
<td>TS</td>
<td>12</td>
<td>Temperature sense input. This input monitors its voltage against an internal threshold to determine if charging is allowed. Use an NTC thermistor and a voltage divider powered from VTSB to develop this voltage (see Figure 6).</td>
</tr>
<tr>
<td>TTC</td>
<td>7</td>
<td>Timer and termination control. Connect a capacitor from this node to GND to set the bqSWITCHER timer. When this input is low, the timer and termination detection are disabled.</td>
</tr>
<tr>
<td>VCC</td>
<td>6</td>
<td>Analog device input. A 0.1- ( \mu )F capacitor to VSS is required.</td>
</tr>
<tr>
<td>VSS</td>
<td>10</td>
<td>Analog ground input</td>
</tr>
<tr>
<td>VTSB</td>
<td>11</td>
<td>TS internal bias regulator voltage. Connect capacitor (with a value between a 0.1- ( \mu )F and 1- ( \mu )F) between this output and VSS.</td>
</tr>
<tr>
<td>Exposed Thermal Pad</td>
<td>Pad</td>
<td>There is an internal electrical connection between the exposed thermal pad and VSS. The exposed thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. The power pad can be used as a star ground connection between VSS and PGND. A common ground plane may be used. VSS pin must be connected to ground at all times.</td>
</tr>
</tbody>
</table>
Figure 1. Stand-Alone 2-Cell Application
TYPICAL OPERATING PERFORMANCE

EFFICIENCY

vs

CHARGE CURRENT

Figure 2.

EFFICIENCY

vs

CHARGE CURRENT

Figure 3.
*NOTE: If the TTC pin is pulled low, the safety timer and termination are disabled; the charger continues to regulate, and the STAT pins indicate charge in progress.

If the TTC pin is pulled high (VTSB), only the safety timer is disabled (termination is normal).

Figure 4. Stand-Alone Version Operational Flow Chart
DETAILED DESCRIPTION

The bqSWITCHER™ supports a precision Li-ion or Li-polymer charging system for one-, two-, or three-cell applications. See Figure 4 for a typical charge profile.

![Typical Charging Profile](image)

**Figure 5. Typical Charging Profile**

**PWM Controller**

The bq24105 provides an integrated fixed 1MHz frequency voltage-mode controller with Feed-Forward function to regulate charge current or voltage. This type of controller is used to help improve line transient response, thereby simplifying the compensation network used for both continuous and discontinuous current conduction operation. The voltage and current loops are internally compensated using a Type-III compensation scheme that provides enough phase boost for stable operation, allowing the use of small ceramic capacitors with very low ESR. There is a 0.5-V offset on the bottom of the PWM ramp to allow the device to operate between 0% to 100% duty cycle.

The internal PWM gate drive can directly control the internal PMOS and NMOS power MOSFETs. The high-side gate voltage swings from \( V_{CC} \) (when off), to \( V_{CC} - 6 \) (when on and \( V_{CC} \) is greater than 6 V) to help reduce the conduction losses of the converter by enhancing the gate an extra volt beyond the standard 5V. The low-side gate voltage swings from 6 V, to turn on the NMOS, down to PGND to turn it off. The bq24105 has two back to back common-drain P-MOSFETs on the high side. An input P-MOSFET prevents battery discharge when IN is lower than BAT. The second P-MOSFET behaves as the switching control FET, eliminating the need of a bootstrap capacitor.

Cycle-by-cycle current limit is sensed through the internal high-side sense FET. The threshold is set to a nominal 3.6A peak current. The low-side FET also has a current limit that decides if the PWM Controller will operate in synchronous or non-synchronous mode. This threshold is set to 100mA and it turns off the low-side NMOS before the current reverses, preventing the battery from discharging. Synchronous operation is used when the current of the low-side FET is greater than 100mA to minimize power losses.
Temperature Qualification

The bqSWITCHER continuously monitors battery temperature by measuring the voltage between the TS pin and VSS pin. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The bqSWITCHER compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the $V_{\text{LTF}}$-to-$V_{\text{HTF}}$ range. During the charge cycle (both precharge and fast charge), the battery temperature must be within the $V_{\text{LTF}}$-to-$V_{\text{TCC}}$ thresholds. If battery temperature is outside of this range, the bqSWITCHER suspends charge and waits until the battery temperature is within the $V_{\text{LTF}}$-to-$V_{\text{HTF}}$ range. The bqSWITCHER suspends charge by turning off the PWM and holding the timer value (i.e., timers are not reset during a suspend condition). Note that the bias for the external resistor divider is provided from the VTSB output. Applying a constant voltage between the $V_{\text{LTF}}$-to-$V_{\text{HTF}}$ thresholds to the TS pin disables the temperature-sensing feature.

$$V_{\text{TSB}} \times R_{\text{TH}} \times R_{\text{TH}} \times \left( \frac{1}{V_{\text{LTF}}} - \frac{1}{V_{\text{HTF}}} \right)$$

$$RT2 = \frac{R_{\text{TH}} \times \left( \frac{V_{\text{TSB}}}{V_{\text{HTF}}} - 1 \right)}{V_{\text{HTF}}} - R_{\text{TH}} \times \left( \frac{V_{\text{TSB}}}{V_{\text{LTF}}} - 1 \right)$$

$$RT1 = \frac{V_{\text{TSB}}}{V_{\text{LTF}}} - 1$$

$$\frac{1}{RT2} + \frac{1}{R_{\text{TH}}}$$

Where:

$$V_{\text{LTF}} = \frac{V_{\text{TSB}} \times \%_{\text{LTF}}}{100}$$

$$V_{\text{HTF}} = \frac{V_{\text{TSB}} \times \%_{\text{HTF}}}{100}$$

(1)

Battery Preconditioning (Precharge)

On power up, if the battery voltage is below the $V_{\text{LOWV}}$ threshold, the bqSWITCHER applies a precharge current, $I_{\text{PRECHG}}$, to the battery. This feature recharges deeply discharged cells. The bqSWITCHER activates a safety timer, $t_{\text{PRECHG}}$, during the conditioning phase. If the $V_{\text{LOWV}}$ threshold is not reached within the timer period, the bqSWITCHER turns off the charger and enunciates FAULT on the STATx pins. In the case of a FAULT condition, the bqSWITCHER reduces the current to $I_{\text{DETECT}}$. $I_{\text{DETECT}}$ is used to detect a battery replacement condition. Fault condition is cleared by POR or battery replacement.

---

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The magnitude of the precharge current, \( I_{O(PRECHG)} \), is determined by the value of programming resistor, \( R_{(ISET2)} \), connected to the ISET2 pin.

\[
I_{O(PRECHG)} = \frac{K_{(ISET2)} \times V_{(ISET2)}}{\left( R_{(ISET2)} \times R_{(SNS)} \right)}
\]

where

- \( R_{SNS} \) is the external current-sense resistor
- \( V_{(ISET2)} \) is the output voltage of the ISET2 pin
- \( K_{(ISET2)} \) is the V/A gain factor
- \( V_{(ISET2)} \) and \( K_{(ISET2)} \) are specified in the Electrical Characteristics table.

**Battery Charge Current**

The battery charge current, \( I_{O(CHARGE)} \), is established by setting the external sense resistor, \( R_{(SNS)} \), and the resistor, \( R_{(ISET1)} \), connected to the ISET1 pin.

In order to set the current, first choose \( R_{(SNS)} \) based on the regulation threshold \( V_{IREG} \) across this resistor. The best accuracy is achieved when the \( V_{IREG} \) is between 100 mV and 200 mV.

\[
R_{(SNS)} = \frac{V_{IREG}}{I_{O(CHARGE)}}
\]

If the results is not a standard sense resistor value, choose the next larger value. Using the selected standard value, solve for \( V_{IREG} \). Once the sense resistor is selected, the ISET1 resistor can be calculated using the following equation:

\[
R_{ISET1} = \frac{K_{ISET1} \times V_{ISET1}}{R_{SNS} \times I_{O(CHARGE)}}
\]

**Battery Voltage Regulation**

The voltage regulation feedback occurs through the BAT pin. This input is tied directly to the positive side of the battery pack. The bqSWITCHER monitors the battery-pack voltage between the BAT and VSS pins.

Output regulation voltage is specified as:

\[
V_{OREG} = \frac{(R1 + R2)}{R2} \times V_{IBAT}
\]

where \( R1 \) and \( R2 \) are resistor divider from BAT to FB and FB to VSS, respectively.

Recharge threshold voltage is specified as:

\[
V_{RCH} = \frac{(R1 + R2)}{R2 \times 50 \text{ mV}}
\]
Charge Termination and Recharge

The bqSWITCHER monitors the charging current during the voltage regulation phase. Once the termination threshold, $I_{\text{TERM}}$, is detected, the bqSWITCHER terminates charge. The termination current level is selected by the value of programming resistor, $R_{\text{ISET2}}$, connected to the ISET2 pin.

$$I_{\text{TERM}} = \frac{K_{\text{ISET2}} \times V_{\text{TERM}}}{R_{\text{ISET2}} \times R_{\text{SNS}}}$$  \hspace{1cm} (7)

where

$R_{\text{SNS}}$ is the external current-sense resistor
$V_{\text{TERM}}$ is the output of the ISET2 pin
$K_{\text{ISET2}}$ is the A/V gain factor
$V_{\text{TERM}}$ and $K_{\text{ISET2}}$ are specified in the Electrical Characteristics table

As a safety backup, the bqSWITCHER also provides a programmable charge timer. The charge time is programmed by the value of a capacitor connected between the TTC pin and GND by the following formula:

$$t_{\text{CHARGE}} = C_{\text{TTC}} \times K_{\text{TTC}}$$  \hspace{1cm} (8)

where

$C_{\text{TTC}}$ is the capacitor connected to the TTC pin
$K_{\text{TTC}}$ is the multiplier

A new charge cycle is initiated when one of the following conditions is detected:

• The battery voltage falls below the $V_{RCH}$ threshold.
• Power-on reset (POR), if battery voltage is below the $V_{RCH}$ threshold
• CE toggle
• TTC pin, described as follows.

In order to disable the charge termination and safety timer, the user can pull the TTC input below the $V_{\text{TTC, EN}}$ threshold. Going above this threshold enables the termination and safety timer features and also resets the timer. Tying TTC high disables the safety timer only.
Sleep Mode
The bqSWITCHER enters the low-power sleep mode if the VCC pin is removed from the circuit. This feature prevents draining the battery during the absence of VCC.

Charge Status Outputs
The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in Table 1. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates that the open-drain transistor is turned off.

<table>
<thead>
<tr>
<th>Charge State</th>
<th>STAT1</th>
<th>STAT2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Charge-in-progress</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>Charge complete</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>Charge suspend, timer fault, overvoltage, sleep mode, battery absent</td>
<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>

Table 2. Status Pins Summary

<table>
<thead>
<tr>
<th>Charge State</th>
<th>STAT1</th>
<th>STAT2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Battery absent</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>Charge-in-progress</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>Charge complete</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>Battery over discharge, $V_{\text{BAT}} &lt; V_{\text{SC}}$</td>
<td>ON/OFF (0.5 Hz)</td>
<td>OFF</td>
</tr>
<tr>
<td>Charge suspend (due to TS pin and internal thermal protection)</td>
<td>ON/OFF (0.5 Hz)</td>
<td>OFF</td>
</tr>
<tr>
<td>Precharge timer fault</td>
<td>ON/OFF (0.5 Hz)</td>
<td>OFF</td>
</tr>
<tr>
<td>Fast charge timer fault</td>
<td>ON/OFF (0.5 Hz)</td>
<td>OFF</td>
</tr>
<tr>
<td>Sleep mode</td>
<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>

PG Output
The open-drain PG (power good) indicates when the AC-to-DC adapter (i.e., $V_{CC}$) is present. The output turns on when sleep-mode exit threshold, $V_{\text{SLP-EXIT}}$, is detected. This output is turned off in the sleep mode. The PG pin can be used to drive an LED or communicate to the host processor.

CE Input (Charge Enable)
The CE digital input is used to disable or enable the charge process. A low-level signal on this pin enables the charge and a high-level $V_{CC}$ signal disables the charge. A high-to-low transition on this pin also resets all timers and fault conditions. Note that the CE pin cannot be pulled up to VTSB voltage. This may create power-up issues.
Timer Fault Recovery

As shown in Figure 6, bqSWITCHER provides a recovery method to deal with timer fault conditions. The following summarizes this method.

**Condition 1** \( V_{IBAT} \) above recharge threshold \( (V_{OREG} - V_{RCH}) \) and timeout fault occurs.

Recovery method: bqSWITCHER waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. Once the battery falls below the recharge threshold, the bqSWITCHER clears the fault and enters the battery absent detection routine. A POR or CE toggle also clears the fault.

**Condition 2** Charge voltage below recharge threshold \( (V_{OREG} - V_{RCH}) \) and timeout fault occurs

Recovery method: Under this scenario, the bqSWITCHER applies the \( I_{DETECT} \) current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the bqSWITCHER disables the \( I_{DETECT} \) current and executes the recovery method described in Condition 1. Once the battery falls below the recharge threshold, the bqSWITCHER clears the fault and enters the battery absent detection routine. A POR or CE toggle also clears the fault.

Output Overvoltage Protection

The bqSWITCHER provides a built-in overvoltage protection to protect the device and other components against damages if the battery voltage gets too high, as when the battery is suddenly removed. When an overvoltage condition is detected, this feature turns off the PWM and STATx pins. The fault is cleared once \( V_{IBAT} \) drops to the recharge threshold \( (V_{OREG} - V_{RCH}) \).

Inductor, Capacitor, and Sense Resistor Selection Guidelines

The bqSWITCHER provides internal loop compensation. With this scheme, best stability occurs when LC resonant frequency, \( f_0 \), is approximately 16 kHz (8 kHz to 32 kHz). Equation 9 can be used to calculate the value of the output inductor and capacitor. Table 3 provides a summary of typical component values for various charge rates.

\[
f_0 = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}}
\]  

(9)

<table>
<thead>
<tr>
<th>Table 3. Output Components Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CHARGE CURRENT</strong></td>
</tr>
<tr>
<td>---------------------</td>
</tr>
<tr>
<td>Output inductor, ( L_{OUT} )</td>
</tr>
<tr>
<td>Output capacitor, ( C_{OUT} )</td>
</tr>
<tr>
<td>Sense resistor, ( R_{SNS} )</td>
</tr>
</tbody>
</table>
Battery Detection

For applications with removable battery packs, bqSWITCHER provides a battery absent detection scheme to reliably detect insertion and/or removal of battery packs.

![Battery Absent Detection Diagram]

The voltage at the BAT pin is held above the battery recharge threshold, $V_{OREG} - V_{RCH}$, by the charged battery following fast charging. When the voltage at the BAT pin falls to the recharge threshold, either by a load on the battery or due to battery removal, the bqSWITCHER begins a battery absent detection test. This test involves enabling a detection current, $I_{DETECT1}$, for a period of $t_{DISCHARGE1}$ and checking to see if the battery voltage is below the short circuit threshold, $V_{SHORT}$. Following this, the wake current, $I_{WAKE}$, is applied for a period of $t_{WAKE}$ and the battery voltage is checked again to ensure that it is above the recharge threshold. The purpose of this current is to attempt to close an open battery pack protector, if one is connected to the bqSWITCHER.

Passing both of the discharge and charge tests indicates a battery absent fault at the STAT pins. Failure of either test starts a new charge cycle. For the absent battery condition, typically the voltage on the BAT pin rises and falls between 0V and $V_{OVP}$ thresholds indefinitely.
Battery Detection Example

In order to detect a no battery condition during the discharge and wake tests, the maximum output capacitance should not exceed the following:

a. Discharge ($I_{\text{DISCHRG1}} = 400 \, \mu\text{A}, t_{\text{DISCHRG1}} = 1\, \text{s}, V_{\text{SHORT}} = 2\, \text{V}$)

$$C_{\text{MAX\_DIS}} = \frac{I_{\text{DISCHRG1}} \times t_{\text{DISCHRG1}}}{V_{\text{OREG}} - V_{\text{SHORT}}}$$

$$C_{\text{MAX\_DIS}} = \frac{400 \, \mu\text{A} \times 1\, \text{s}}{4.2 \, \text{V} - 2 \, \text{V}}$$

$$C_{\text{MAX\_DIS}} = 182 \, \mu\text{F}$$

(10)

b. Wake ($I_{\text{WAKE}} = 2 \, \text{mA}, t_{\text{WAKE}} = 0.5 \, \text{s}, V_{\text{OREG}} - V_{\text{RCH}} = 4.1\, \text{V}$)

$$C_{\text{MAX\_WAKE}} = \frac{I_{\text{WAKE}} \times t_{\text{WAKE}}}{(V_{\text{OREG}} - V_{\text{RCH}}) - 0 \, \text{V}}$$

$$C_{\text{MAX\_WAKE}} = \frac{2 \, \text{mA} \times 0.5\, \text{s}}{(4.2 \, \text{V} - 0.1 \, \text{V}) - 0\, \text{V}}$$

$$C_{\text{MAX\_WAKE}} = 244 \, \mu\text{F}$$

(11)

Based on these calculations the recommended maximum output capacitance to ensure proper operation of the battery detection scheme is 100 $\mu\text{F}$ which will allow for process and temperature variations.

Figure 9 shows the battery detection scheme when a battery is inserted. Channel 3 is the output signal and Channel 4 is the output current. The output signal switches between $V_{\text{OREG}}$ and GND until a battery is inserted. Once the battery is detected, the output current increases from 0A to 1.3A, which is the programmed charge current for this application.
Figure 9. Battery Detection Waveform When a Battery is Inserted

Figure 10 shows the battery detection scheme when a battery is removed. Channel 3 is the output signal and Channel 4 is the output current. When the battery is removed, the output signal goes up due to the stored energy in the inductor and it crosses the $V_{OREG} - V_{RCH}$ threshold. At this point the output current goes to 0A and the IC terminates the charge process and turns on the $I_{DISCHG2}$ for $t_{DISCHG2}$. This causes the output voltage to fall down below the $V_{OREG} - V_{RCHG}$ threshold triggering a Battery Absent condition and starting the battery detection scheme.

Figure 10. Battery Detection Waveform When a Battery is Removed
Current Sense Amplifier

A current sense amplifier feature that translates the charge current into a DC voltage is offered. Figure 11 is a block diagram of this feature.

![Diagram of Current Sense Amplifier](image)

**Figure 11. Current Sense Amplifier**

The voltage on the ISET2 pin can be used to calculate the charge current. Equation 12 shows the relationship between the ISET2 voltage and the charge current:

\[
I_{\text{CHARGE}} = \frac{V_{\text{ISET2}} \times K_{\text{ISET2}}}{R_{\text{SNS}} \times R_{\text{SET2}}}
\]

(12)

This feature can be used to monitor the charge current (Figure 12) during the current regulation phase (Fastcharge only) and the voltage regulation phase. The schematic for the application circuit for this waveform is shown in Figure 14.

![Waveform of Current Sense Amplifier](image)

**Figure 12. Current Sense Amplifier Charge Current Waveform**
bqSWITCHER SYSTEM DESIGN EXAMPLE

The following section provides a detailed system design example for the bq24100.

System Design Specifications:
- $V_{IN} = 16V$
- $V_{BAT} = 4.2V$ (1-Cell)
- $I_{CHARGE} = 1.33$ A
- $I_{PRECHARGE} = I_{TERM} = 133$ mA
- Safety Timer = 5 hours
- Inductor Ripple Current = 30% of Fast Charge Current
- Initiate Charge Temperature = 0°C to 45°C

1. Determine the inductor value ($L_{OUT}$) for the specified charge current ripple:
   \[
   \Delta I_L = I_{CHARGE} \times I_{CHARGE} \text{Ripple}
   \]
   \[
   L_{OUT} = \frac{V_{BAT} \times (V_{INMAX} - V_{BAT})}{V_{INMAX} \times f \times \Delta I_L} \]
   \[
   L_{OUT} = \frac{4.2 \times (16 - 4.2)}{16 \times (1.1 \times 10^6) \times (1.33 \times 0.3)}
   \]
   \[
   L_{OUT} = 7.06 \mu H
   \]

Set the output inductor to standard 10 $\mu$H. Calculate the total ripple current with using the 10 $\mu$H inductor:
\[
\Delta I_L = \frac{V_{BAT} \times (V_{INMAX} - V_{BAT})}{V_{INMAX} \times f \times L_{OUT}}
\]
\[
\Delta I_L = \frac{4.2 \times (16 - 4.2)}{16 \times (1.1 \times 10^6) \times (10 \times 10^{-6})}
\]
\[
\Delta I_L = 0.282$ A
\]

Calculate the maximum output current (peak current):
\[
I_{LPK} = I_{OUT} + \frac{\Delta I_L}{2}
\]
\[
I_{LPK} = 1.33 + \frac{0.282}{2}
\]
\[
I_{LPK} = 1.471$ A
\]

Use standard 10 $\mu$H inductor with a saturation current higher than 1.471A. (i.e., Sumida CDRH74-100)
2. Determine the output capacitor value ($C_{OUT}$) using 16 kHz as the resonant frequency:

$$f_0 = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}}$$

$$C_{OUT} = \frac{1}{4\pi^2 \times f_0^2 \times L_{OUT}}$$

$$C_{OUT} = \frac{1}{4\pi^2 \times (16 \times 10^{-3})^2 \times (10 \times 10^{-6})}$$

$$C_{OUT} = 9.89 \mu \text{F} \quad (16)$$

Use standard value 10 \(\mu\)F, 25V, X5R, ±20% ceramic capacitor (i.e., Panasonic 1206 ECJ-3Y1B1E106M)

3. Determine the sense resistor using the following equation:

$$R_{SNS} = \frac{V_{RSNS}}{I_{CHARGE}} \quad (17)$$

In order to get better current regulation accuracy (±10%), let $V_{RSNS}$ be between 100 mV and 200 mV. Use $V_{RSNS} = 100$ mV and calculate the value for the sense resistor.

$$R_{SNS} = \frac{100 \text{ mV}}{1.33 \text{ A}}$$

$$R_{SNS} = 0.075 \Omega \quad (18)$$

This value is not standard in resistors. If this happens, then choose the next larger value which in this case is 0.1Ω. Using the same equation (15) the actual $V_{RSNS}$ will be 133mV. Calculate the power dissipation on the sense resistor:

$$P_{RSNS} = I_{CHARGE}^2 \times R_{SNS}$$

$$P_{RSNS} = 1.33^2 \times 0.1$$

$$P_{RSNS} = 176.9 \text{ mW} \quad (19)$$

Select standard value 100 mΩ, 0.25W 0805, 1206 or 2010 size, high precision sensing resistor. (i.e., Vishay CRCW1210-0R10F)

4. Determine $ISET_1$ resistor using the following equation:

$$R_{ISET1} = \frac{K_{ISET1} \times V_{ISET1}}{R_{SNS} \times I_{CHARGE}}$$

$$R_{ISET1} = \frac{1000 \times 1.0}{0.1 \times 1.33}$$

$$R_{ISET1} = 7.5 \text{ k}\Omega \quad (20)$$

Select standard value 7.5 kΩ, 1/16W ±1% resistor (i.e., Vishay CRCWD0603-7501-F)

5. Determine $ISET_2$ resistor using the following equation:

$$R_{ISET2} = \frac{K_{ISET2} \times V_{ISET2}}{R_{SNS} \times I_{PRECHARGE}}$$

$$R_{ISET2} = \frac{1000 \times 0.1}{0.1 \times 0.133}$$

$$R_{ISET2} = 7.5 \text{ k}\Omega \quad (21)$$

Select standard value 7.5 kΩ, 1/16W ±1% resistor (i.e., Vishay CRCWD0603-7501-F)
6. Determine TTC capacitor (\(TTC\)) for the 5.0 hours safety timer using the following equation:

\[
C_{TTC} = \frac{i_{\text{CHARGE}}}{K_{TTC}}
\]

\[
C_{TTC} = \frac{300 \text{ m}}{2.6 \text{ m/nF}}
\]

\[
C_{TTC} = 115.4 \text{ nF}
\]

(22)

Select standard value 100 nF, 16V, X7R, ±10% ceramic capacitor (i.e., Panasonic ECJ-1VB1C104K). Using this capacitor the actual safety timer will be 4.3 hours.

7. Determine TS resistor network for an operating temperature range from 0°C to 45°C.

![Figure 13. TS Resistor Network](image)

Assuming a 103AT NTC Thermistor on the battery pack, determine the values for RT1 and RT2 using the following equations:

\[
RT2 = \frac{V_{O(VTSB)} \times RTH_{\text{COLD}} \times RTH_{\text{HOT}} \times \left[ \frac{1}{V_{\text{LTF}}} - \frac{1}{V_{\text{HTF}}} \right]}{RTH_{\text{HOT}} \times \left( \frac{V_{O(VTSB)}}{V_{\text{HTF}}} - 1 \right) - RTH_{\text{COLD}} \times \left( \frac{V_{O(VTSB)}}{V_{\text{LTF}}} - 1 \right)}
\]

\[
RT1 = \frac{V_{O(VTSB)}}{V_{\text{LTF}}} - 1
\]

Where:

\[
V_{\text{LTF}} = V_{O(VTSB)} \times \%_{\text{LTF-100}} / 100
\]

\[
V_{\text{HTF}} = V_{O(VTSB)} \times \%_{\text{HTF-100}} / 100
\]

(23)

\[
RTH_{\text{COLD}} = 27.28 \text{ k}\Omega
\]

\[
RTH_{\text{HOT}} = 4.912 \text{ k}\Omega
\]

\[
RT1 = 9.31 \text{ k}\Omega
\]

\[
RT2 = 442 \text{ k}\Omega
\]

(24)
APPLICATION INFORMATION

Charging Battery and Powering System Without Affecting Battery Charge and Termination

Figure 14. Application Circuit for Charging a Battery and Powering a System Without Affecting Termination

The bqSWITCHER was designed as a stand-alone battery charger but can be easily adapted to power a system load, while considering a few minor issues.

Advantages:
1. The charger controller is based only on what current goes through the current-sense resistor (so precharge, constant current, and termination all work well), and is not affected by the system load.
2. The input voltage has been converted to a usable system voltage with good efficiency from the input.
3. Extra external FETs are not needed to switch power source to the battery.
4. The TTC pin can be grounded to disable termination and keep the converter running and the battery fully charged, or let the switcher terminate when the battery is full and then run off of the battery via the sense resistor.

Other Issues:
1. If the system load current is large (≥ 1 A), the IR drop across the battery impedance causes the battery voltage to drop below the refresh threshold and start a new charge. The charger would then terminate due to low charge current. Therefore, the charger would cycle between charging and termination. If the load is smaller, the battery would have to discharge down to the refresh threshold resulting in a much slower cycling. Note that grounding the TTC pin keeps the converter on continuously.
2. If TTC is grounded, the battery is kept at 4.2 V (not much different than leaving a fully charged battery set unloaded).
3. Efficiency declines 2-3% hit when discharging through the sense resistor to the system.
Using bq24105 to Charge LiFePO₄ Battery

The LiFePO₄ battery has many unique features such as a high thermal runaway temperature, discharge current capability, and charge current. These special features make it attractive in many applications such as power tools. The recommended charge voltage is 3.6 V and termination current is 50 mA. Figure 15 shows an application circuit for charging one cell LiFePO₄ using bq24105. The charge voltage is 3.6 V and recharge voltage is 3.516 V. The fast charging current is set to 1.33 A while the termination current is 50 mA. This circuit can be easily changed to support two or three cell applications. However, only 84 mV difference between regulation set point and rechargeable threshold makes it frequently enter into recharge mode when small load current is applied. This can be solved by lower down the recharge voltage threshold to 200 mV to discharge more energy from the battery before it enters recharge mode again. See the application report, Using the bq24105/25 to Charge LiFePO₄ Battery (SLUA443), for additional details. The recharge threshold should be selected according to real application conditions.

Figure 15. 1-Cell LiFePO₄ Application
THERMAL CONSIDERATIONS

The SWITCHER is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application report entitled: QFN/SON PCB Attachment (SLUA271).

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

\[
\theta_{(JA)} = \frac{T_J - T_A}{P}
\]  

Where:
- \( T_J \) = chip junction temperature
- \( T_A \) = ambient temperature
- \( P \) = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:
- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

The device power dissipation, \( P \), is a function of the charge rate and the voltage drop across the internal power FET. It can be calculated from the following equation:

\[
P = [Vin \times \text{lin} - Vbat \times \text{Ibat}]
\]

Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. (See Figure 5.)
PCB LAYOUT CONSIDERATION

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the power input capacitors, connected from input to PGND, should be placed as close as possible to the bqSWITCHER. The output inductor should be placed directly above the IC and the output capacitor connected between the inductor and PGND of the IC. The intent is to minimize the current path loop area from the OUT pin through the LC filter and back to the GND pin. The sense resistor should be adjacent to the junction of the inductor and output capacitor. Route the sense leads connected across the \( R_{(SNS)} \) back to the IC, close to each other (minimize loop area) or on top of each other on adjacent layers (do not route the sense leads through a high-current path). Use an optional capacitor downstream from the sense resistor if long (inductive) battery leads are used.

- Place all small-signal components (\( C_{TTIC} \), RSET1/2 and TS) close to their respective IC pin (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.

- The PCB should have a ground plane (return) connected directly to the return of all components through vias (three vias per capacitor for power-stage capacitors, three vias for the IC PGND, one via per capacitor for small-signal components). A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is not a ground-bounce issue, and having the components segregated minimizes coupling between signals.

- The high-current charge paths into IN and from the OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins should be connected to the ground plane to return current through the internal low-side FET. The thermal vias in the IC PowerPAD™ provide the return-path connection.

- The bqSWITCHER is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the PCB. Full PCB design guidelines for this package are provided in the application report entitled: QFN/SON PCB Attachment (SLUA271). Six 10-mil to 13-mil vias are a minimum number of recommended vias, placed in the IC’s power pad, connecting it to a ground thermal plane on the opposite side of the PWB. This plane must be at the same potential as \( V_{SS} \) and PGND of this IC.

- See user guide SLUU200 for an example of good layout.

WAVEFORMS: All waveforms are taken at Lout (IC Out pin). \( V_{IN} = 7.6 \) V and the battery was set to 2.6 V, 3.5 V, and 4.2 V for the three waveforms. When the top switch of the converter is on, the waveform is at ~7.5 V, and when off, the waveform is near ground. Note that the ringing on the switching edges is small. This is due to a tight layout (minimized loop areas), a shielded inductor (closed core), and using a low-inductive scope ground lead (i.e., short with minimum loop).
Precharge: The current is low in precharge; so, the bottom synchronous FET turns off after its minimum on-time which explains the step between ≈0 V and -0.5 V. When the bottom FET and top FET are off, the current conducts through the body diode of the bottom FET which results in a diode drop below the ground potential. The initial negative spike is the delay turning on the bottom FET, which is to prevent shoot-through current as the top FET is turning off.

Fast Charge: This is captured during the constant-current phase. The two negative spikes are the result of the short delay when switching between the top and bottom FETs. The break-before-make action prevents current shoot-through and results in a body diode drop below ground potential during the break time.

Charge during Voltage Regulation and Approaching Termination: Note that this waveform is similar to the precharge waveform. The difference is that the battery voltage is higher so the duty cycle is slightly higher. The bottom FET stays on longer because there is more of a current load than during precharge; it takes longer for the inductor current to ramp down to the current threshold where the synchronous FET is disabled.
## REVISION HISTORY

**Changes from Original (August, 2009) to Revision A**

<table>
<thead>
<tr>
<th>Description</th>
<th>Page</th>
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<tbody>
<tr>
<td>Updated $V_{OREG}$ formula to match the BQ24105 commercial datasheet.</td>
<td>13</td>
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<tr>
<td>Orderable Device</td>
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<tr>
<td>BQ24105IRHLRQ1</td>
<td>ACTIVE</td>
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(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**OTHER QUALIFIED VERSIONS OF BQ24105-Q1**:
Catalog: BQ24105

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product
**TAPE AND REEL INFORMATION**

*All dimensions are nominal*

<table>
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<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
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<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
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**TAPE DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**REEL DIMENSIONS**

- Reel Diameter
- Reel Width (W1)

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Pocket Quadrants
- Sprocket Holes
- User Direction of Feed
### TAPE AND REEL BOX DIMENSIONS

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*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.