

## CMOS 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

### High-Voltage Types (20-Volt Rating)

■ CD4034B is a static eight-stage parallel-or serial-input parallel-output register. It can be used to:

1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B), and PARALLEL/SERIAL (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (3-state outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

### PARALLEL OPERATION

A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is low. If the A/S input is high the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs); a low A/B signal reverses the direction of data flow.

The AE input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high.

Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

### Applications:

- Parallel Input/Parallel Output, Serial Input/Parallel Output, Serial Input/Serial Output Register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-Down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

### SERIAL OPERATION

A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed).

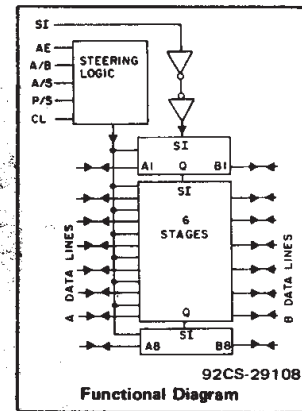
The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high).

Register expansion can be accomplished by simply cascading CD4034B packages.

The CD4034B types are supplied in 24-lead hermetic dual-in-line ceramic packages (F3A suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead small-outline packages (M, M96, and NSR suffixes), and 24-lead thin shrink small-outline packages (PW and PWR suffixes).

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	
Voltages referenced to $V_{SS}$ Terminal)	–0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	500mW
For $T_A = +100^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Derate Linearly at 12mW/ $^{\circ}\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	–55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	–65 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265 $^{\circ}\text{C}$



### Features:

- Bidirectional parallel data input
- Parallel or serial inputs/parallel outputs
- Asynchronous or synchronous parallel data loading
- Parallel data-input enable on "A" data lines (3-state output)
- Data recirculation for register expansion
- Multipackage register expansion
- Fully static operation dc-to-10 MHz (typ.) at  $V_{DD} = 10\text{ V}$
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1  $\mu\text{A}$  at 18 V over full package-temperature range; 100 nA at 18 V and 25 $^{\circ}\text{C}$
- Noise margin (over full package-temperature range):
  - 1 V at  $V_{DD} = 5\text{ V}$
  - 2 V at  $V_{DD} = 10\text{ V}$
  - 2.5 V at  $V_{DD} = 15\text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

# CD4034B Types

RECOMMENDED OPERATING CONDITIONS at  $T_A = 25^\circ\text{C}$ , Except as Noted.  
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	$V_{DD}$ (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A = \text{Full Package-Temperature Range}$ )		3	18	V
Data Setup Time, $t_S$	Serial Data to Clock	5	160	ns
		10	60	
		15	40	
	Parallel Data to Clock	5	50	ns
		10	30	
		15	20	
Clock Pulse Width, $t_W$	5	350	ns	
	10	140		
	15	80		
Clock Input Frequency, $f_{CL}$	5	dc	MHz	
	10	5		
	15	7		
Clock Input Rise or Fall Time, $t_{rCL}$ , $t_{fCL}^*$	5, 10, 15	—	15	$\mu\text{s}$

\*If more than one unit is cascaded  $t_{rCL}$  should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

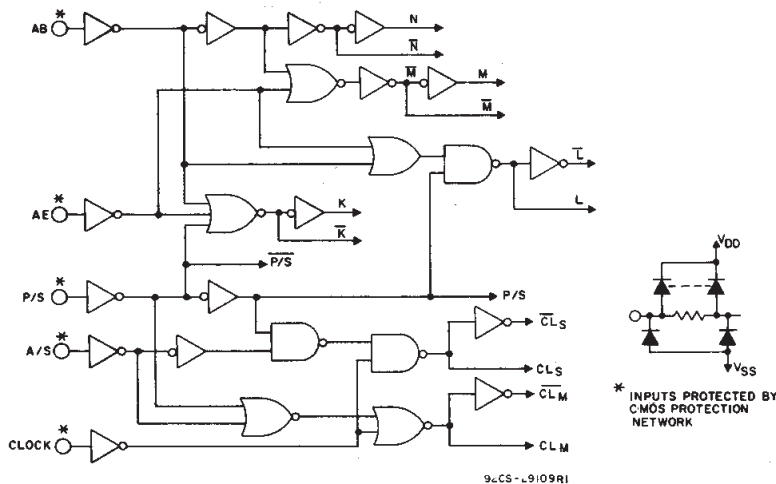


Fig. 1 — Steering logic diagram.

### FLIP-FLOP TRUTH TABLE

INPUTS		D	Q
$\overline{CLM}$	$\overline{CLS}$		
Low	Low	0	0
High	Low	0	0
Low	High	0	INVALID CONDITION
High	High	X	0
Low	Low	1	1
High	Low	1	1
Low	High	1	INVALID CONDITION

1 = High Level    0 = Low Level    X = Don't Care

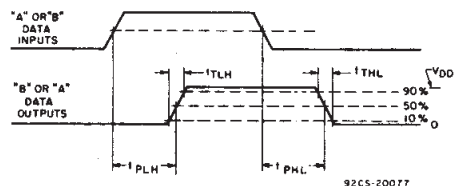
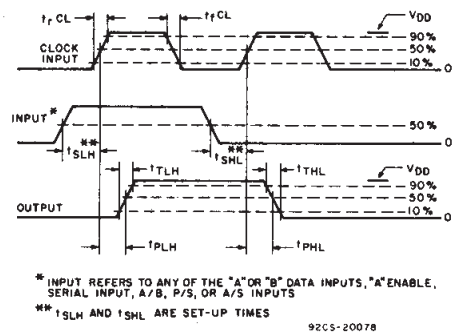


Fig. 2 — Asynchronous operation propagation delay time and transition time.



\* INPUT REFERS TO ANY OF THE "A" OR "B" DATA INPUTS, "A" ENABLE, SERIAL INPUT, A/B, P/S, OR A/S INPUTS

\*\*  $t_{SLH}$  AND  $t_{SHL}$  ARE SET-UP TIMES

Fig. 3 — Synchronous operation propagation delay times, transition times, and set-up times.

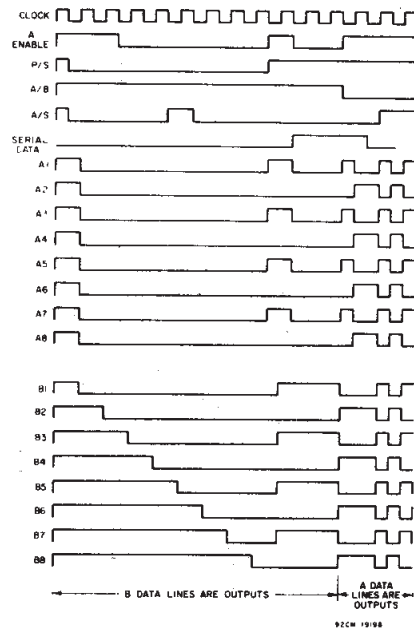


Fig. 4 — Timing diagram.

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# CD4034B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	-	0.5	5	5	5	150	150	-	0.04	5	μA
	-	0.10	10	10	10	300	300	-	0.04	10	
	-	0.15	15	20	20	600	600	-	0.04	20	
	-	0.20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I <sub>OL</sub> Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	-	0.5	5	0.05				-	0	0.05	V
	-	0.10	10	0.05				-	0	0.05	
	-	0.15	15	0.05				-	0	0.05	
Output Voltage: High-Level, V <sub>OH</sub> Min.	-	0.5	5	4.95				4.95	5	-	V
	-	0.10	10	9.95				9.95	10	-	
	-	0.15	15	14.95				14.95	15	-	
Input Low Voltage V <sub>IL</sub> Max.	0.5, 4.5	-	5	1.5				-	-	1.5	V
	1.9	-	10	3				-	-	3	
	1.5, 13.5	-	15	4				-	-	4	
Input High Voltage, V <sub>IH</sub> Min.	0.5, 4.5	-	5	3.5				3.5	-	-	V
	1.9	-	10	7				7	-	-	
	1.5, 13.5	-	15	11				11	-	-	
Input Current* I <sub>IN</sub> Max.	-	0.18	18	±0.1	±0.1	±1	±1	-	±10 <sup>-5</sup>	±0.1	μA
3-State Output Leakage Current I <sub>OUT</sub> Max.	0.18	0.18	18	±0.4	±0.4	±12	±12	-	±10 <sup>-4</sup>	±0.4	μA

\* All inputs except A and B Lines.

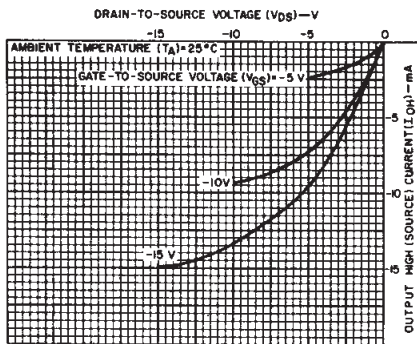


Fig. 8 - Minimum output high (source) current characteristics.

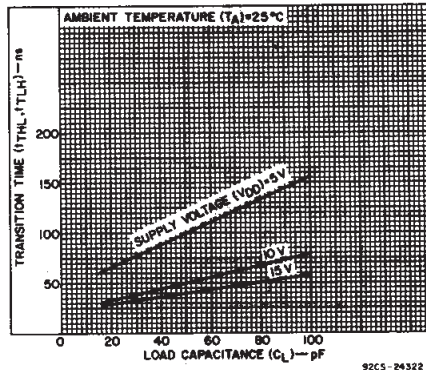


Fig. 9 - Typical transition time as a function of load capacitance.

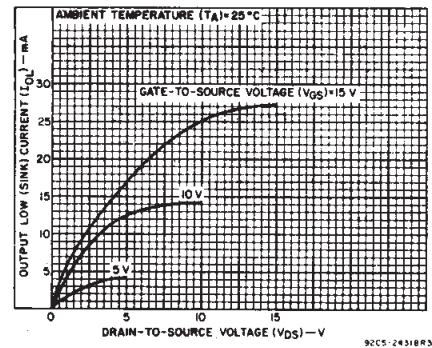


Fig. 5 - Typical output low (sink) current characteristics.

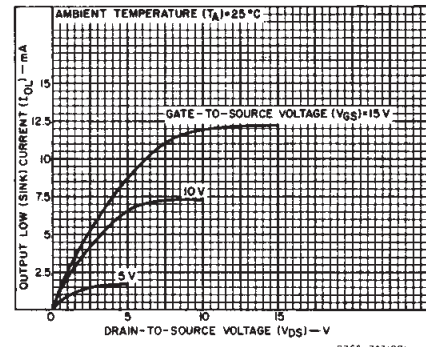


Fig. 6 - Minimum output low (sink) current characteristics.

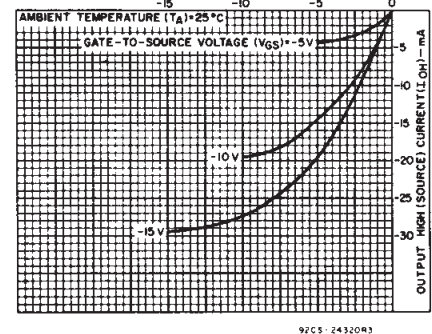


Fig. 7 - Typical output high (source) current characteristics.

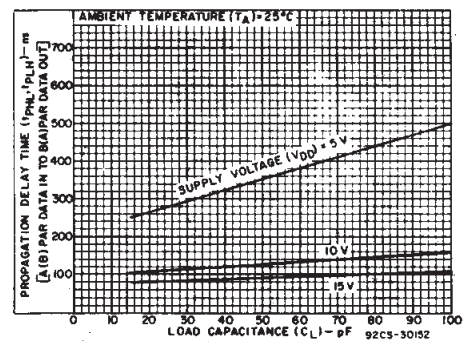


Fig. 10 - Typical propagation delay time as a function of load capacitance [A(B) parallel Data Input to B(A) parallel Data Output, synchronous or asynchronous].

# CD4034B Types

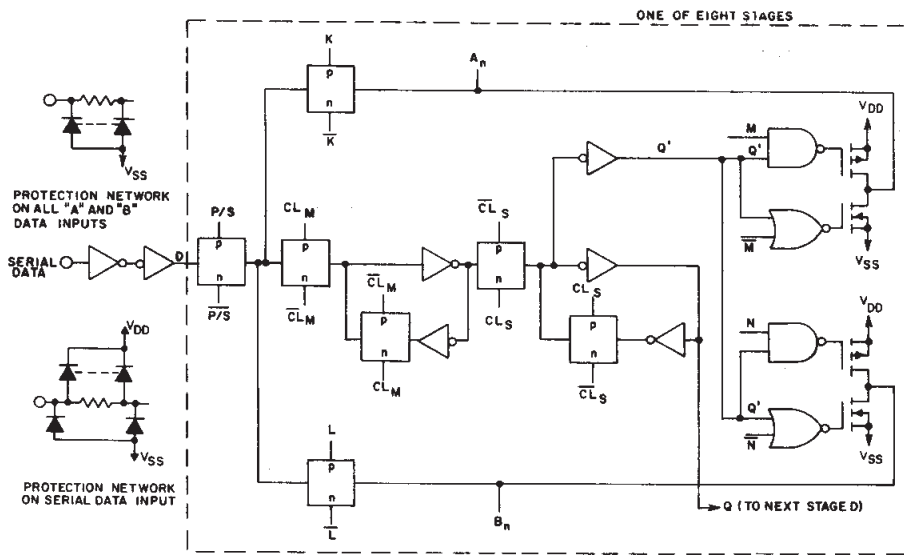


Fig. 11 - Register stage logic diagram (1 of 8 stages).

TRUTH TABLE FOR REGISTER INPUT-LEVELS AND RESULTING REGISTER OPERATION

"A" Enable	P/S	A/B	A/S	Operation*
0	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
0	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
0	1	0	0	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	1	0	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch. Data Recirculation
0	1	1	1	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch. Data Recirculation
1	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
1	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
1	1	0	0	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
1	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
1	1	1	0	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
1	1	1	1	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

\*Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode. During transfer from parallel to serial operation A/S should remain low in order to prevent  $D_S$  transfer into Flip Flops.

1 = HIGH LEVEL      0 = LOW LEVEL      X = DON'T CARE

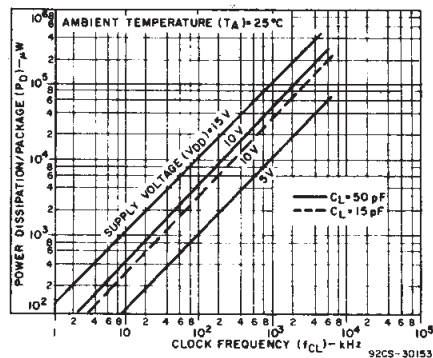


Fig. 12 - Typical dynamic power dissipation as a function of clock frequency.

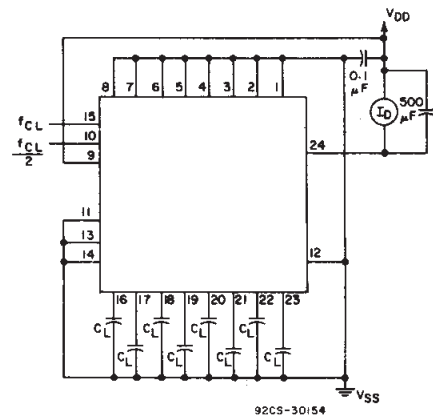


Fig. 13 - Dynamic power dissipation test circuit.

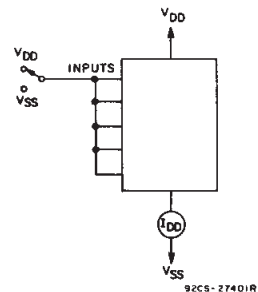


Fig. 14 - Quiescent device current test circuit.

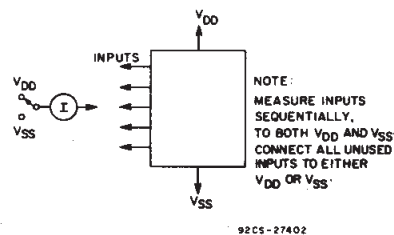


Fig. 15 - Input current test circuit.

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# CD4034B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  
 $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	$V_{DD}$ (V)	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Propagation Delay Time, $t_{PHL}, t_{PLH}$	5	—	350	700	ns
A(B) Parallel Data In to	10	—	120	240	
B(A) Parallel Data Out	15	—	85	170	
Serial to Parallel Data Out					
3-State Propagation Delay $t_{PLZ}, t_{PHZ}$	5	—	200	400	
A/B or AE to "A" OUT $t_{PZL}, t_{PZH}$	10	—	80	160	
	15	—	60	120	
Transition Time, $t_{THL}, t_{TLH}$	5	—	100	200	
	10	—	50	100	
	15	—	40	80	
Minimum Data Setup Time, $t_{SU}$	5	—	80	160	ns
Serial Data to Clock	10	—	30	60	
	15	—	20	40	
Parallel Data to Clock	5	—	25	50	ns
	10	—	15	30	
	15	—	10	20	
Minimum Data Hold Time, $t_H$	5	—	—	50	ns
	10	—	—	15	
	15	—	—	10	
Minimum High-Level Pulse Width, $t_w$	5	—	175	350	ns
AE, P/S, A/S	15	—	40	80	
Maximum Clock Frequency, $f_{CL}$	5	2	4	—	MHz
	10	5	10	—	
	15	7	14	—	
Minimum Clock Pulse Width, $t_w$	5	—	125	250	ns
	10	—	50	100	
	15	—	35	70	
Maximum Clock Rise or Fall Time, $t_{CL}, t_{CL}^*$	5,10,15	—	—	15	$\mu\text{s}$
Input Capacitance, $C_{IN}$	Any Input	—	5	7.5	pF

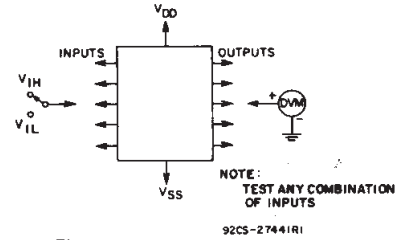


Fig. 16 — Input-voltage test circuit.

## Applications

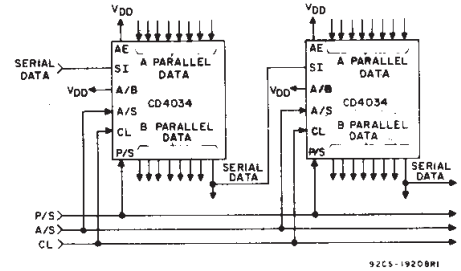


Fig. 17 — 16-bit parallel in/parallel out, parallel in/serial out, serial in/parallel out, serial in/serial out register.

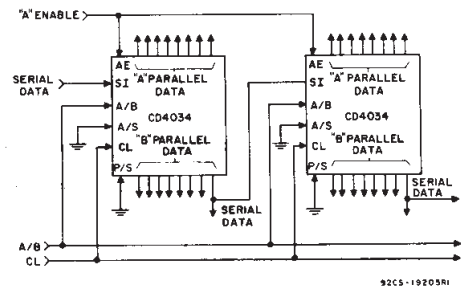
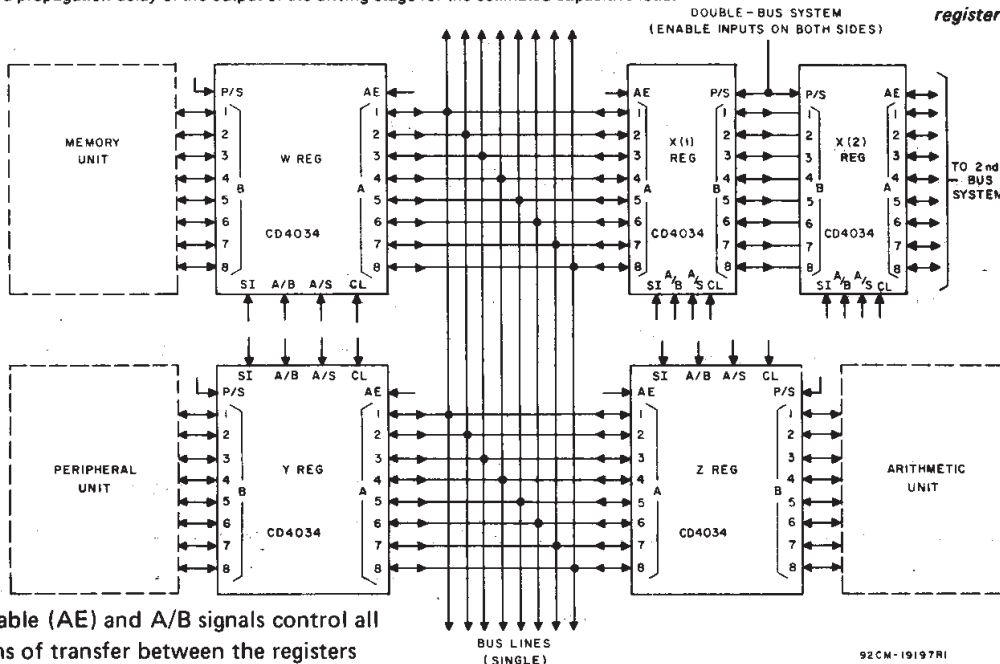


Fig. 18 — 16-bit serial in/gated parallel out register.

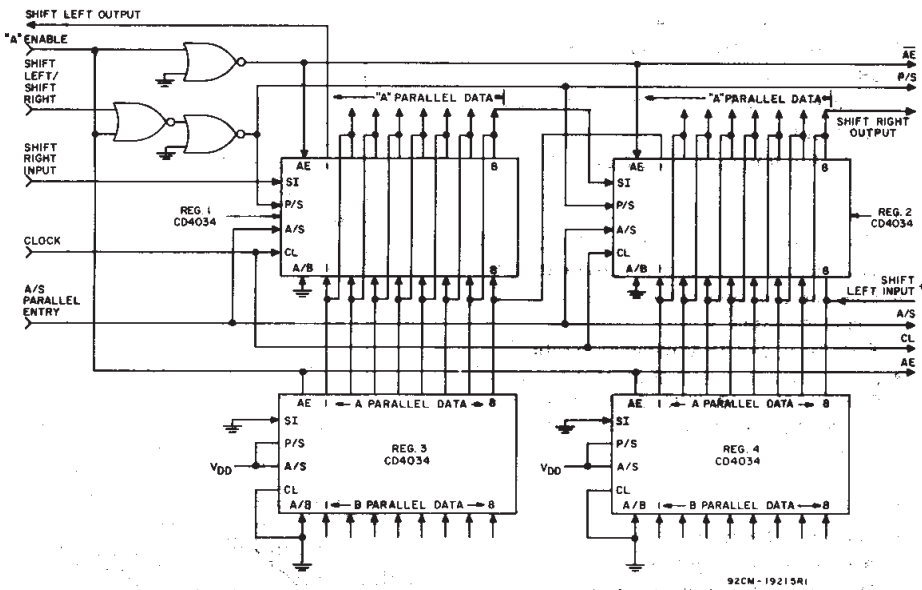
\*If more than one unit is cascaded  $t_{CL}$  should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.



The "A" enable (AE) and A/B signals control all combinations of transfer between the registers and bus systems.

Fig. 19 — Single- and double-bus systems.

# CD4034B Types



A "High" ("Low") on the shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data

into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

\* Shift left input must be disabled during parallel entry.

Fig. 20 - Shift right/shift left with parallel inputs.

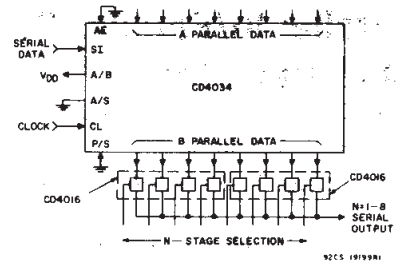


Fig. 21 - N-stage shift register with fixed serial output line.

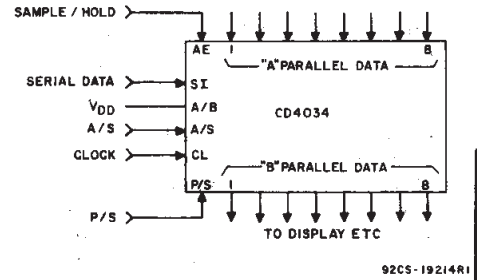
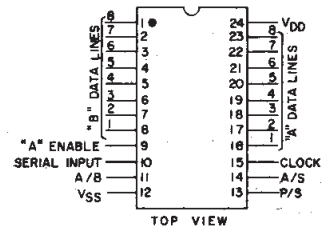
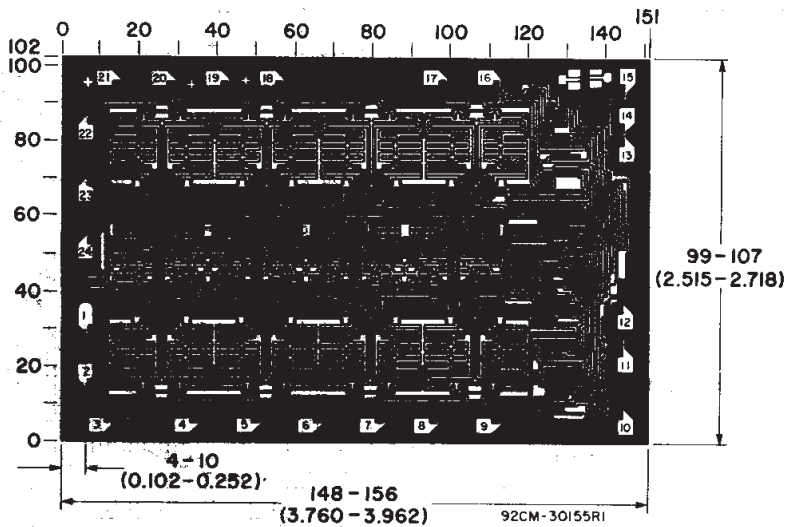


Fig. 22 - Sample and hold register-serial/parallel in-parallel out.





TERMINAL DIAGRAM



Dimensions and pad layout for CD4034BH.

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4034BF3A	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	CD4034BF3A	
CD4034BM	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4034BM	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD4034B, CD4034B-MIL :**

- Catalog: [CD4034B](#)
- Military: [CD4034B-MIL](#)

NOTE: Qualified Version Definitions:

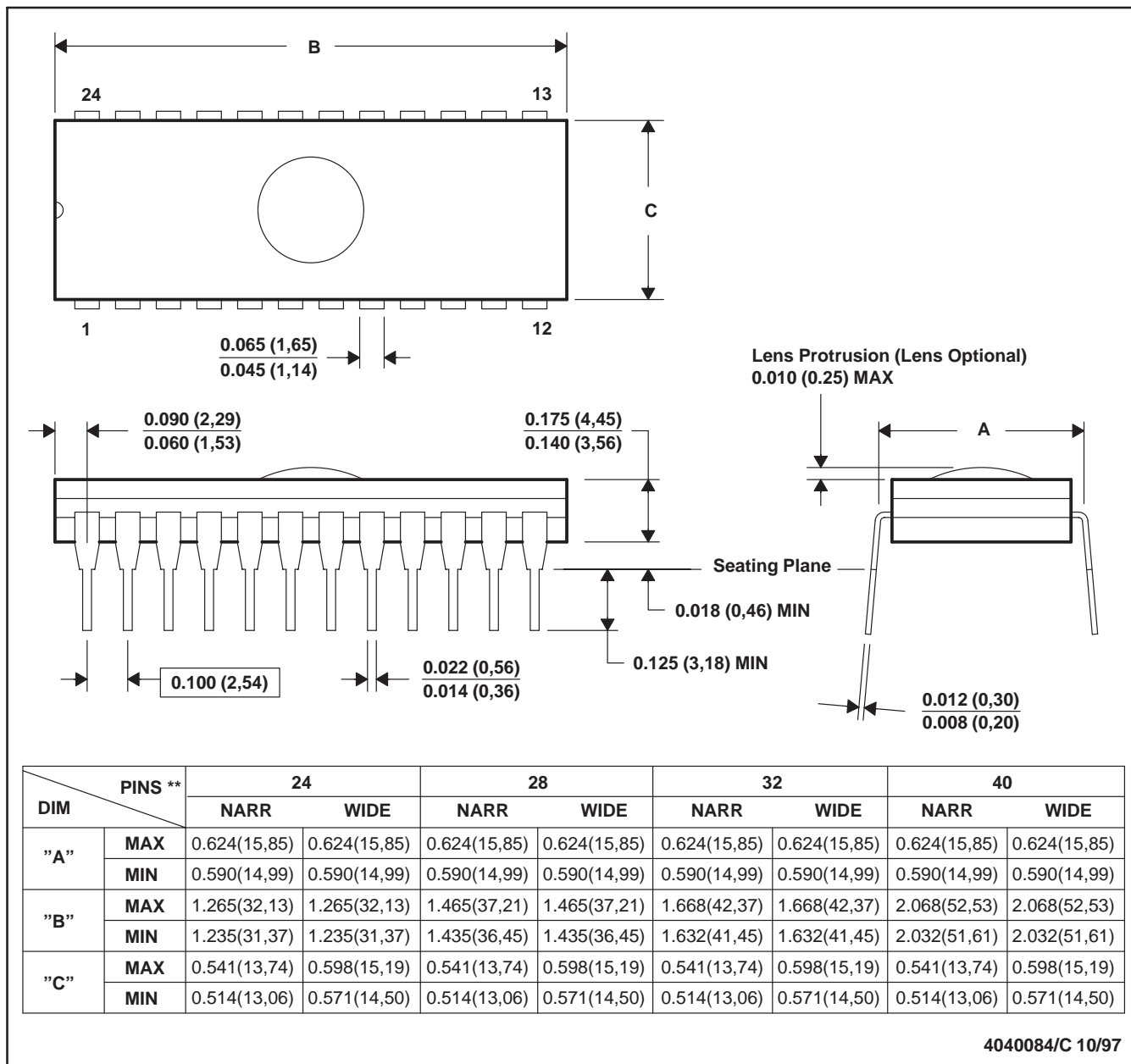
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



J (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).  
 D. This package can be hermetically sealed with a ceramic lid using glass frit.  
 E. Index point is provided on cap for terminal identification.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

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