

## High-Speed CMOS Logic Quad Bilateral Switch

February 1998 - Revised August 2004

### Features

- **Wide Analog-Input-Voltage Range** . . . . . 0V to 10V
- **Low "ON" Resistance**
  - 45Ω (Typ) . . . . .  $V_{CC} = 4.5V$
  - 35Ω (Typ) . . . . .  $V_{CC} = 6V$
  - 30Ω (Typ) . . . . .  $1fV_{CC} = 9V$
- **Fast Switching and Propagation Delay Times**
- **Low "OFF" Leakage Current**
- **Built-In "Break-Before-Make" Switching**
- **Suitable for Sample and Hold Applications**
- **Wide Operating Temperature Range** . . . -55°C to 125°C
- **HC Types**
  - 2V to 10V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$

### Description

The CD74HC4016 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

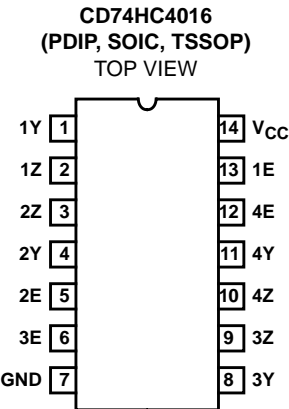
Each switch has two input/output terminals (nY, nZ) and an active high enable input (nE). Current through the switch will not cause additional  $V_{CC}$  current provided the analog voltage is maintained between  $V_{CC}$  and GND.

### Ordering Information

| PART NUMBER   | TEMP. RANGE (°C) | PACKAGE     |
|---------------|------------------|-------------|
| CD74HC4016E   | -55 to 125       | 14 Ld PDIP  |
| CD74HC4016M   | -55 to 125       | 14 Ld SOIC  |
| CD74HC4016MT  | -55 to 125       | 14 Ld SOIC  |
| CD74HC4016M96 | -55 to 125       | 14 Ld SOIC  |
| CD74HC4016PW  | -55 to 125       | 14 Ld TSSOP |
| CD74HC4016PWR | -55 to 125       | 14 Ld TSSOP |

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

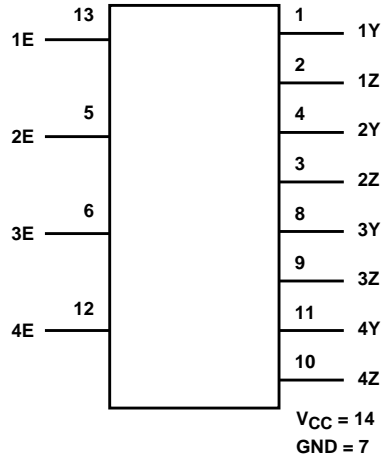
### Pinout



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

# CD74HC4016

## Functional Diagram

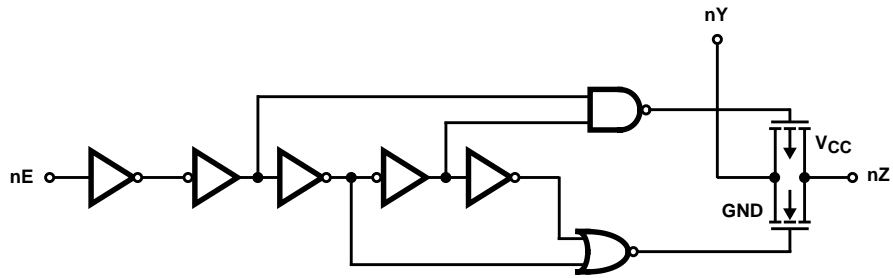


TRUTH TABLE

| INPUT<br>nE | SWITCH |
|-------------|--------|
| L           | OFF    |
| H           | ON     |

H = High Level Voltage  
L = Low Level Voltage

## Logic Diagram



# CD74HC4016

## Absolute Maximum Ratings

|  |             |
|--|-------------|
| DC Supply Voltage, $V_{CC}$ .....                      | -0.5V to 7V |
| DC Input Diode Current, $I_{IK}$                       |             |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....       | $\pm 20mA$  |
| DC Drain Current, per Output, $I_O$                    |             |
| For $-0.5V < V_O < V_{CC} + 0.5V$ .....                | $\pm 25mA$  |
| DC Output Diode Current, $I_{OK}$                      |             |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....       | $\pm 20mA$  |
| DC Output Source or Sink Current per Output Pin, $I_O$ |             |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....       | $\pm 25mA$  |
| DC $V_{CC}$ or Ground Current, $I_{CC}$ .....          | $\pm 50mA$  |

## Thermal Information

|  |                                    |
|--|------------------------------------|
| Thermal Resistance (Typical, Note 1)                 | $\theta_{JA}$ ( $^{\circ}C/W$ )    |
| E (PDIP) Package .....                               | 80                                 |
| M (SOIC) Package .....                               | 86                                 |
| PW (TSSOP) Package .....                             | 96                                 |
| Maximum Junction Temperature (Plastic Package) ..... | 150 $^{\circ}C$                    |
| Maximum Storage Temperature Range .....              | -65 $^{\circ}C$ to 150 $^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) .....       | 300 $^{\circ}C$                    |

## Operating Conditions

|  |                                    |
|--|------------------------------------|
| Temperature Range, $T_A$ .....               | -55 $^{\circ}C$ to 125 $^{\circ}C$ |
| Supply Voltage Range, $V_{CC}$               |                                    |
| HC Types .....                               | .2V to 10V                         |
| DC Input or Output Voltage, $V_I, V_O$ ..... | 0V to $V_{CC}$                     |
| Input Rise and Fall Time                     |                                    |
| 2V .....                                     | 1000ns (Max)                       |
| 4.5V .....                                   | 500ns (Max)                        |
| 6V .....                                     | 400ns (Max)                        |
| 9V .....                                     | 250ns (Max)                        |

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER  | SYMBOL          | TEST CONDITIONS         |                    |              | 25 $^{\circ}C$ |     |           | -40 $^{\circ}C$ TO 85 $^{\circ}C$ |         | -55 $^{\circ}C$ TO 125 $^{\circ}C$ |         | UNITS    |
|--|-----------------|-------------------------|--------------------|--------------|----------------|-----|-----------|-----------------------------------|---------|------------------------------------|---------|----------|
|  |                 | $V_I$ (V)               | $V_{IS}$ (V)       | $V_{CC}$ (V) | MIN            | TYP | MAX       | MIN                               | MAX     | MIN                                | MAX     |          |
| <b>HC TYPES</b>                                  |                 |                         |                    |              |                |     |           |                                   |         |                                    |         |          |
| High Level Input Voltage                         | $V_{IH}$        | -                       | -                  | 2            | 1.5            | -   | -         | 1.5                               | -       | 1.5                                | -       | V        |
|  |                 |                         |                    | 4.5          | 3.15           | -   | -         | 3.15                              | -       | 3.15                               | -       | V        |
|  |                 |                         |                    | 6            | 4.2            | -   | -         | 4.2                               | -       | 4.2                                | -       | V        |
| Low Level Input Voltage                          | $V_{IL}$        | -                       | -                  | 2            | -              | -   | 0.5       | -                                 | 0.5     | -                                  | 0.5     | V        |
|  |                 |                         |                    | 4.5          | -              | -   | 1.35      | -                                 | 1.35    | -                                  | 1.35    | V        |
|  |                 |                         |                    | 6            | -              | -   | 1.8       | -                                 | 1.8     | -                                  | 1.8     | V        |
| "ON" Resistance<br>$I_O = 1mA$                   | $R_{ON}$        | $V_{IH}$ or<br>$V_{IL}$ | $V_{CC}$ or<br>GND | 4.5          | -              | 45  | 180       | -                                 | 225     | -                                  | 270     | $\Omega$ |
|  |                 |                         |                    | 6            | -              | 35  | 160       | -                                 | 200     | -                                  | 240     | $\Omega$ |
|  |                 |                         |                    | 9            | -              | 30  | 135       | -                                 | 170     | -                                  | 205     | $\Omega$ |
|  |                 |                         |                    | 4.5          | -              | 85  | 320       | -                                 | 400     | -                                  | 480     | $\Omega$ |
|  |                 |                         |                    | 6            | -              | 55  | 240       | -                                 | 300     | -                                  | 360     | $\Omega$ |
|  |                 |                         |                    | 9            | -              | 35  | 170       | -                                 | 215     | -                                  | 255     | $\Omega$ |
| Maximum "ON" Resistance Between Any Two Switches | $\Delta R_{ON}$ | $V_{IL}$ or<br>$V_{IH}$ | $V_{CC}$ or<br>GND | 4.5          | -              | 10  | -         | -                                 | -       | -                                  | -       | $\Omega$ |
|  |                 |                         |                    | 6            | -              | 8.5 | -         | -                                 | -       | -                                  | -       | $\Omega$ |
| Switch Off Leakage Current                       | $I_{IZ}$        | En =<br>GND             | $V_{CC}$ or<br>GND | 6            | -              | -   | $\pm 0.1$ | -                                 | $\pm 1$ | -                                  | $\pm 1$ | $\mu A$  |
|  |                 |                         |                    | 10           | -              | -   | $\pm 0.1$ | -                                 | $\pm 1$ | -                                  | $\pm 1$ | $\mu A$  |
| Logic Input Leakage Current                      | $I_I$           | $V_{CC}$ or<br>GND      | -                  | 6            | -              | -   | $\pm 0.1$ | -                                 | $\pm 1$ | -                                  | $\pm 1$ | $\mu A$  |

# CD74HC4016

## DC Electrical Specifications (Continued)

| PARAMETER  | SYMBOL          | TEST CONDITIONS        |                        |                     | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|--|-----------------|------------------------|------------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|  |                 | V <sub>I</sub> (V)     | V <sub>IS</sub> (V)    | V <sub>CC</sub> (V) | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| Quiescent Device Current<br>I <sub>O</sub> = 0mA | I <sub>CC</sub> | V <sub>CC</sub> or GND | V <sub>CC</sub> or GND | 6                   | -    | -   | 2   | -             | 20  | -              | 40  | μA    |
|  |                 |                        |                        | 10                  | -    | -   | 16  | -             | 160 | -              | 320 | μA    |

## Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

| PARAMETER                                       | SYMBOL                              | TEST CONDITIONS       | V <sub>CC</sub> (V)   | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|---|-------------------------------------|-----------------------|-----------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|   |                                     |                       |                       | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| <b>HC TYPES</b>                                 |                                     |                       |                       |      |     |     |               |     |                |     |       |
| Propagation Delay,<br>Switch In to Switch Out   | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                     | -    | -   | 60  | -             | 75  | -              | 90  | ns    |
|   |                                     |                       | 4.5                   | -    | -   | 12  | -             | 15  | -              | 18  | ns    |
|   |                                     | C <sub>L</sub> = 15pF | 5                     | -    | 4   | -   | -             | -   | -              | -   | ns    |
|   |                                     |                       | C <sub>L</sub> = 50pF | 6    | -   | -   | 10            | -   | 13             | -   | 15    |
|   |                                     | 9                     |                       | -    | -   | 8   | -             | 10  | -              | 12  | ns    |
| Propagation Delay,<br>Switch Turn-On En to Out  | t <sub>PZH</sub> , t <sub>PZL</sub> | C <sub>L</sub> = 50pF | 2                     | -    | -   | 190 | -             | 240 | -              | 285 | ns    |
|   |                                     |                       | 4.5                   | -    | -   | 38  | -             | 48  | -              | 57  | ns    |
|   |                                     | C <sub>L</sub> = 15pF | 5                     | -    | 16  | -   | -             | -   | -              | -   | ns    |
|   |                                     |                       | C <sub>L</sub> = 50pF | 6    | -   | -   | 32            | -   | 41             | -   | 48    |
|   |                                     | 9                     |                       | -    | -   | 28  | -             | 35  | -              | 42  | ns    |
| Propagation Delay,<br>Switch Turn-Off En to Out | t <sub>PHZ</sub> , t <sub>PLZ</sub> | C <sub>L</sub> = 50pF | 2                     | -    | -   | 145 | -             | 180 | -              | 220 | ns    |
|   |                                     |                       | 4.5                   | -    | -   | 29  | -             | 36  | -              | 44  | ns    |
|   |                                     | C <sub>L</sub> = 15pF | 5                     | -    | 12  | -   | -             | -   | -              | -   | ns    |
|   |                                     |                       | C <sub>L</sub> = 50pF | 6    | -   | -   | 25            | -   | 31             | -   | 38    |
|   |                                     | 9                     |                       | -    | -   | 22  | -             | 28  | -              | 33  | ns    |
| Input Capacitance                               | C <sub>I</sub>                      | -                     | -                     | -    | 10  | -   | 10            | -   | 10             | pF  |       |
| Power Dissipation Capacitance<br>(Notes 2, 3)   | C <sub>PD</sub>                     | -                     | 5                     | -    | 12  | -   | -             | -   | -              | -   | pF    |

**NOTES:**

- C<sub>PD</sub> is used to determine the dynamic power consumption, per package.
- $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L + C_S) V_{CC}^2 f_o$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $C_S$  = switch capacitance,  $V_{CC}$  = supply voltage.

## Analog Channel Specifications T<sub>A</sub> = 25°C

| PARAMETER   | TEST CONDITIONS                                       | V <sub>CC</sub> (V) | CD74HC4016 | UNITS |
|---|---|---------------------|------------|-------|
| Switch Frequency Response Bandwidth at -3dB<br>Figure 3 | Figure 6, Notes 4, 5                                  | 4.5                 | >200       | MHz   |
| Crosstalk Between Any Two Switches, Figure 4            | Figure 5, Notes 5, 6                                  | 4.5                 | TBE        | dB    |
| Total Harmonic Distortion                               | 1kHz, V <sub>IS</sub> = 4V <sub>P-P</sub><br>Figure 7 | 4, 5                | 0.078      | %     |
|   | 1kHz, V <sub>IS</sub> = 8V <sub>P-P</sub><br>Figure 7 | 9                   | 0.018      | %     |

# CD74HC4016

## Analog Channel Specifications $T_A = 25^\circ\text{C}$ (Continued)

| PARAMETER                                 | TEST CONDITIONS      | $V_{CC}$ (V) | CD74HC4016 | UNITS |
|---|----------------------|--------------|------------|-------|
| Control to Switch Feedthrough Noise       | Figure 8             | 4.5          | TBE        | mV    |
|   |                      | 9            | TBE        | mV    |
| Switch "OFF" Signal Feedthrough, Figure 4 | Figure 9, Notes 5, 6 | 4.5          | -62        | dB    |
| Switch Input Capacitance, $C_S$           |                      | -            | 5          | pF    |

**NOTES:**

4. Adjust input level for 0dBm at output,  $f = 1\text{MHz}$ .
5.  $V_{IS}$  is centered at  $V_{CC}/2$ .
6. Adjust input for 0dBm at  $V_{IS}$ .

## Typical Performance Curves

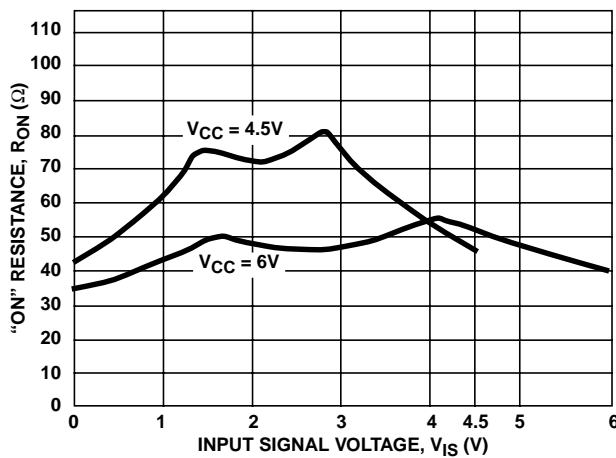


FIGURE 1. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

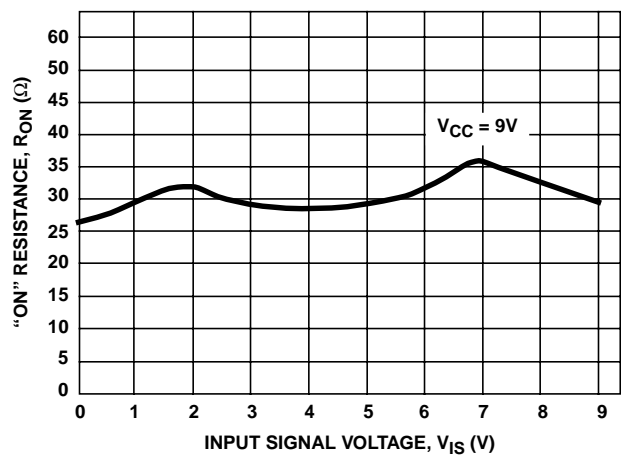


FIGURE 2. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

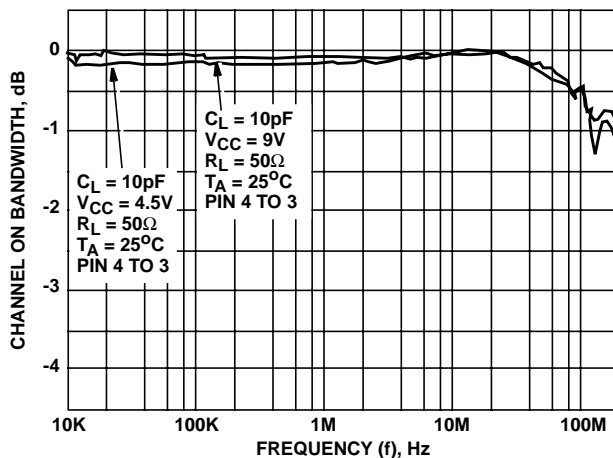


FIGURE 3. SWITCH FREQUENCY RESPONSE

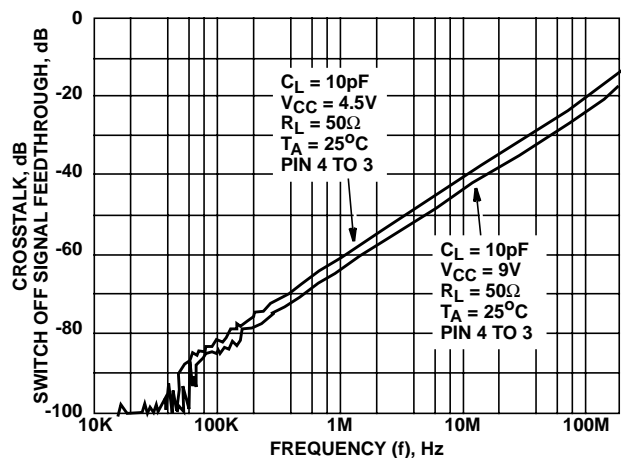


FIGURE 4. SWITCH-OFF SIGNAL FEEDTHROUGH AND CROSSTALK vs FREQUENCY

Analog Test Circuits

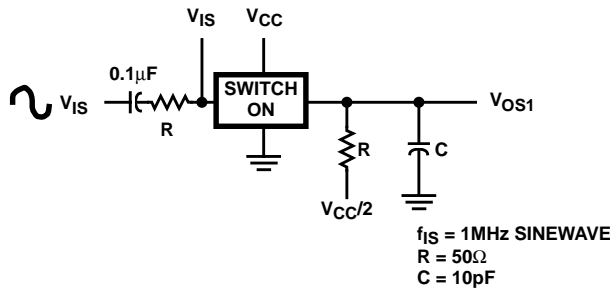


FIGURE 5. CROSSTALK BETWEEN TWO SWITCHES TEST CIRCUIT

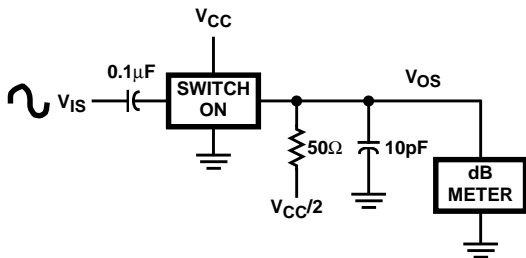
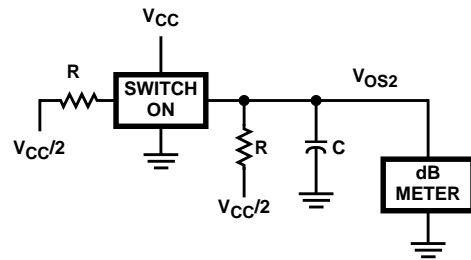


FIGURE 6. FREQUENCY RESPONSE TEST CIRCUIT

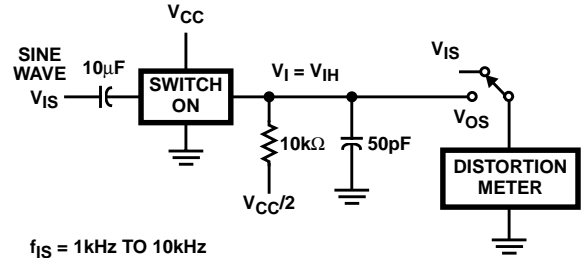


FIGURE 7. TOTAL HARMONIC DISTORTION TEST CIRCUIT

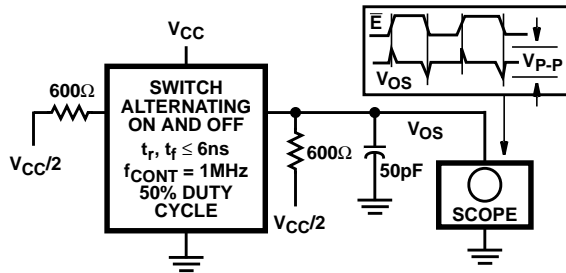


FIGURE 8. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

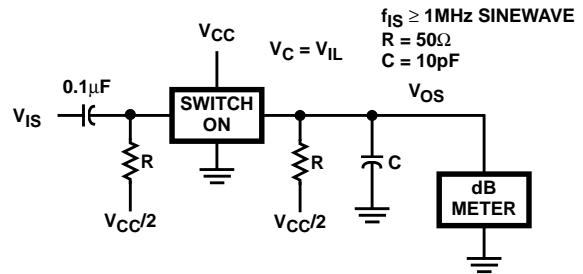


FIGURE 9. SWITCH OFF SIGNAL FEEDTHROUGH TEST CIRCUIT

Test Circuits and Waveforms

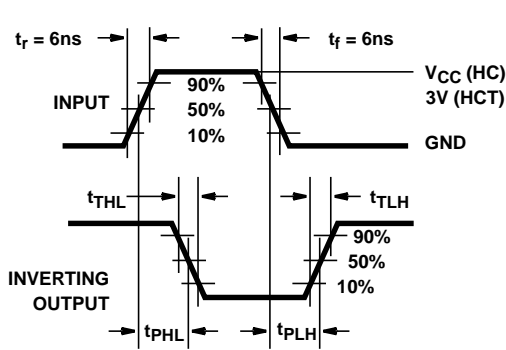


FIGURE 10. HC/HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

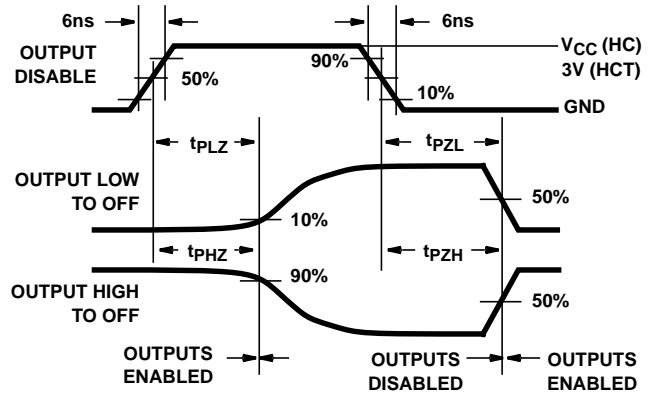


FIGURE 11. SWITCH TURN-ON AND TURN-OFF PROPAGATION DELAY TIMES

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD74HC4016E      | ACTIVE        | PDIP         | N                  | 14   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | -55 to 125   | CD74HC4016E             | <a href="#">Samples</a> |
| CD74HC4016M96    | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC4016M                 | <a href="#">Samples</a> |
| CD74HC4016MT     | ACTIVE        | SOIC         | D                  | 14   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HC4016M                 | <a href="#">Samples</a> |
| CD74HC4016PW     | ACTIVE        | TSSOP        | PW                 | 14   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -55 to 125   | HP14                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC4016M96 | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC4016MT  | SOIC         | D               | 14   | 250  | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC4016M96 | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| CD74HC4016MT  | SOIC         | D               | 14   | 250  | 210.0       | 185.0      | 35.0        |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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