The CDCVF25081 is a high-performance, low-skew, low-jitter, phase-lock loop clock driver. It uses a PLL to precisely align, in both frequency and phase, the output clocks to the input clock signal. The CDCVF25081 operates from a nominal supply voltage of 3.3 V. The device also includes integrated series-damping resistors in the output drivers that make it ideal for driving point-to-point loads.

Two banks of four outputs each provide low-skew, low-jitter copies of CLKin. All outputs operate at the same frequency. Output duty cycles are adjusted to 50%, independent of duty cycle at CLKin. The device automatically goes into power-down mode when no input signal is applied to CLKin and the outputs go into a low state. Unlike many products containing PLLs, the CDCVF25081 does not require an external RC network. The loop filter for the PLL is included on-chip, minimizing component count, space, and cost.

Because it is based on a PLL circuitry, the CDCVF25081 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization is required following power up and application of a fixed-frequency signal at CLKin and any following changes to the PLL reference.

The CDCVF25081 is characterized for operation from -40°C to 85°C.

### FUNCTION TABLE

<table>
<thead>
<tr>
<th>S2</th>
<th>S1</th>
<th>1Y0–1Y3</th>
<th>2Y0–2Y3</th>
<th>OUTPUT SOURCE</th>
<th>PLL SHUTDOWN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Hi-Z</td>
<td>Hi-Z</td>
<td>N/A</td>
<td>Yes</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Active</td>
<td>Hi-Z</td>
<td>PLL†</td>
<td>No</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Active</td>
<td>Active</td>
<td>Input clock (PLL bypass)</td>
<td>Yes</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Active</td>
<td>Active</td>
<td>PLL†</td>
<td>No</td>
</tr>
</tbody>
</table>

† CLK input frequency < 2 MHz switches the outputs to low level

---

**description**

The CDCVF25081 is a high-performance, low-skew, low-jitter, phase-lock loop clock driver. It uses a PLL to precisely align, in both frequency and phase, the output clocks to the input clock signal. The CDCVF25081 operates from a nominal supply voltage of 3.3 V. The device also includes integrated series-damping resistors in the output drivers that make it ideal for driving point-to-point loads.

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Because it is based on a PLL circuitry, the CDCVF25081 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization is required following power up and application of a fixed-frequency signal at CLKin and any following changes to the PLL reference.

The CDCVF25081 is characterized for operation from -40°C to 85°C.
## Terminal Functions

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>PIN NO.</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1Y[0:3]</td>
<td>2, 3, 14, 15</td>
<td>O</td>
<td>Bank 1Yn clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25-Ω series-damping resistor.</td>
</tr>
<tr>
<td>2Y[0:3]</td>
<td>6, 7, 10, 11</td>
<td>O</td>
<td>Bank 2Yn clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25-Ω series-damping resistor.</td>
</tr>
<tr>
<td>CLKIN</td>
<td>1</td>
<td>I</td>
<td>Clock input. CLKIN provides the clock signal to be distributed by the CDCVF25081 clock driver. CLKIN is used to provide the reference signal to the integrated PLL that generates the output signal. CLKIN must have a fixed frequency and phase in order for the PLL to acquire lock. Once the circuit is powered up and a valid signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to CLKIN.</td>
</tr>
<tr>
<td>FBIN</td>
<td>16</td>
<td>I</td>
<td>Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be wired to one of the outputs to complete the feedback loop of the internal PLL. The integrated PLL synchronizes the FBIN and output signal so there is nominally zero-delay from input clock to output clock.</td>
</tr>
<tr>
<td>GND</td>
<td>5, 12</td>
<td>Ground</td>
<td>Ground</td>
</tr>
<tr>
<td>S1, S2</td>
<td>9, 8</td>
<td>I</td>
<td>Select pins to determine mode of operation. See the FUNCTION TABLE for mode selection options.</td>
</tr>
<tr>
<td>VDD</td>
<td>4, 13</td>
<td>Power</td>
<td>Supply voltage. The supply voltage range is 3 V to 3.6 V</td>
</tr>
</tbody>
</table>
functional block diagram
absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

 Supply voltage range, \( V_{DD} \) .......................... \(-0.5 \) V to \( 4.6 \) V
 Input voltage range, \( V_I \) (see Notes 1 and 2) .......................... \(-0.5 \) V to \( 4.6 \) V
 Output voltage range, \( V_O \) (see Notes 1 and 2) .......................... \(-0.5 \) V to \( V_{DD} + 0.5 \) V
 Input clamp current, \( I_{IK} (V_I < 0) \) .......................... \(-50 \) mA
 Output clamp current, \( I_{OK} (V_O < 0) \) .......................... \(-50 \) mA
 Continuous total output current, \( I_O (V_O = 0 \) to \( V_{DD} \) .......................... \(-50 \) mA
 Package thermal impedance, \( \theta_{JA} \) (see Note 3): PW package .......................... \( 147^\circ \)C/W
 D package .......................... \( 112^\circ \)C/W
 Storage temperature range, \( T_{stg} \) .......................... \(-65^\circ \)C to \( 150^\circ \)C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to \( 4.6 \) V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, ( V_{DD} )</td>
<td>3</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Low level input voltage, ( V_{IL} )</td>
<td></td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>High level input voltage, ( V_{IH} )</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input voltage, ( V_I )</td>
<td>0</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>High-level output current, ( I_{OH} )</td>
<td></td>
<td>(-12)</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Low-level output current, ( I_{OL} )</td>
<td></td>
<td>12</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Operating free-air temperature, ( T_A )</td>
<td>(-40)</td>
<td>85</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

timing requirements over recommended ranges of supply voltage, load and operating free-air temperature

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock frequency, ( f_{\text{clk}} )</td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( C_L = 25 ) pF</td>
<td>8</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_L = 15 ) pF</td>
<td>66</td>
<td>200</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Electrical Characteristics

**Input Voltage**
- \( V_{IK} \): Input voltage
- \( V_{DD} = 3 \text{ V} \), \( I_I = -18 \text{ mA} \)

**Input Current**
- \( I_I \): Input current
- \( V_I = 0 \text{ V or } V_{DD} \), \( \pm 5 \mu A \)

**Power Down Current**
- \( I_{PD} \): Power down current
- \( f_{CLKIN} = 0 \text{ MHz} \), \( V_{DD} = 3.3 \text{ V} \), \( 20 \mu A \)

**Output 3-state Current**
- \( I_{OZ} \): Output 3-state current
- \( V_O = 0 \text{ V or } V_{DD} \), \( V_{DD} = 3.6 \text{ V} \), \( \pm 5 \mu A \)

**Input Capacitance**
- \( C_I \): Input capacitance at \( FBIN, CLKIN \)
- \( V_I = 0 \text{ V or } V_{DD} \), \( 4 \text{ pF} \)
- \( C_I \): Input capacitance at \( S1, S2 \)
- \( V_I = 0 \text{ V or } V_{DD} \), \( 2.2 \text{ pF} \)

**Output Capacitance**
- \( C_O \): Output capacitance
- \( V_I = 0 \text{ V or } V_{DD} \), \( 3 \text{ pF} \)

**High-level Output Voltage**
- \( V_{OH} \): High-level output voltage
- \( V_{DD} = \text{min to max}, I_{OH} = -100 \mu A \), \( V_{DD} = 0.2 \text{ V} \)
  - \( V_{DD} = 3 \text{ V}, I_{OH} = -12 \text{ mA} \), \( 2.1 \text{ V} \)
  - \( V_{DD} = 3 \text{ V}, I_{OH} = -6 \text{ mA} \), \( 2.4 \text{ V} \)

**Low-level Output Voltage**
- \( V_{OL} \): Low-level output voltage
- \( V_{DD} = \text{min to max}, I_{OL} = 100 \mu A \), \( 0.2 \text{ V} \)
  - \( V_{DD} = 3 \text{ V}, I_{OL} = 12 \text{ mA} \), \( 0.8 \text{ V} \)
  - \( V_{DD} = 3 \text{ V}, I_{OL} = 6 \text{ mA} \), \( 0.55 \text{ V} \)

**High-level Output Current**
- \( I_{OH} \): High-level output current
- \( V_{DD} = 3 \text{ V}, V_O = 1 \text{ V} \), \( -24 \text{ mA} \)
  - \( V_{DD} = 3.3 \text{ V}, V_O = 1.65 \text{ V} \), \( -30 \text{ mA} \)
  - \( V_{DD} = 3.6 \text{ V}, V_O = 3.135 \text{ V} \), \( -15 \text{ mA} \)

**Low-level Output Current**
- \( I_{OL} \): Low-level output current
- \( V_{DD} = 3 \text{ V}, V_O = 1.95 \text{ V} \), \( 26 \text{ mA} \)
  - \( V_{DD} = 3.3 \text{ V}, V_O = 1.65 \text{ V} \), \( 33 \text{ mA} \)
  - \( V_{DD} = 3.6 \text{ V}, V_O = 0.4 \text{ V} \), \( 14 \text{ mA} \)

† All typical values are at respective nominal \( V_{DD} \).
‡ For \( I_{DD} \) over frequency see Figure 7.
switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP†</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{lock}$</td>
<td>PLL lock time</td>
<td>$f = 100$ MHz</td>
<td>10</td>
<td>6</td>
<td>μs</td>
</tr>
<tr>
<td>$t_{phase}$</td>
<td>Phase offset (CLKIN to FBIN)</td>
<td>$f = 8$ MHz to 66 MHz, $V_{th} = V_{DD}/2$ (see Note 5)</td>
<td>–200</td>
<td>200</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 66$ MHz to 200 MHz, $V_{th} = V_{DD}/2$ (see Note 5)</td>
<td>–150</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>Low-to-high level output propagation delay</td>
<td>$S_2 = \text{Hi}$, $S_1 = \text{Low}$ (PLL bypass)</td>
<td>2.5</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>High-to-low level output propagation delay</td>
<td>$f = 1$ MHz, $C_L = 25$ pF</td>
<td>150</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{sk(o)}$</td>
<td>Output skew (Yn to Yn) (see Note 4)</td>
<td></td>
<td>150</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{sk(pp)}$</td>
<td>Part-to-part skew</td>
<td>$S_2 = \text{high}$, $S_1 = \text{high (PLL mode)}$</td>
<td>600</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$S_2 = \text{high}$, $S_1 = \text{low}$ (PLL bypass)</td>
<td>700</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{jit(cc)}$</td>
<td>Jitter (cycle-to-cycle)</td>
<td>$f = 66$ MHz to 200 MHz, $C_L = 15$ pF</td>
<td>±100</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 66$ MHz to 100 MHz, $C_L = 25$ pF</td>
<td>±150</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{drc}$</td>
<td>Output duty cycle</td>
<td>$f = 8$ MHz to 200 MHz</td>
<td>43%</td>
<td>57%</td>
<td></td>
</tr>
<tr>
<td>$t_{sk(p)}$</td>
<td>Pulse skew</td>
<td>$S_2 = \text{High}$, $S_1 = \text{low}$ (PLL bypass)</td>
<td>0.7</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Rise time rate</td>
<td>$C_L = 15$ pF, See Figure 4</td>
<td>0.8</td>
<td>3.3</td>
<td>V/ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = 25$ pF, See Figure 4</td>
<td>0.5</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>$t_f$</td>
<td>Fall time rate</td>
<td>$C_L = 15$ pF, See Figure 4</td>
<td>0.8</td>
<td>3.3</td>
<td>V/ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_L = 25$ pF, See Figure 4</td>
<td>0.5</td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

† All typical values are at respective nominal $V_{DD}$.

NOTES:
4. The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
5. Similar waveform at CLKIN and FBIN are required. For phase displacement between CLKIN and Y-outputs see Figure 5.
PARAMETER MEASUREMENT INFORMATION

From Output Under Test

\[ C_L = 25 \text{ pF at } f = 8 \text{ MHz to } 100 \text{ MHz} \]
\[ C_L = 15 \text{ pF at } f = 66 \text{ MHz to } 200 \text{ MHz} \]

NOTES:
A. \( C_L \) includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics:
   \( Z_O = 50 \Omega, t_r < 1.2 \text{ ns}, t_f < 1.2 \text{ ns} \).
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Test Load Circuit

Figure 2. Voltage Thresholds for Measurements, Phase Offset (PLL Mode)

Figure 3. Output Skew and Output Duty Cycle (PLL Mode)

NOTE: \( odc = \frac{t_1}{(t_1 + t_2)} \times 100\% \)
PARAMETER MEASUREMENT INFORMATION

NOTE: \( t_{sk(p)} = |t_{PLH} - t_{PHL}| \)

Figure 4. Propagation Delay and Pulse Skew (Non-PLL Mode)

Figure 5

Figure 6
PARAMETER MEASUREMENT INFORMATION

SUPPLY CURRENT
vs
FREQUENCY

Figure 7

$V_{DD} = 3 \text{ V to } 3.6 \text{ V}$
$C_L(Y_{in}) = 15 \text{ pF} \parallel 500 \text{ } \Omega$
$T_A = -40 \degree \text{ C to } 85 \degree \text{ C}$

$V_{DD} = 3.6 \text{ V}$
$T_A = 85 \degree \text{ C}$

$V_{DD} = 3 \text{ V}$
$T_A = -40 \degree \text{ C}$

$V_{DD} = 3 \text{ V}$
$T_A = 85 \degree \text{ C}$
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Top-Side Markings</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDCVF25081D</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>CKV25081</td>
<td><a href="#">Samples</a></td>
</tr>
<tr>
<td>CDCVF25081DG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>CKV25081</td>
<td><a href="#">Samples</a></td>
</tr>
<tr>
<td>CDCVF25081DR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>CKV25081</td>
<td><a href="#">Samples</a></td>
</tr>
<tr>
<td>CDCVF25081DRG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>CKV25081</td>
<td><a href="#">Samples</a></td>
</tr>
<tr>
<td>CDCVF25081PW</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>90</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>CK081</td>
<td><a href="#">Samples</a></td>
</tr>
<tr>
<td>CDCVF25081PWG4</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>90</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>CK081</td>
<td><a href="#">Samples</a></td>
</tr>
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<td>CU NIPDAU</td>
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<td>-40 to 85</td>
<td>CK081</td>
<td><a href="#">Samples</a></td>
</tr>
<tr>
<td>CDCVF25081PWRG4</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>CK081</td>
<td><a href="#">Samples</a></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. – The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W  (mm)</th>
<th>Pin1 Quadrant</th>
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<tr>
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<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>10.3</td>
<td>2.1</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
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<tr>
<td>CDCVF25081PWR</td>
<td>TSSOP</td>
<td>PW</td>
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<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.

A0: Dimension designed to accommodate the component width
B0: Dimension designed to accommodate the component length
K0: Dimension designed to accommodate the component thickness
W: Overall width of the carrier tape
P1: Pitch between successive cavity centers

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### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
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<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
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<th>SPQ</th>
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<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AC.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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