CLC501

CLC501 High Speed, Output Clamping Op Amp

Literature Number: SNOS858C
High Speed, Output Clamping Op Amp

General Description
The CLC501 is a high speed current-feedback op amp with the unique feature of output voltage clamping. This feature allows both the maximum positive ($V_{\text{HIGH}}$) and negative ($V_{\text{LOW}}$) output voltage levels to be established. This is useful in a number of applications in which “downstream” circuitry must be protected from over driving input signals. Not only can this prevent damage to downstream circuitry, but can also reduce time delays since saturation is avoided. The CLC501’s very fast 1ns overload/clamping recovery time is useful in applications in which information containing signals follow overdriving signals.

Engineers designing high resolution, subranging A/D systems have long sought an amplifier capable of meeting the demanding requirements of the residue amplifier function. Amplifiers providing the residue function must not only settle quickly, but recover from overdrive quickly, protect the second stage A/D, and provide high fidelity at relatively high gain settings. The CLC501, which excels in these areas, is the ideal design solution in this onerous application. To further support this application, the CLC501 is both characterized and tested at a gain setting of +32—the most common gain setting for residue amplifier applications.

The CLC501’s other features provide a quick, high performance design solution. Since the CLC501’s current feedback design requires no external compensation, designers need not spend their time designing compensation networks. The small 8-pin package and low, 180mW power consumption make the CLC501 ideal in numerous applications having small power and size budgets.

The CLC501 is available in several versions to meet a variety of requirements. A three letter suffix determines the version:
- Enhanced Solutions (Military/Aerospace)
- SMD Number: 5962-94597
- *Space level version also available.
- *For more information, visit http://www.national.com/mil

Features
- Output clamping ($V_{\text{HIGH}}$ and $V_{\text{LOW}}$)
- 1ns recovery from clamping/overdrive
- 0.05% settling in 12ns
- Characterized and guaranteed at $A_{v} = +32$
- Low power: 180mW

Applications
- Residue amplifier in high accuracy, subranging A/D systems
- High speed communications
- Output clamping applications
- Pulse amplitude modulation systems

Connection Diagrams

Features

Applications
## Ordering Information

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<tr>
<th>Package</th>
<th>Temperature Range</th>
<th>Part Number</th>
<th>Package Marking</th>
<th>NSC Drawing</th>
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<td>CLC501AJP</td>
<td>CLC501AJP</td>
<td>N08E</td>
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<td>CLC501AJE</td>
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### Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Supply Voltage ($V_{CC}$): ±7V
- $I_{OUT}$: Output is short circuit protected to ground, but maximum reliability will be maintained if $I_{OUT}$ does not exceed... 60mA
- Common Mode Input Voltage: ±$V_{CC}$
- Junction Temperature: +150°C
- Operating Temperature Range: −40°C to +85°C

Storage Temperature Range: −65°C to +150°C
Lead Solder Duration (+300°C): 10 sec
ESD Rating (Human Body Model): <1000V
Recommended Gain Range: +7 to +50, −1 to −50

### Operating Ratings

<table>
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<tr>
<th>Package</th>
<th>Thermal Resistance ($\theta_{JC}$)</th>
<th>($\theta_{JA}$)</th>
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<td>MDIP</td>
<td>70°C/W</td>
<td>125°C/W</td>
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<td>SOIC</td>
<td>65°C/W</td>
<td>145°C/W</td>
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### Electrical Characteristics

($A_V = +32, V_{CC} = \pm 5$ V, $R_L = 100\Omega, R_f = 1.5\Omega$, $V_H = +3$V; unless specified)

<table>
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<th>Parameters</th>
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<th>Typ</th>
<th>Max &amp; Min Ratings</th>
<th>Units</th>
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<td>Ambient Temperature</td>
<td>CLC501AJ</td>
<td>+25°C</td>
<td>−40°C to +85°C</td>
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#### Frequency Domain Response
- SSBW: −3dB Bandwidth ($V_{OUT} < 5V_{PP}$): 75 > 60 > 60 > 45 MHz
- SS20: −3dB Bandwidth ($@ A_V = +20, V_{OUT} < 2V_{PP}$): 110 > 85 > 85 > 55 MHz

#### Gain Flatness
- GFPL: Peaking ($<15$MHz): 0 < 0.1 < 0.1 < 0.1 dB
- GFPH: Peaking ($>15$MHz): 0 < 0.2 < 0.2 < 0.2 dB
- GFR: Rolloff ($<30$MHz): 0.2 < 1.0 < 1.0 < 1.3 dB
- LPD: Linear Phase Deviation: DC to 30MHz 0.2 < 1.0 < 1.0 < 1.0 deg

#### Time Domain Response
- TRS: Rise and Fall Time ($2V$ Step): 4.7 < 5.8 < 5.8 < 7.8 ns
- TRL: 5V Step: 5.5 < 6.5 < 6.5 < 8.0 ns
- TSP: Settling Time to ±0.05% ($2V$ Step): 12 < 18 < 18 < 24 ns
- OS: Overshoot ($2V$ Step): 0 < 5 < 5 < 5 %
- SR: Slew Rate: 1200 > 800 > 800 > 700 V/µs

#### Distortion And Noise Response
- HD2: 2nd Harmonic Distortion ($2V_{PP}, 20$MHz): −45 < −30 < −33 < −30 dBc
- HD3: 3rd Harmonic Distortion ($2V_{PP}, 20$MHz): −60 < −45 < −50 < −50 dBc
- SNF: Noise Floor ($>1$MHz): −158 < −156 < −156 < −155 dBM (1Hz)
- INV: Integrated Noise ($1$MHz to 100MHz): 28 < 35 < 35 < 40 µV

#### Clamp Performance
- OVC: Overshoot in Clamp (32× Overdrive): 5 < 15 < 15 %
- TSO: Overload Recovery from Clamp (32× Overdrive): 1 < 3 < 3 < 3 ns
- CDR: $V_{op}$ Drift after Recovery: 150 < 200 < 200 < 200 µV
- VOC: Clamp Accuracy (Note 3) (2× Overdrive): 0.1 < 0.2 < 0.2 < 0.2 V
- ICL: Input Bias Current on $V_H$, $V_L$: 20 < 100 < 50 < 50 µA
- CBW: −3dB Bandwidth ($V_L, V_H = 2V_{PP}$): 50 < 3.0 < 3.3 < 3.3 MHz
- CMC: Useful Clamping Range ($V_H$ or $V_L$): < 3.0 < 3.3 < 3.3 V

#### Static, DC Performance
- VIO: Input Offset Voltage (Note 3): 1.5 < 4.6 < 3.0 < 5.0 mV
- DVO: Average Temperature Coefficient: 10 < 20 – < 20 µV/°C
- IBN: Input Bias Current (Note 3) (Non-Inverting): 10 < 37 < 25 < 35 µA
Symbol | Parameters | Condition | Typ | Max & Min Ratings(Note 2) | Units
--- | --- | --- | --- | --- | ---
DIBN | Average Temperature Coefficient | | 100 | <150 | – | <100 nA/°C
IBI | Input Bias Current(Note 3) | Inverting | 10 | <46 | <30 | <40 µA
DIBI | Average Temperature Coefficient | | 100 | <200 | – | <100 nA/°C
PSRR | Power Supply Rejection Ratio | | 70 | >55 | >60 | >60 dB
CMRR | Common Mode Rejection Ratio | | 70 | >55 | >60 | >60 dB
ICC | Supply Current(Note 3) | No Load | 18 | <25 | <24 | <24 mA

### Miscellaneous Performance

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<th>Units</th>
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<td>&gt;0.3</td>
<td>Ω</td>
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<td>&gt;2.5 V</td>
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<td>VO</td>
<td>Output Voltage Range</td>
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<td>±60</td>
<td>&gt;±35</td>
<td>&gt;±50</td>
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<tr>
<td>IO</td>
<td>Output Current</td>
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<td>±60</td>
<td>&gt;±35</td>
<td>&gt;±50</td>
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**Note 1:** “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

**Note 2:** Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

**Note 3:** AJ 100% tested at +25°C, sample at +85°C

### Typical Performance Characteristics

(T<sub>A</sub> = 25°C, A<sub>V</sub> = +32, V<sub>CC</sub> = ±5V, R<sub>L</sub> = 100Ω, R<sub>f</sub> = 1.5Ω, V<sub>H</sub> = +3V, V<sub>L</sub> = −3V)

**Non-Inverting Frequency Response**

**Inverting Frequency Response**

![Non-Inverting Frequency Response](image1)

![Inverting Frequency Response](image2)
Frequency Response for $R_L S$

Open-Loop Transimpedance Gain, $Z(s)$

2nd and 3rd Harmonic Distortion

2-Tone, 3rd Order, Intermodulation Intercept

Equivalent Input Noise

CMRR and PSRR
Clamped Pulse Response

Settling, Clamped (32x overdrive)

Long-Term Settling, Clamped (32x overdrive)

Nonlinearity Near Clamp Voltage

Settling, Unclamped

Long-Term Settling, Unclamped
Settling Time vs. Capacitive Load

Application Division

FIGURE 1. Recommended non-Inverting gain circuit

FIGURE 2. Recommended Inverting gain circuit

FIGURE 3. Recommended clamp biasing for clamp levels of +1V and -2V
Clamp Operation

The maximum positive or negative excursion of the output voltage is determined by voltage applied to the clamping pins, \(V_H\) and \(V_L\). \(V_H\) determines the positive clamping level; \(V_L\) determines the negative level. For example, if \(V_H\) is at +2V and \(V_L\) is set at −0.5V the output voltage is restricted within this −0.5V to +2V range. When the output voltage tries to exceed this level, the amplifier goes into “clamp mode” and the output voltage limits at the clamp voltage.

Clamp Accuracy and Amplifier Linearity

Ideally, the clamped output voltage and the clamp voltage should be identical. In practice, however, there are two sources of clamp inaccuracy: the inherent clamp accuracy (which is shown in the specification page) and resistor divider action of open-loop output resistance of 10Ω and the load resistor. Or, in equation form,

\[
V_{OUT, \ \text{CLAMP}} = (V_H \text{ or } L \pm 200 \text{ mV}) \frac{R_L}{R_L = 10 \Omega} \quad (1)
\]

When setting the clamp voltage, the designer should also recognize that within about 200mV of the clamp voltage, amplifier linearity begins to deteriorate. (See plot on the previous page.)

Biasing \(V_H\) and \(V_L\)

Each of the clamping pins is buffered internally so simple resistive voltage divider circuits work well in providing the clamp voltage (see Figure 3). The 100Ω isolating resistor ensures stability when the clamp pin is connected to \(V_{CC}\) or when the clamp pins is driven by an external signal source; in other situations, such as the one described in Figure 3, the isolating resistor is not necessary.

\(V_H\) should be biased more positively than \(V_L\). \(V_H\) may be biased below 0V; however, with this biasing, the output voltage will actually clamp at 0V unless a simple pull down circuit is added to the op amp output. (When clamped against \(V_H\), the output cannot sink current.) An analogous situation and design solution exists for \(V_L\) when it is biased above 0V, but in this case, a pull up circuit is used to source current when the amplifier is clamped against \(V_L\).

The clamps, which have a bandwidth of about 50MHz, may be driven by high frequency signal source. This allows the clamping level to be modulated, which is useful in many applications such as pulse amplitude modulation. The source resistance of the signal source should be less than 500Ω to ensure stability.

Clamp-Mode Dynamics

As can be seen in the clamped pulse response plot on the previous page, clamping is virtually instantaneous. Note, however, that there can be a small amount of overshoot, as indicated on the specification page. The output voltage stays at the clamp voltage level as long as the product of the input voltage and the gain setting exceeds the clamp voltage. When the input voltage decreases, it will eventually reach a point where it is no longer trying to drive the output voltage above the clamp voltage, when this occurs, there is typically a 1ns “overload recovery from clamp,” which is the time it takes for the op amp to resume linear operation. The normal op amp parameters, such as the rise time, apply when the op amp is in linear operation.

When the op amp is in clamp mode for more than about 100ns, a small thermal tail can be detected in the settling performance. This tail, which has a maximum value of 200µV referred to the input, is proportional to the amount of time spent in clamp in clamp mode. In most applications, this will have only a minor effect. For example, in a system with a 100ns overdrive occurring with a duty cycle of 10%, the input-referred tail is 20µV which is only 0.001% of a 2V signal.

DC Accuracy and Noise

Since the two inputs for the CLC501 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. Specifically, the inverting input current noise is much larger than the non-inverting current noise. Also the two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting pin resistors ineffective.

In equation 3, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaced the algebraic sum. \(R_{eq}\) is the non-inverting pin resistance.

\[
\text{PSRR and CMRR:} \quad PSRR: \quad \frac{\Delta V_{\text{IN}}}{\Delta V_{\text{CC}}} = 180 \mu V/V \quad \text{CMRR:} \quad \frac{\Delta I_{\text{IN}}}{\Delta V_{\text{CC}}} = 3 \mu A/V
\]

The total effect, as reference to the input, is given by the following:

\[
\begin{align*}
\text{PSRR:} & = -20 \log \left( \frac{\Delta V_{\text{IN}}}{\Delta V_{\text{CC}}} + \frac{\Delta I_{\text{IN}}}{\Delta V_{\text{CC}}} \frac{R_{eq}}{R_{eq}} + \frac{\Delta I_{\text{IN}}}{\Delta V_{\text{CC}}} \frac{R_{eq}}{R_{eq}} \right) \\
\text{CMRR:} & = -20 \log \left( \frac{\Delta V_{\text{IN}}}{\Delta V_{\text{CC}}} + \frac{\Delta I_{\text{IN}}}{\Delta V_{\text{CC}}} \frac{R_{eq}}{R_{eq}} + \frac{\Delta I_{\text{IN}}}{\Delta V_{\text{CC}}} \frac{R_{eq}}{R_{eq}} \right)
\end{align*}
\]

Where \(R_{eq}\) is the equivalent resistance seen by the non-inverting input and \(R_{eq}\) is the equivalent resistance of \(R_{eq}\) in parallel with \(R_{eq}\).

Printed circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Evaluation PC boards (part number CLC730013 for through-hole and CLC730027 for SOIC) for the CLC501 are available.
CLC501 High Speed, Output Clamping Op Amp

Notes

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