

# DualCool™ N-Channel NexFET™ Power MOSFETs

 Check for Samples: [CSD16325Q5C](#)

## FEATURES

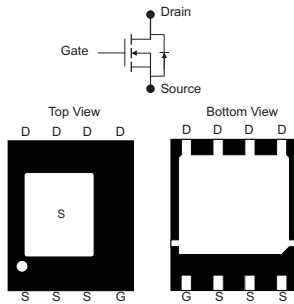
- DualCool™ Package SON 5x6mm
- Optimized for 2-Sided Cooling
- Optimized for 5V Gate Drive
- Ultralow  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant and Halogen Free

## APPLICATIONS

- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

## DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications and optimized for 5V gate drive applications.



## PRODUCT SUMMARY

$V_{DS}$	Drain to Source Voltage	25	V
$Q_g$	Gate Charge Total (4.5V)	18	nC
$Q_{gd}$	Gate Charge Gate to Drain	3.5	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	2.1 mΩ
		$V_{GS} = 4.5V$	1.7 mΩ
		$V_{GS} = 8V$	1.5 mΩ
$V_{GS(th)}$	Threshold Voltage	1.1	V

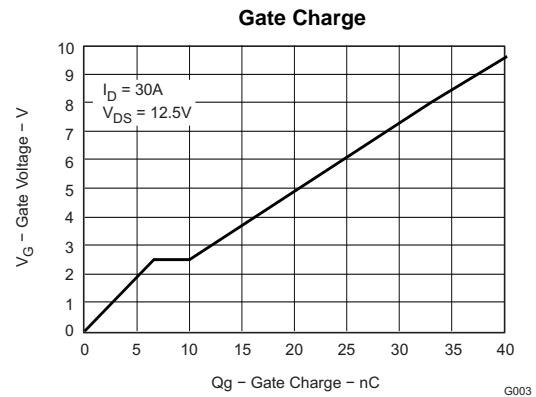
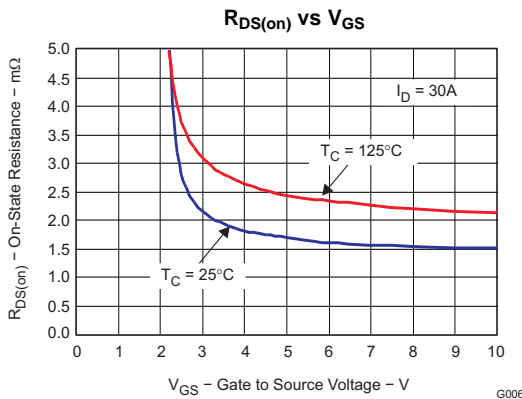
## ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16325Q5C	SON 5x6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage	+10 / -8	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current <sup>(1)</sup>	33	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	200	A
$P_D$	Power Dissipation <sup>(1)</sup>	3.1	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 100\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	500	mJ

- (1) Typical  $R_{\theta JA} = 38^\circ\text{C/W}$  on 1-in<sup>2</sup> Cu, (2-oz.) on a 0.060" thick FR4 PCB.  
 (2) Pulse duration  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25			V
$I_{DSS}$	Drain to Source Leakage	$V_{GS} = 0V, V_{DS} = 20V$			1	$\mu A$
$I_{GSS}$	Gate to Source Leakage	$V_{DS} = 0V, V_{GS} = +10/-8V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V, I_D = 30A$		2.1	2.9	m $\Omega$
		$V_{GS} = 4.5V, I_D = 30A$		1.7	2.2	m $\Omega$
		$V_{GS} = 8V, I_D = 30A$		1.5	2	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 15V, I_D = 30A$		159		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 12.5V,$ $f = 1MHz$		3070	4000	pF
$C_{oss}$	Output Capacitance			2190	2850	pF
$C_{rss}$	Reverse Transfer Capacitance			120	150	pF
$R_G$	Series Gate Resistance			1.6	3.2	$\Omega$
$Q_g$	Gate Charge Total (4.5V)	$V_{DS} = 12.5V,$ $I_{DS} = 30A$		18	25	nC
$Q_{gd}$	Gate Charge – Gate to Drain			3.5		nC
$Q_{gs}$	Gate Charge – Gate to Source			6.6		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			3.1		nC
$Q_{oss}$	Output Charge	$V_{DS} = 13V, V_{GS} = 0V$		43		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 12.5V, V_{GS} = 4.5V,$ $I_{DS} = 30A, R_G = 2\Omega$		10.5		ns
$t_r$	Rise Time			16		ns
$t_{d(off)}$	Turn Off Delay Time			32		ns
$t_f$	Fall Time			12		ns
<b>Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_{DS} = 30A, V_{GS} = 0V$		0.8	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 13V, I_F = 30A, di/dt = 300A/\mu s$		63		nC
$t_{rr}$	Reverse Recovery Time			47		ns

## THERMAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

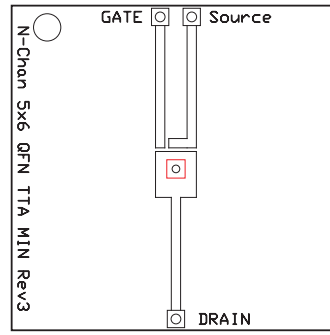
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case (Top Source) <sup>(1)</sup>			1.4	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction to Case (Bottom drain) <sup>(1)</sup>			1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)(2)</sup>			50	$^\circ\text{C/W}$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> 2-oz. Cu pad on a 1.5 × 1.5-inch 0.060-inch thick FR4 board.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta CA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch<sup>2</sup> of 2-oz. Cu.



Max  $R_{\theta JA} = 50^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> of 2-oz. Cu.

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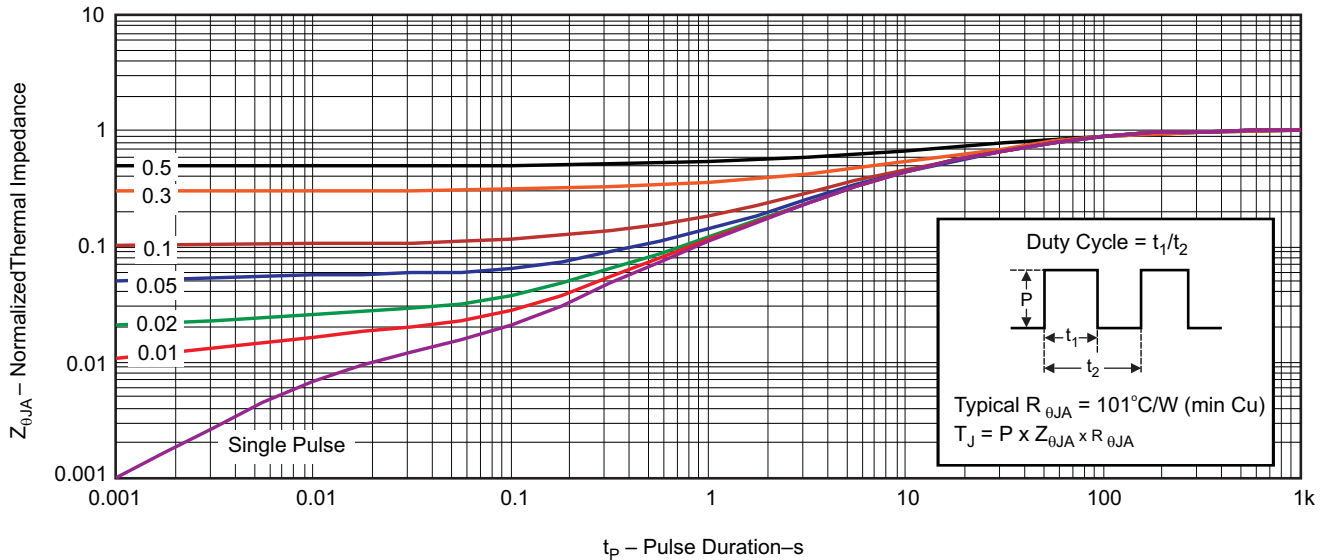


Max  $R_{\theta JA} = 126^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of  
2-oz. Cu.

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### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

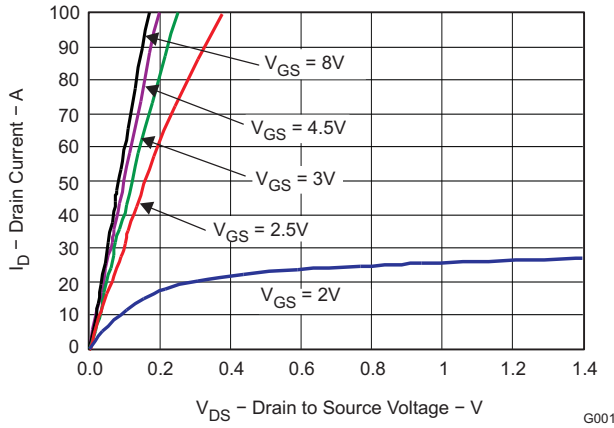


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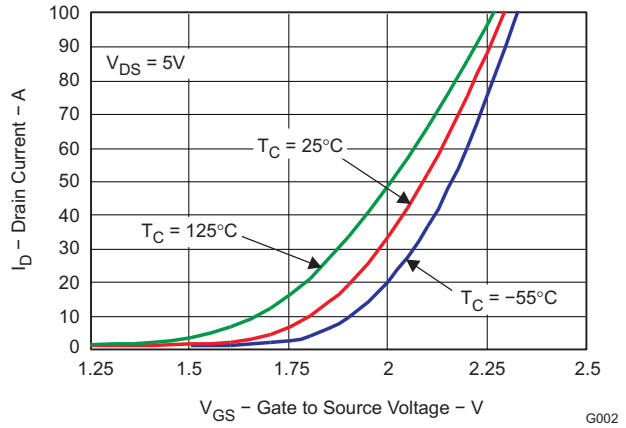
Figure 1. Transient Thermal Impedance

**TYPICAL MOSFET CHARACTERISTICS (continued)**

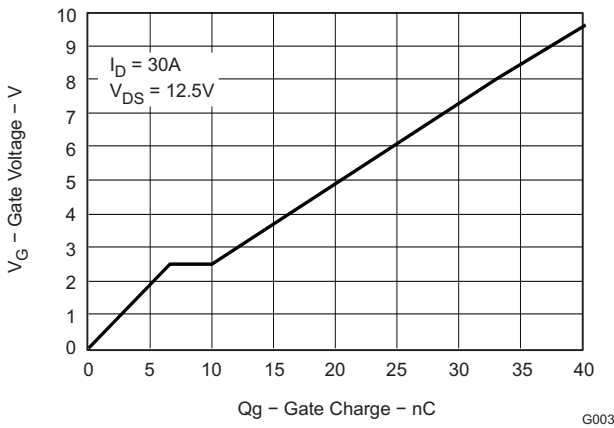
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



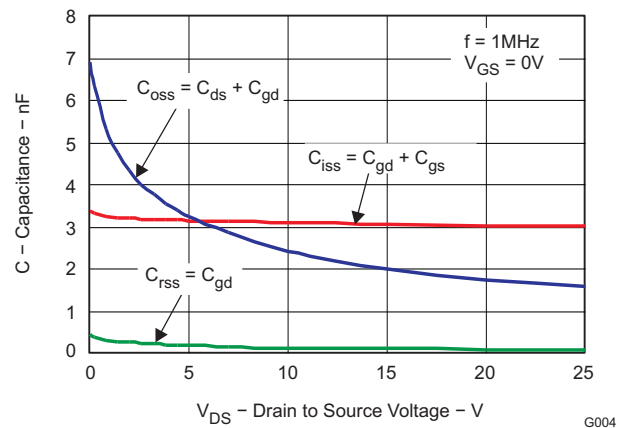
**Figure 2. Saturation Characteristics**



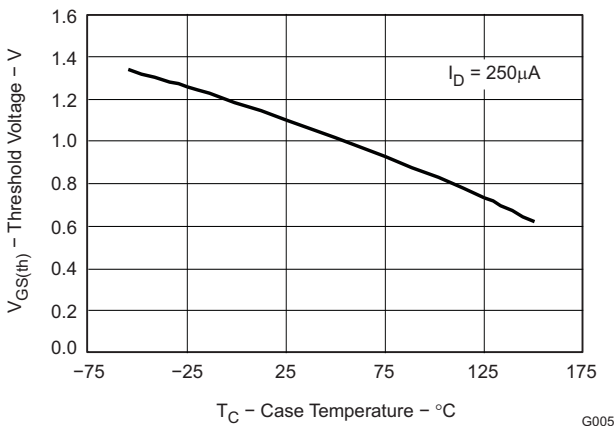
**Figure 3. Transfer Characteristics**



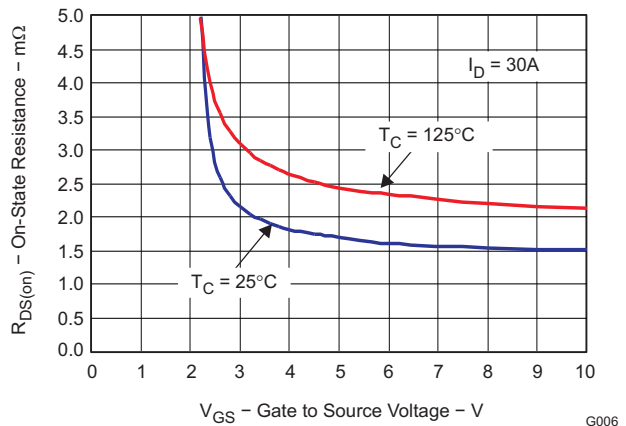
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On Resistance vs. Gate Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

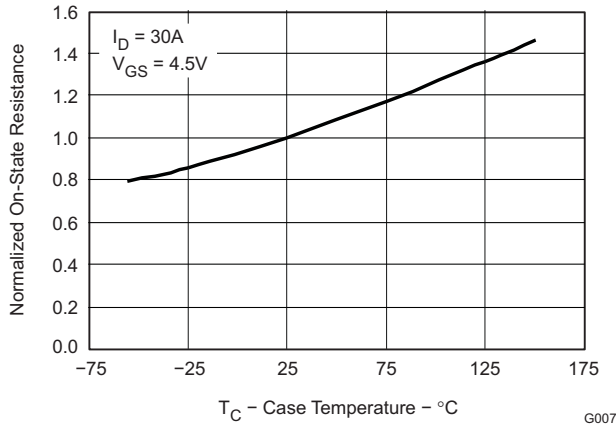


Figure 8. On Resistance vs. Temperature

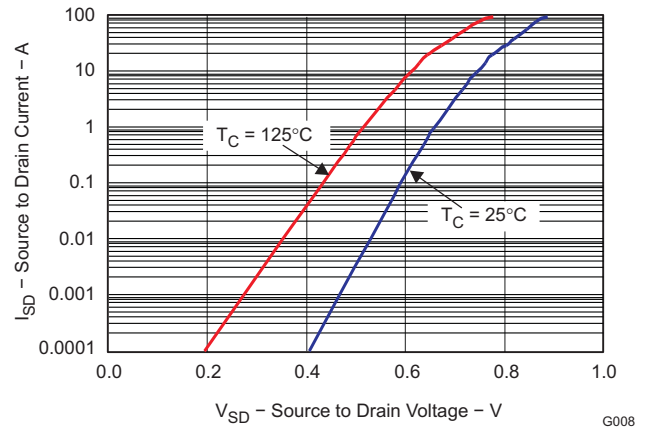


Figure 9. Typical Diode Forward Voltage

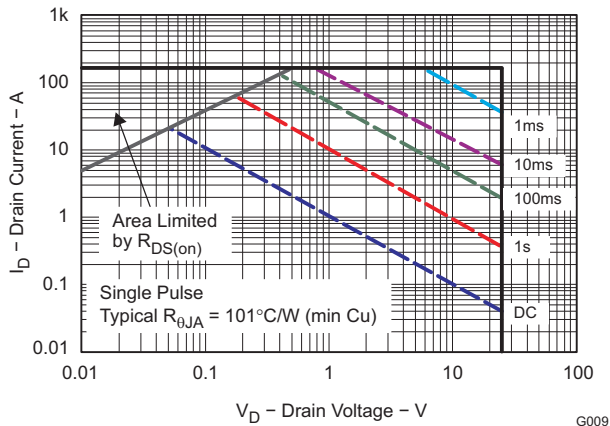


Figure 10. Maximum Safe Operating Area

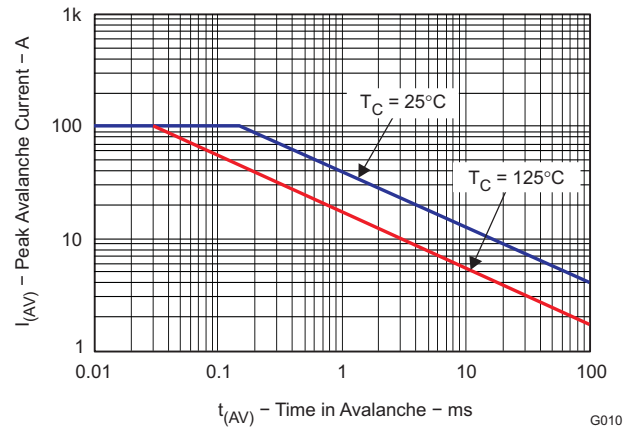


Figure 11. Single Pulse Unclamped Inductive Switching

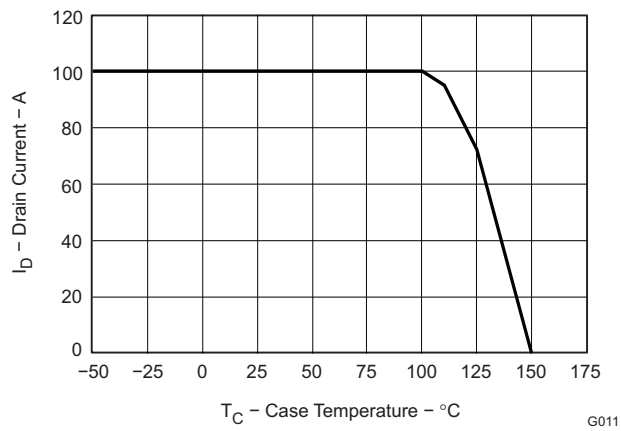
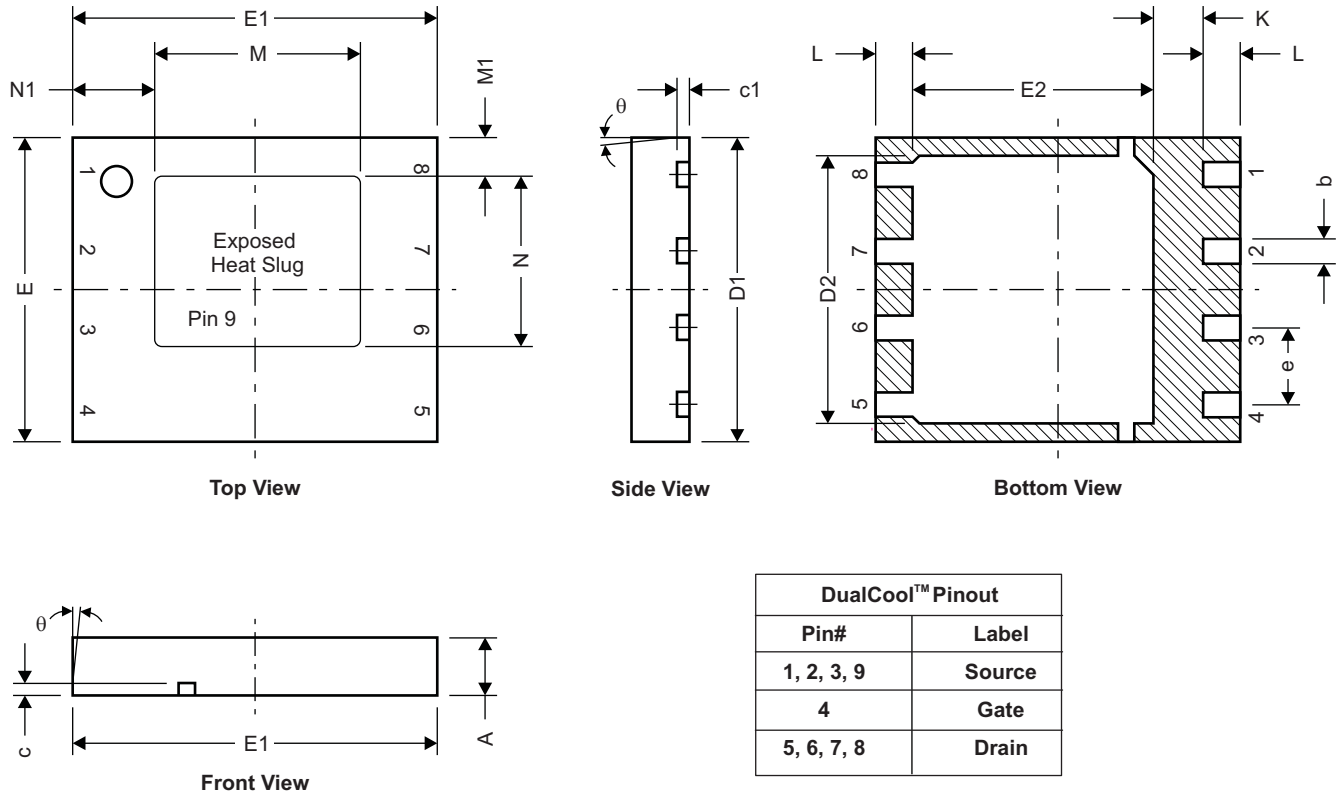


Figure 12. Maximum Drain Current vs. Temperature

**MECHANICAL DATA**

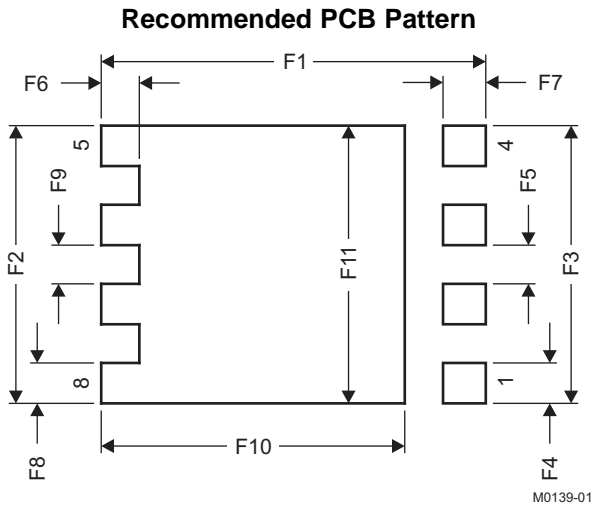
**Q5C Package Dimensions**



DualCool™ Pinout	
Pin#	Label
1, 2, 3, 9	Source
4	Gate
5, 6, 7, 8	Drain

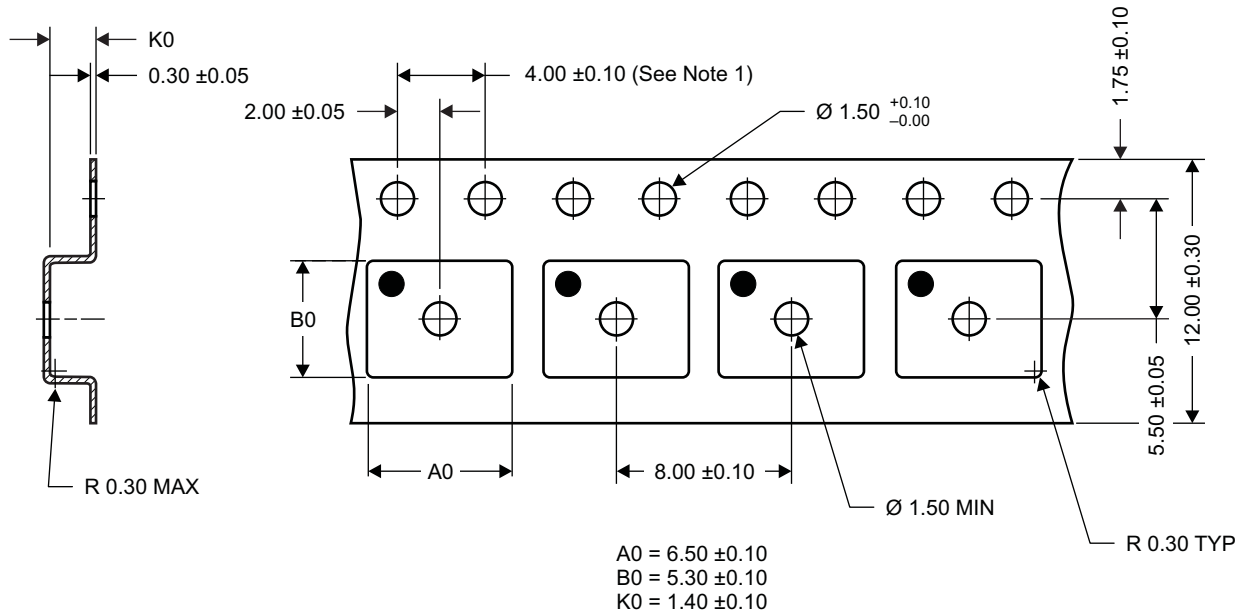
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DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
L	0.510	0.710	0.020	0.028
theta	-	-	-	-
K	0.760	-	0.030	-
M	3.260	3.460	0.128	0.136
M1	0.520	0.720	0.020	0.028
N	2.720	2.920	0.107	0.115
N1	1.227	1.427	0.048	0.056



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

**Q5C Tape and Reel Information**



M0138-01

**Notes:**

1. 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified.
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
6. MSL1 260°C (IR and convection) PbF reflow compatible

## REVISION HISTORY

### Changes from Original (December 2009) to Revision A

Page

- 
- Changed the labels on the Bottom View pinout image ..... 1
  - Changed the Mechanical Data dimensions table. Added dimensions for M, M1, N and N1 ..... 6
- 

### Changes from Revision A (April 2010) to Revision B

Page

- 
- Changed  $R_{DS(on)} - V_{GS} = 3V$  in the Electrical Characteristics table From: 2.7 To: 2.9 in the max column ..... 2
  - Deleted the Package Marking Information section ..... 7
-



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