DualCool™ N-Ch NexFET™ Power MOSFET

FEATURES

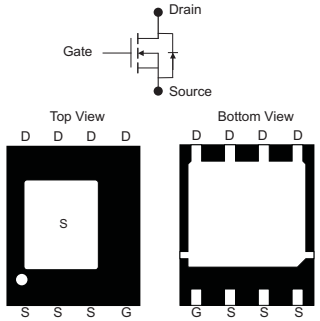
- Ultra Low Q_g and Q_{gd}
- DualCool™ Package
- Optimized for 2-Sided Cooling
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm x 6-mm Plastic Package

APPLICATIONS

- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Control FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (4.5V)	6.7		nC
Q_{gd}	Gate Charge Gate to Drain	1.9		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V	5.4	mΩ
		V_{GS} = 10V	3.6	mΩ
$V_{GS(th)}$	Threshold Voltage	1.8		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16408Q5C	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

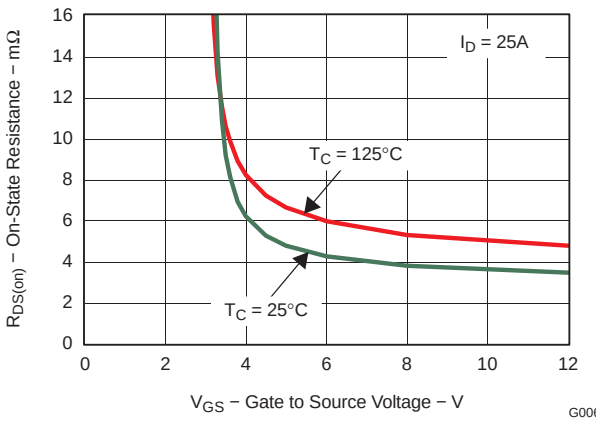
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+16 / –12	V
I_D	Continuous Drain Current, T_C = 25°C	113	A
	Continuous Drain Current (1)	22	A
I_{DM}	Pulsed Drain Current, T_A = 25°C (2)	141	A
P_D	Power Dissipation (1)	3.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 23A, L = 0.1mH, R_G = 25Ω	126	mJ

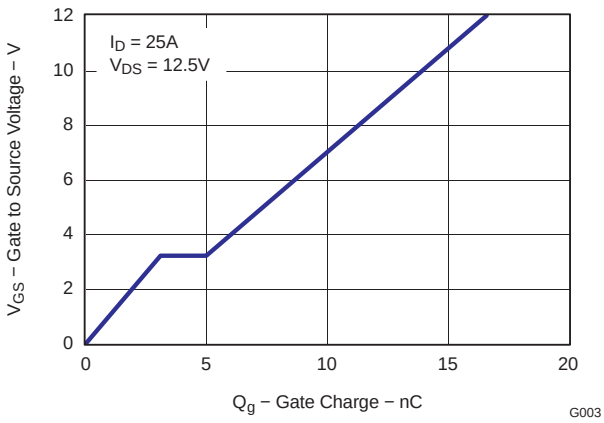
(1) Typical $R_{\theta JA}$ = 41°C/W on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤300μs, duty cycle ≤2%

$R_{DS(on)}$ vs V_{GS}



GATE CHARGE



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

T_A = 25°C unless otherwise stated

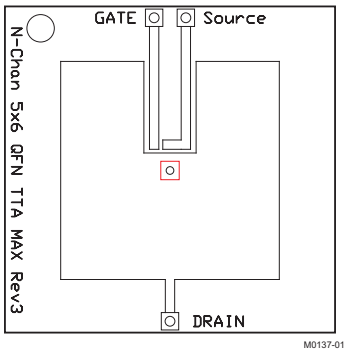
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250μA	25			V
I_{DSS}	Drain to Source Leakage	V_{GS} = 0V, V_{DS} = 20V			1	μA
I_{GSS}	Gate to Source Leakage	V_{DS} = 0V, V_{GS} = +16/-12V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.4	1.8	2.1	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_D = 25A		5.4	6.8	mΩ
		V_{GS} = 10V, I_D = 25A		3.6	4.5	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_D = 25A		60		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 12.5V , f = 1MHz		990	1300	pF
C_{OSS}	Output Capacitance			760	1000	pF
C_{RSS}	Reverse Transfer Capacitance			75	100	pF
R_g	Series Gate Resistance			0.8	1.6	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 12.5V, I_D = 25A		6.7	8.9	nC
Q_{gd}	Gate Charge – Gate to Drain			1.9		nC
Q_{gs}	Gate Charge – Gate to Source			3.1		nC
$Q_{g(th)}$	Gate Charge at Vth			1.8		nC
Q_{OSS}	Output Charge	V_{DS} = 13V, V_{GS} = 0V		15.7		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 25A, R_G = 2Ω		11.3		ns
t_r	Rise Time			25		ns
$t_{d(off)}$	Turn Off Delay Time			11		ns
t_f	Fall Time			10.8		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = 25A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 13V, I_F = 25A, di/dt = 300A/μs		17		nC
t_{rr}	Reverse Recovery Time	V_{DD} = 13V, I_F = 25A, di/dt = 300A/μs		21		ns

THERMAL CHARACTERISTICS

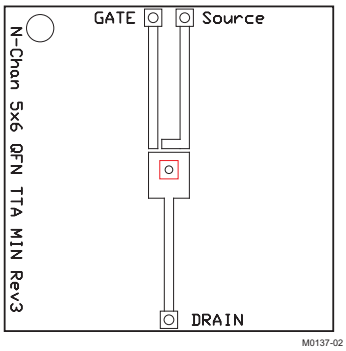
T_A = 25°C unless otherwise stated

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case (Top Source) (1)			3.1	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case (Bottom Drain) (1)			1.9	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (1) (2)			51	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 51ºC/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 125ºC/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

T_A = 25°C unless otherwise stated

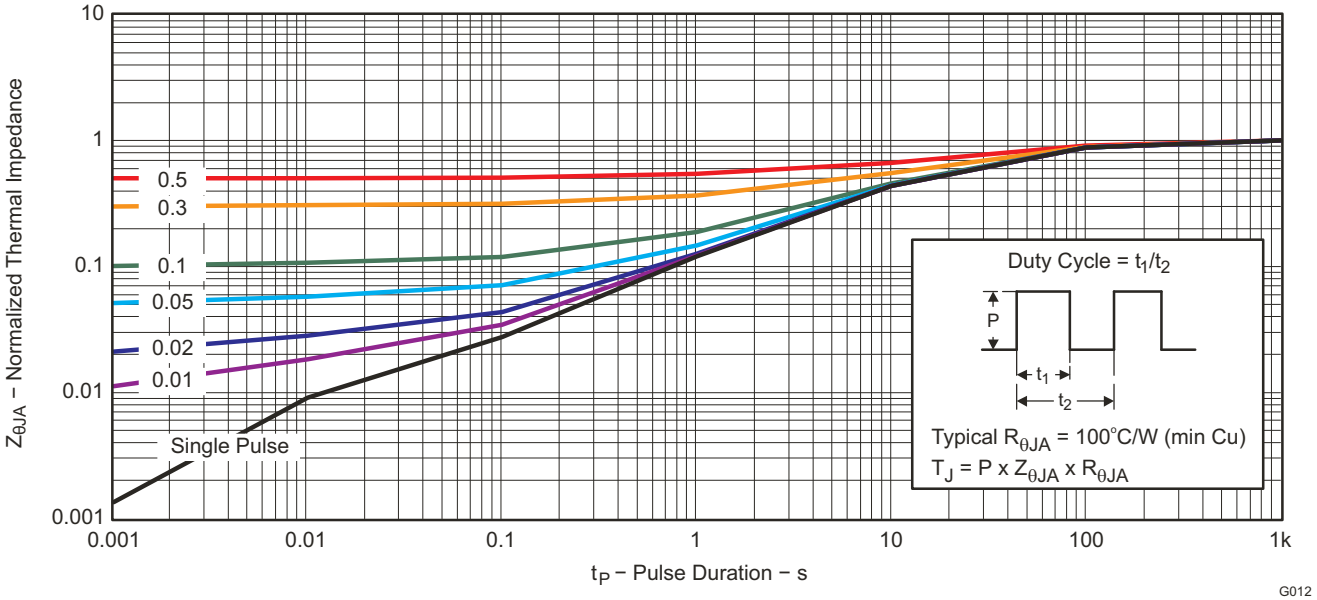


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

T_A = 25°C unless otherwise stated

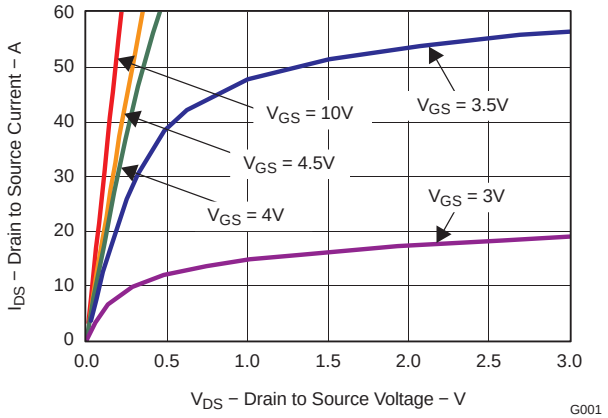


Figure 2. Saturation Characteristics

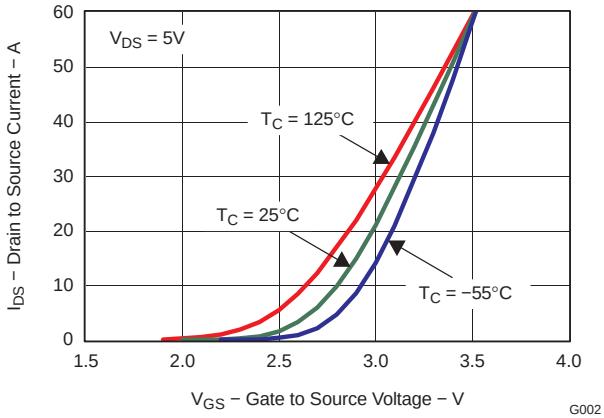


Figure 3. Transfer Characteristics

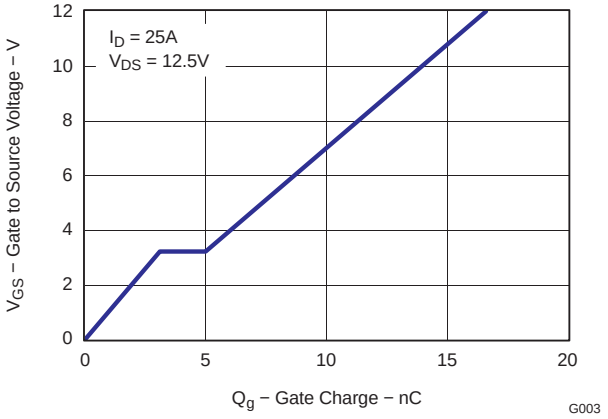


Figure 4. Gate Charge

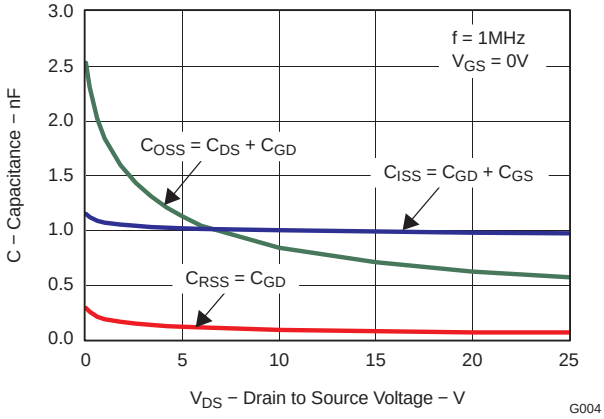


Figure 5. Capacitance

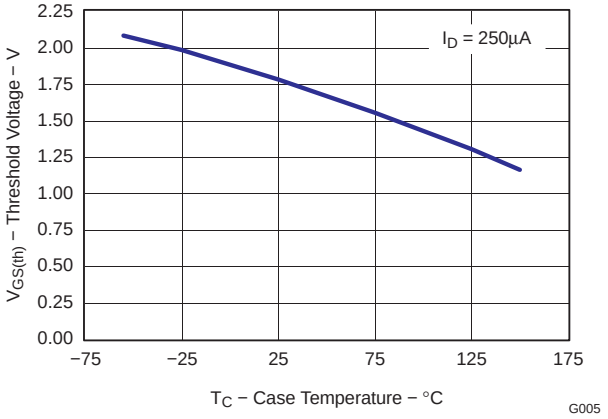


Figure 6. Threshold Voltage vs. Temperature

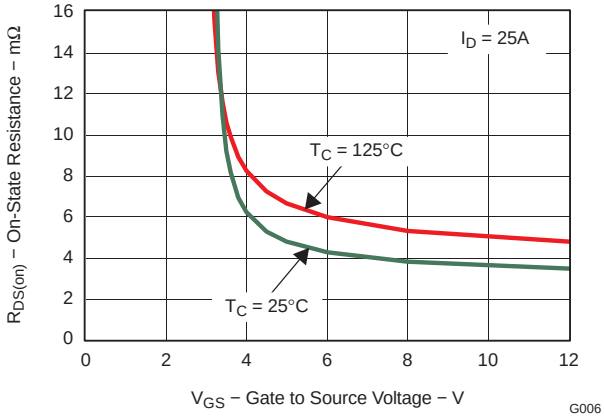


Figure 7. On-State Resistance vs. Gate to Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

T_A = 25°C unless otherwise stated

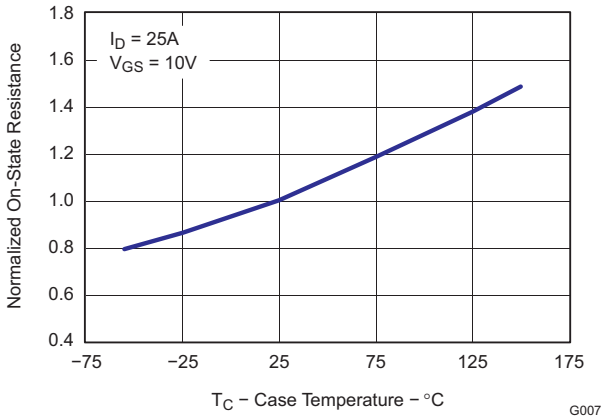


Figure 8. Normalized On-State Resistance vs. Temperature

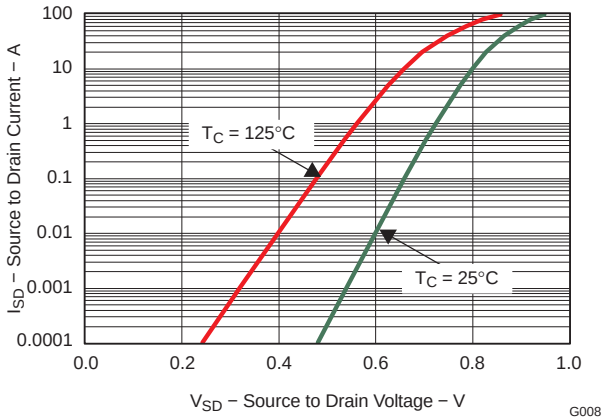


Figure 9. Typical Diode Forward Voltage

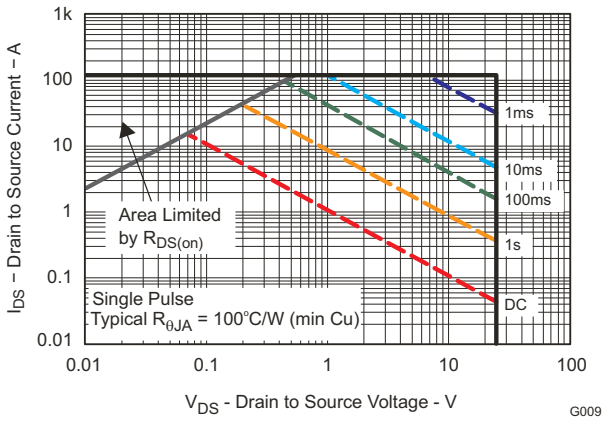


Figure 10. Maximum Safe Operating Area

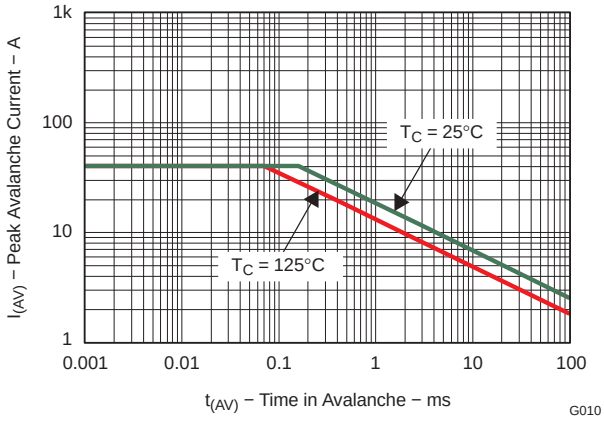


Figure 11. Single Pulse Unclamped Inductive Switching

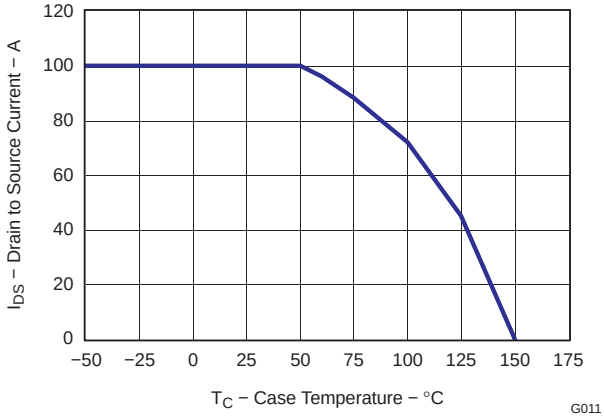
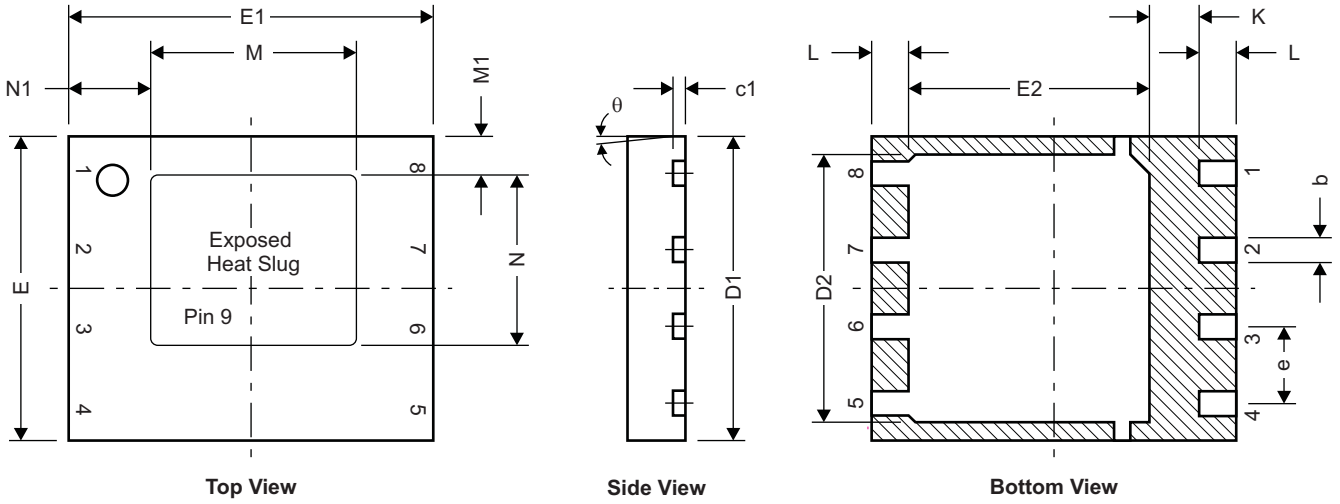


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q5C Package Dimensions

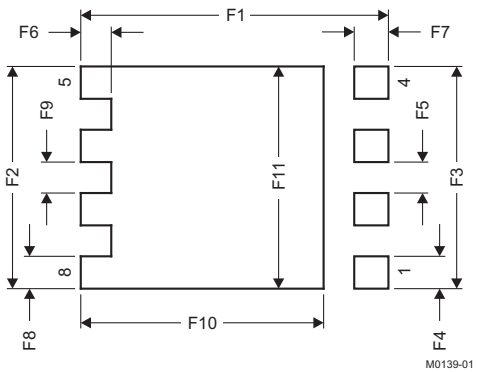


DualCool™ Pinout	
Pin#	**Label**
1, 2, 3, 9	**Source**
4	**Gate**
5, 6, 7, 8	**Drain**

M0162-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
K	0.760	–	0.030	–
L	0.510	0.710	0.020	0.028
θ	–	–	–	–
M	3.260	3.460	0.128	0.136
M1	0.520	0.720	0.020	0.028
N	2.720	2.920	0.107	0.115
N1	1.227	1.427	0.048	0.056

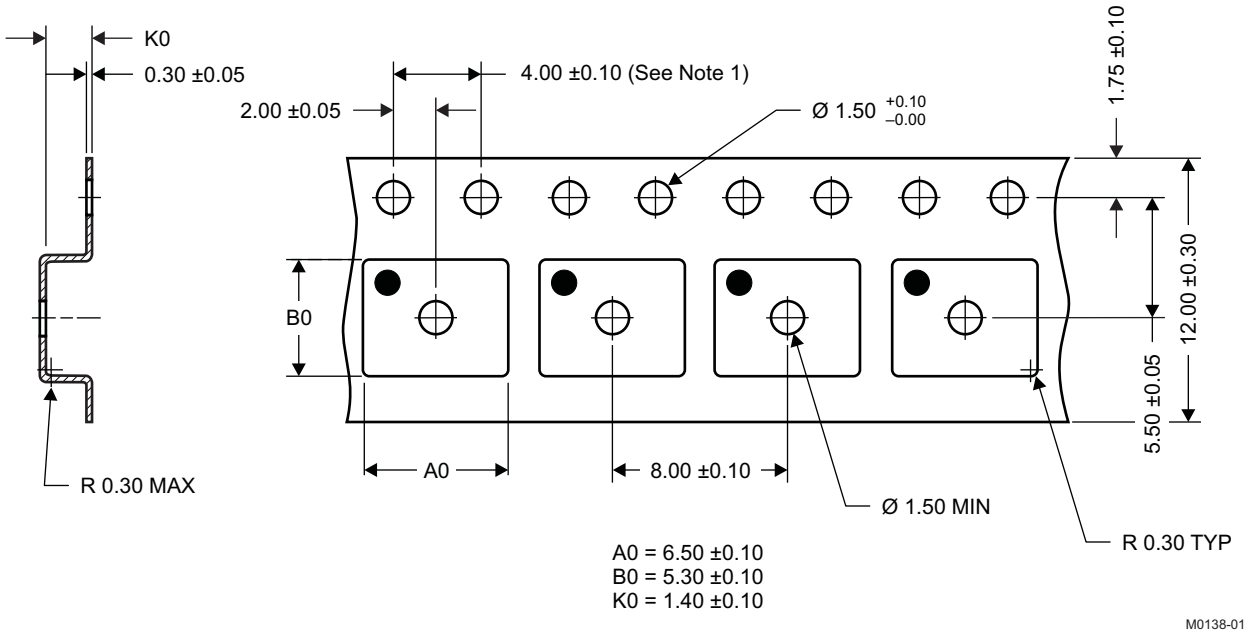
Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

Q5 Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified.
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
6. MSL1 260°C (IR and convection) PbF reflow compatible

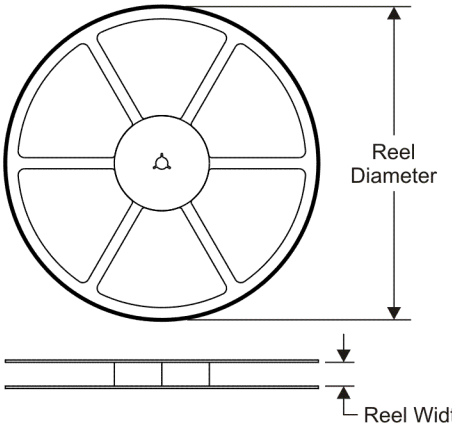
REVISION HISTORY

Changes from Original (December 2009) to Revision A	Page
• Changed the labels on the Bottom View pinout image	1

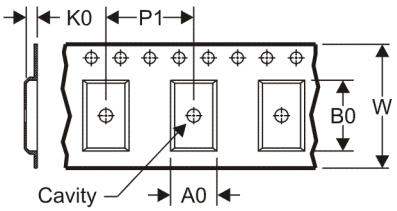
Changes from Revision A (February) to Revision B	Page
• the Package Marking Information section	7

TAPE AND REEL INFORMATION

REEL DIMENSIONS

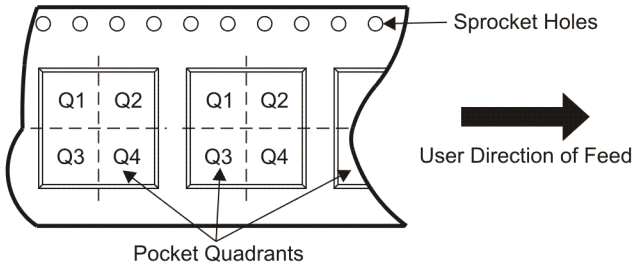


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

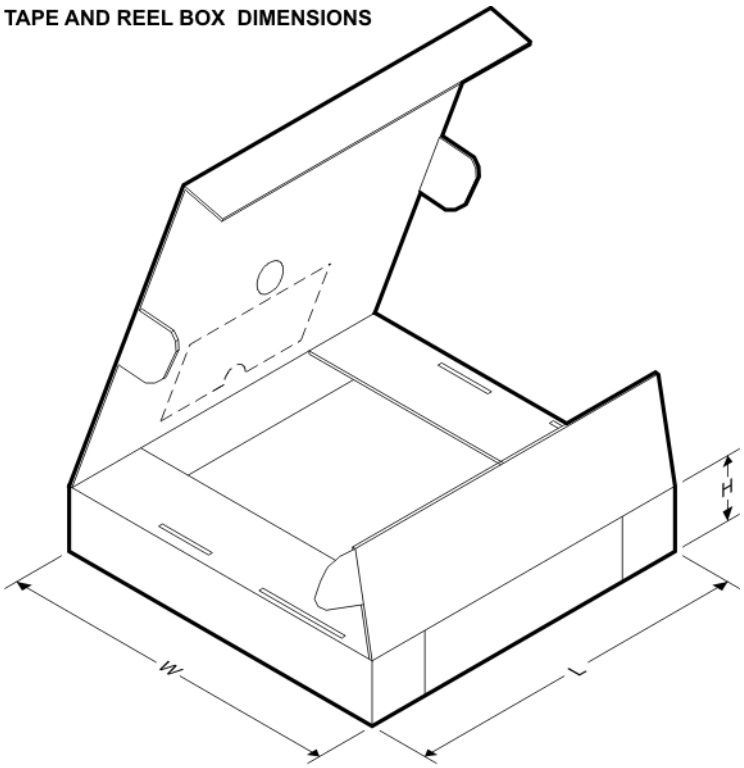
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16408Q5C	SON	DQU	8	2500	330.0	12.8	6.5	5.3	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16408Q5C	SON	DQU	8	2500	335.0	335.0	32.0

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