TEXAS INSTRUMENTS

CSD18502Q5B

SLPS320B – NOVEMBER 2012 – REVISED MAY 2017

CSD18502Q5B 40 V N-Channel NexFET™ Power MOSFET

1 Features

- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen-Free
- SON 5 mm × 6 mm Plastic Package

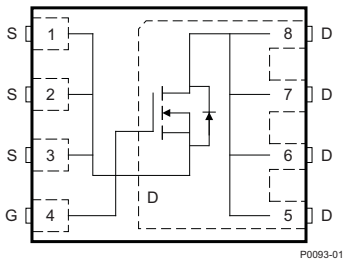
2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 40-V, 1.8-mΩ, 5 mm × 6 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain to source voltage	40		V
Q_g	Gate charge total (4.5 V)	25		nC
Q_{gd}	Gate charge gate to drain	8.4		nC
$R_{DS(on)}$	Drain to source on resistance	V_{GS} = 4.5 V	2.5	mΩ
		V_{GS} = 10 V	1.8	mΩ
$V_{GS(th)}$	Threshold voltage	1.8		V

Ordering Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18502Q5B	2500	13-Inch Reel	SON 5 mm × 6 mm Plastic Package	Tape and Reel
CSD18502Q5BT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

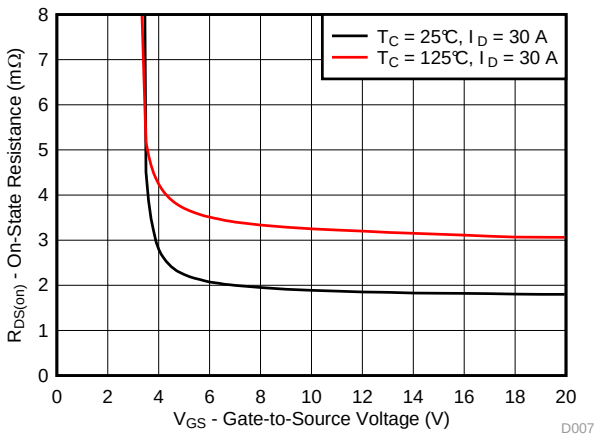
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain to source voltage	40	V
V_{GS}	Gate to source voltage	±20	V
I_D	Continuous drain current (package limited)	100	A
	Continuous drain current (silicon limited), T_C = 25°C	204	
	Continuous drain current(1)	26	
I_{DM}	Pulsed drain current(2)	400	A
P_D	Power dissipation(1)	3.2	W
	Power dissipation, T_C = 25°C	156	
T_J	Operating junction temperature	–55 to 150	°C
T_{stg}	Storage temperature	–55 to 150	°C
E_{AS}	Avalanche energy, single pulse I_D = 88 A, L = 0.1 mH, R_G = 25 Ω	387	mJ

(1) Typical $R_{\theta JA}$ = 40°C/W on a 1 inch^2 , 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 0.8°C/W, pulse duration ≤100 µs, duty cycle ≤1%

$R_{DS(on)}$ vs V_{GS}



Gate Charge

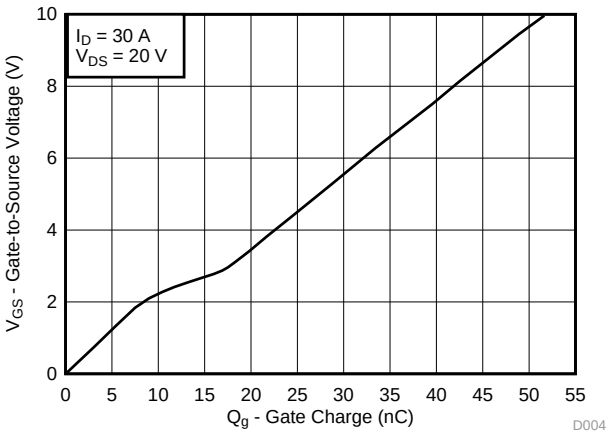


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2015) to Revision B **Page**

- Added *Receiving Notification of Documentation Updates* section. ... 7
- Changed the dimension between pads 3 and 4 from 0.028 inches: to 0.050 inches in the *Recommended PCB Pattern* section diagram ... 9

Changes from Original (November 2012) to Revision A **Page**

- Added part number to title. ... 1
- Added 7-inch reel to *Ordering Information*. ... 1
- Added power dissipation at T_C = 25°C to *Absolute Maximum Ratings*. ... 1
- Updated pulsed drain current conditions in *Absolute Maximum Ratings*. ... 1
- Updated Figure 1 to normalized $R_{\theta JC}$ curves. ... 4
- Updated SOA in Figure 10. ... 6
- Added *Community Resources*. ... 8
- Updated mechanical drawings to show additional dimensions. ... 8

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

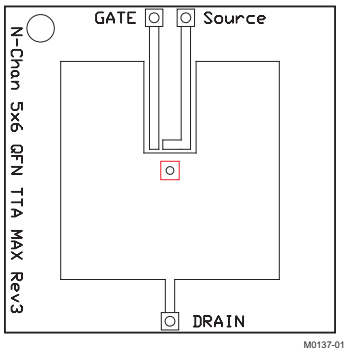
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain to source voltage	V_{GS} = 0 V, I_D = 250 μA	40			V
I_{DSS}	Drain to source leakage current	V_{GS} = 0 V, V_{DS} = 32 V			1	μA
I_{GSS}	Gate to source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate to source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.5	1.8	2.2	V
$R_{DS(on)}$	Drain to source on resistance	V_{GS} = 4.5 V, I_D = 30 A		2.5	3.3	mΩ
		V_{GS} = 10 V, I_D = 30 A		1.8	2.3	mΩ
g_{fs}	Transconductance	V_{DS} = 20 V, I_D = 30 A		143		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz		3900	5070	pF
C_{oss}	Output capacitance			900	1170	pF
C_{rss}	Reverse transfer capacitance			21	27	pF
R_G	Series gate resistance			1.2	2.4	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 20 V, I_D = 30 A		25	33	nC
Q_g	Gate charge total (10 V)			52	68	nC
Q_{gd}	Gate charge gate to drain			8.4		nC
Q_{gs}	Gate charge gate to source			10.3		nC
$Q_{g(th)}$	Gate charge at V_{th}			6.9		nC
Q_{oss}	Output charge	V_{DS} = 20 V, V_{GS} = 0 V		59		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 20 V, V_{GS} = 10 V, I_{DS} = 30 A, R_G = 0 Ω		5.3		ns
t_r	Rise time			6.8		ns
$t_{d(off)}$	Turn off delay time			23		ns
t_f	Fall time			4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 30 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 20 V, I_F = 30 A, di/dt = 300 A/μs		88		nC
t_{rr}	Reverse recovery time			44		ns

5.2 Thermal Information

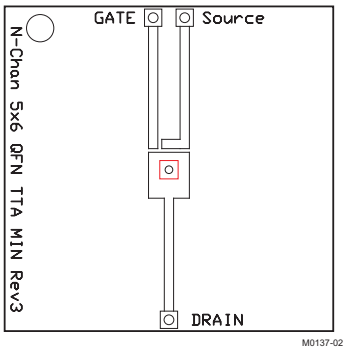
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case (top of package) thermal resistance (1)			0.8	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2 oz. (0.071 mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

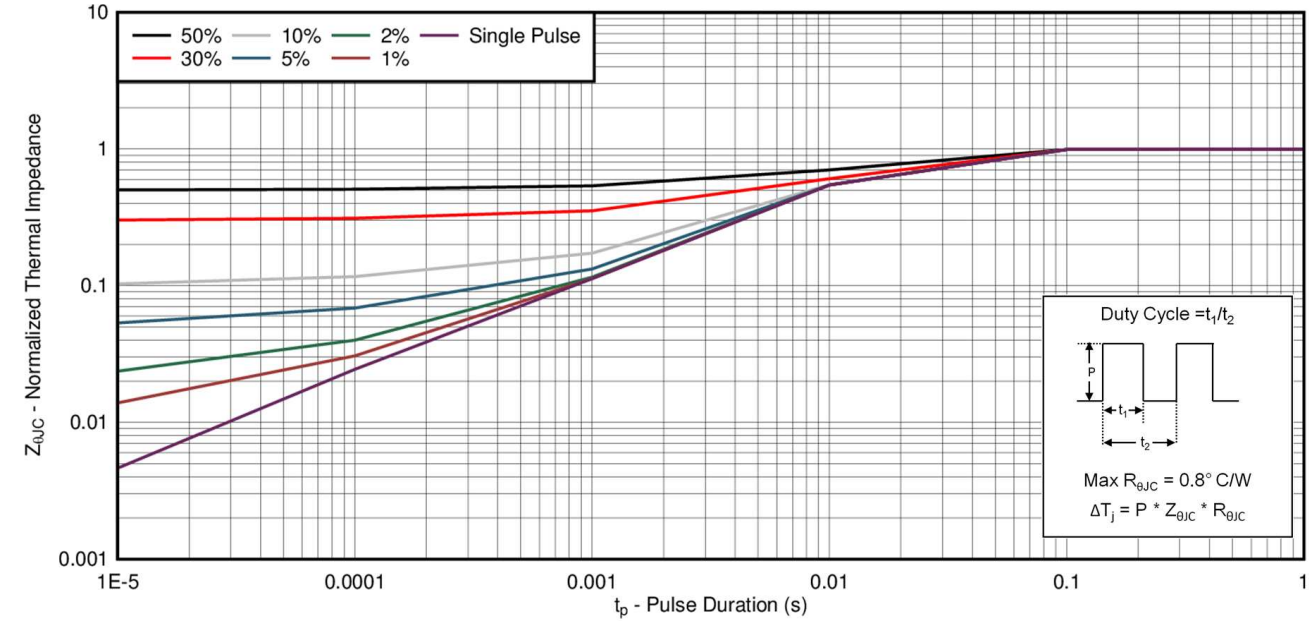


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

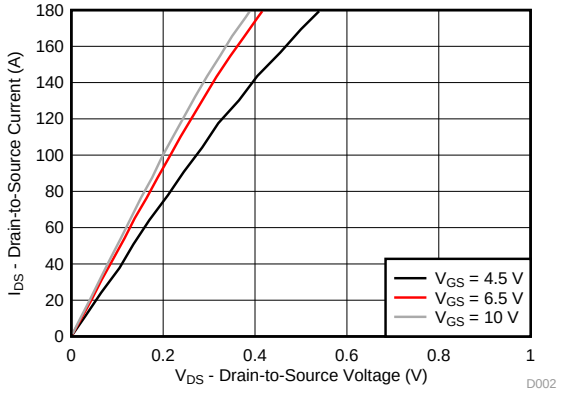


Figure 2. Saturation Characteristics

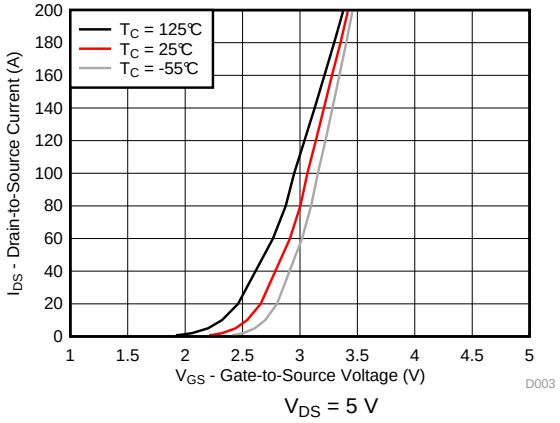


Figure 3. Transfer Characteristics

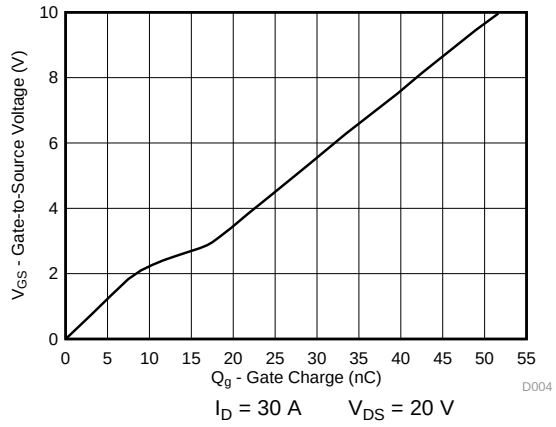


Figure 4. Gate Charge

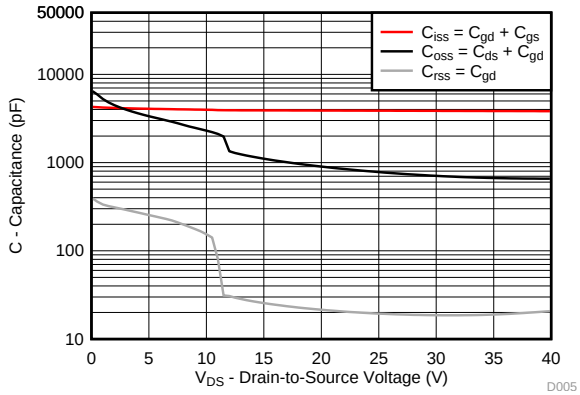


Figure 5. Capacitance

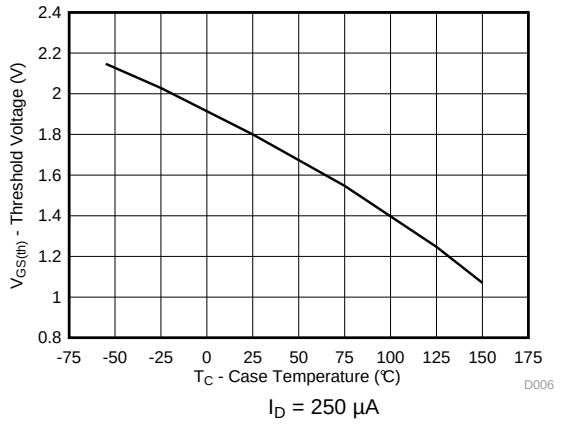


Figure 6. Threshold Voltage vs Temperature

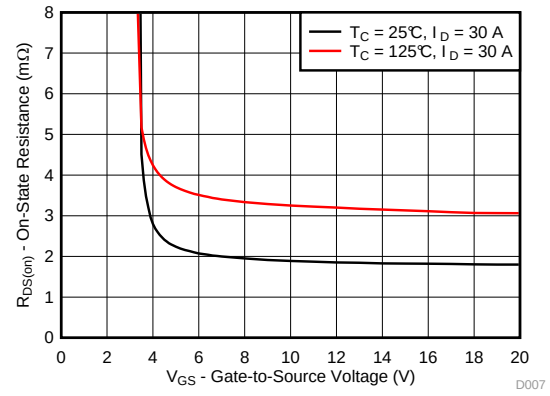
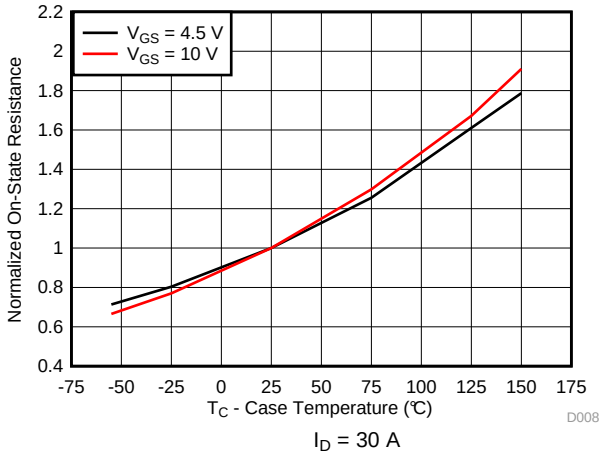


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)



ID = 30 A

Figure 8. Normalized On-State Resistance vs Temperature

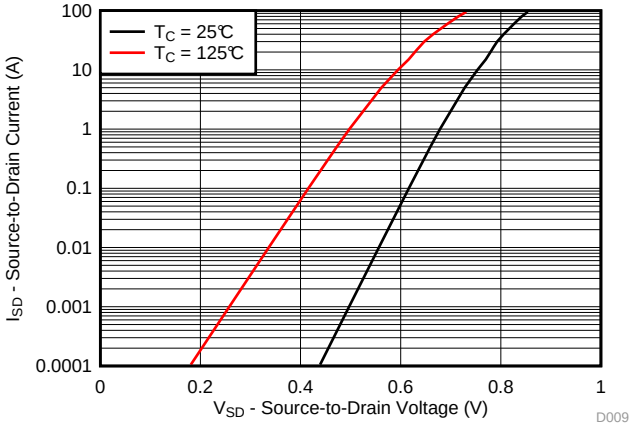
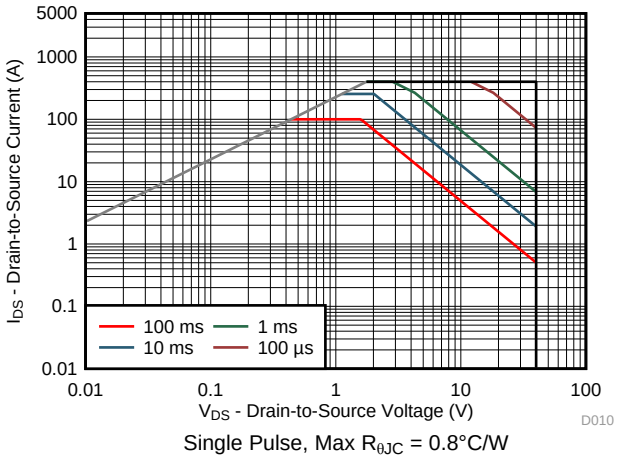


Figure 9. Typical Diode Forward Voltage



Single Pulse, Max $R_{\theta JC}$ = 0.8°C/W

Figure 10. Maximum Safe Operating Area

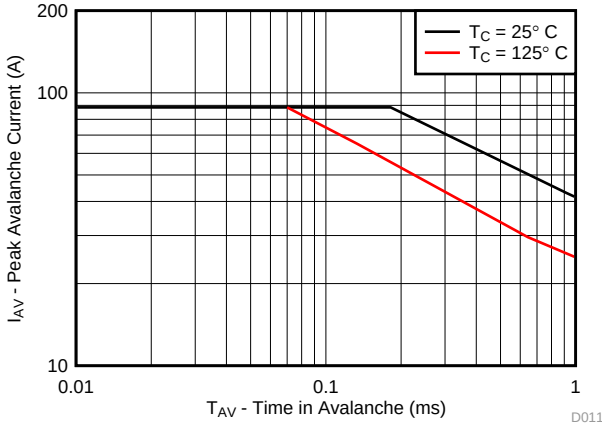


Figure 11. Single Pulse Unclamped Inductive Switching

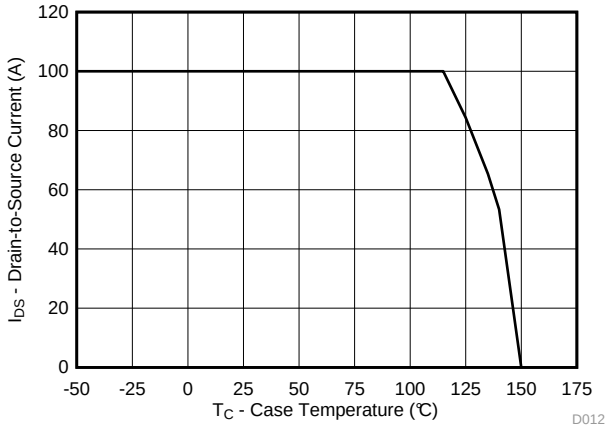


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

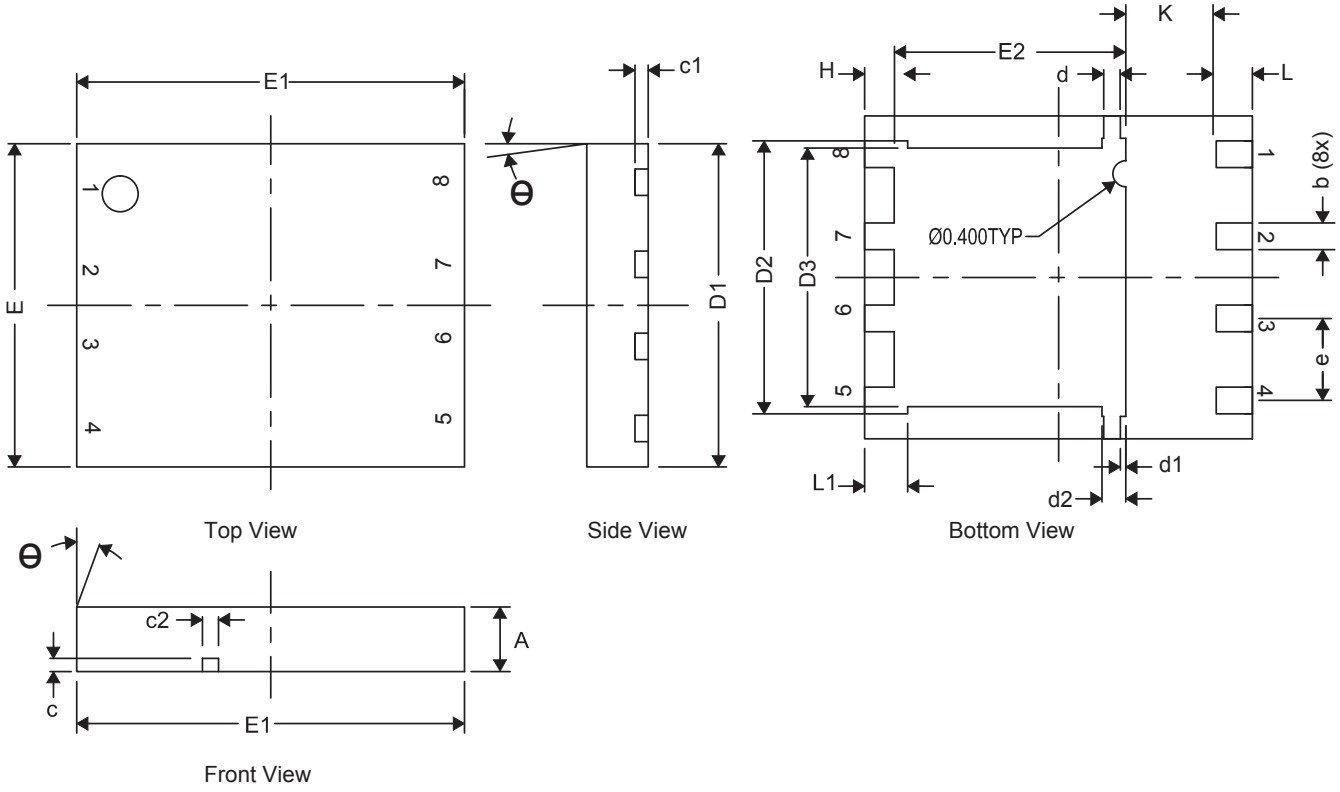
6.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

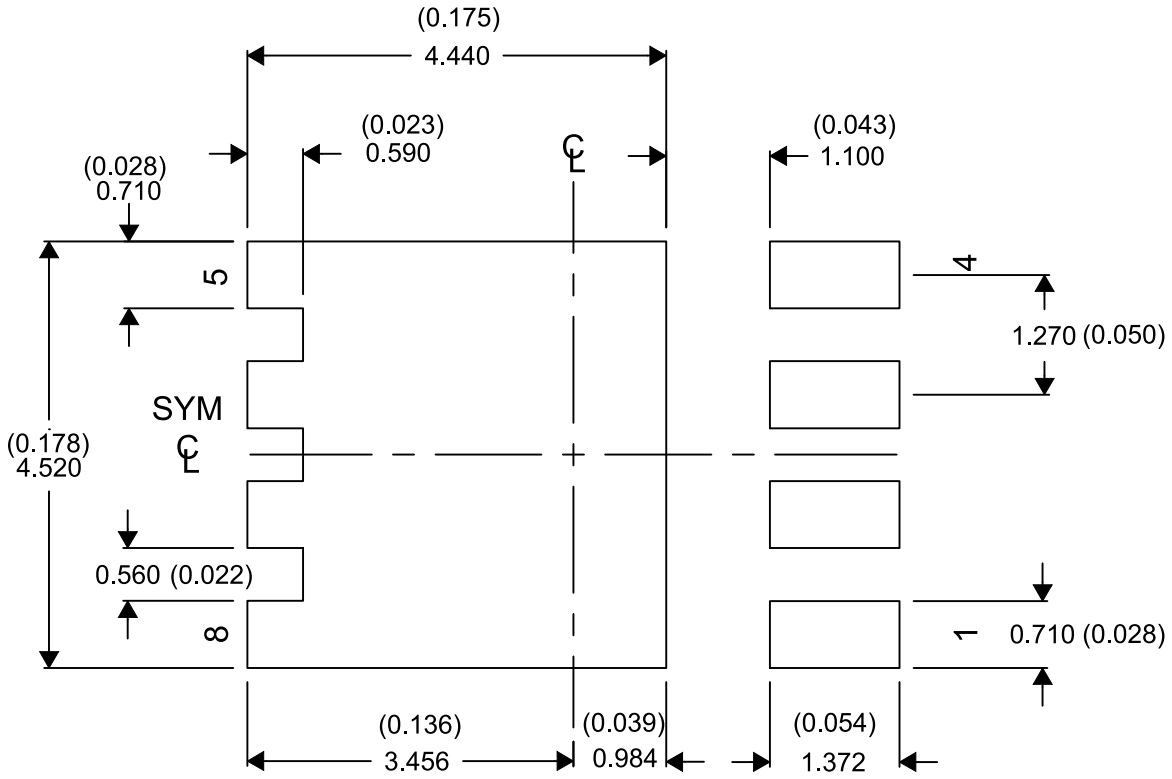
7 Mechanical, Packaging, and Orderable Information

7.1 Q5B Package Dimensions



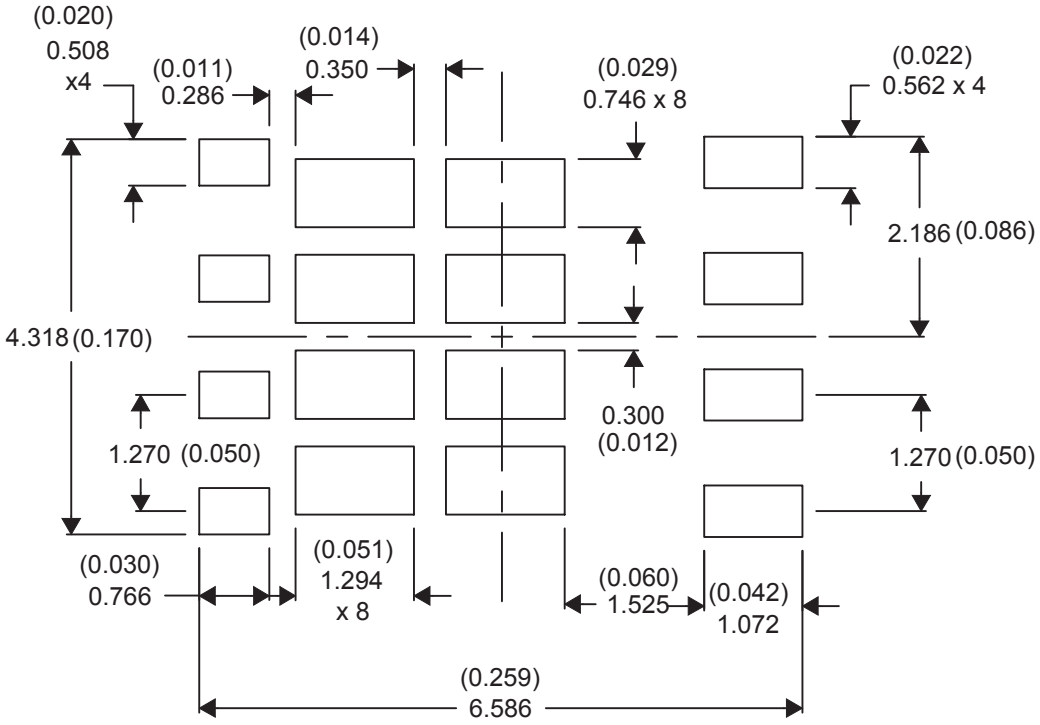
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.95	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
d	0.20	0.25	0.30
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e		1.27 TYP	
L	0.46	0.56	0.66
θ	0°	—	—
K		1.40 TYP	

7.2 Recommended PCB Pattern

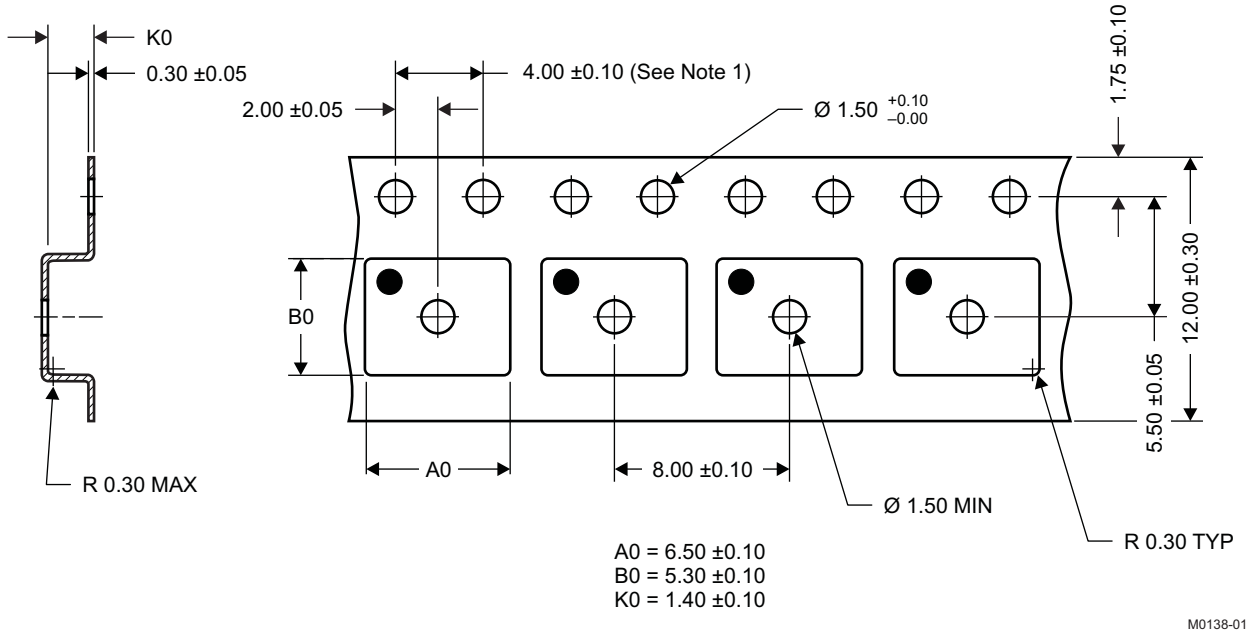


For recommended circuit layout for PCB designs, see *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

7.3 Recommended Stencil Pattern



7.4 Q5B Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18502Q5B	ACTIVE	VSON-CLIP	DNK	8	2500	Pb-Free (RoHS Exempt)	CU NIPDAU | CU SN	Level-1-260C-UNLIM		CSD18502	Samples
CSD18502Q5BT	ACTIVE	VSON-CLIP	DNK	8	250	Pb-Free (RoHS Exempt)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 150	CSD18502	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

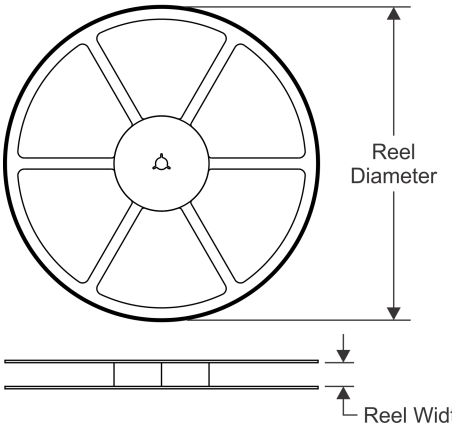
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

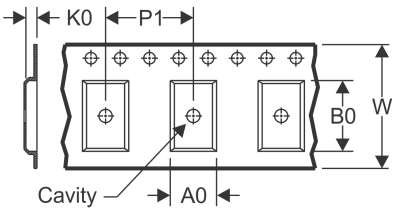
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

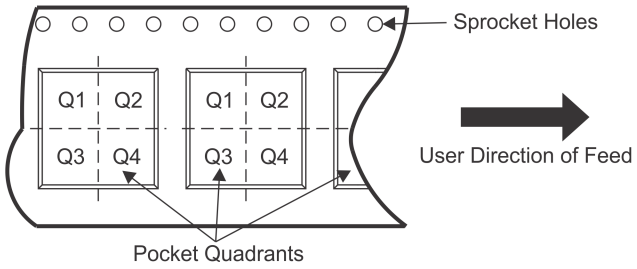


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

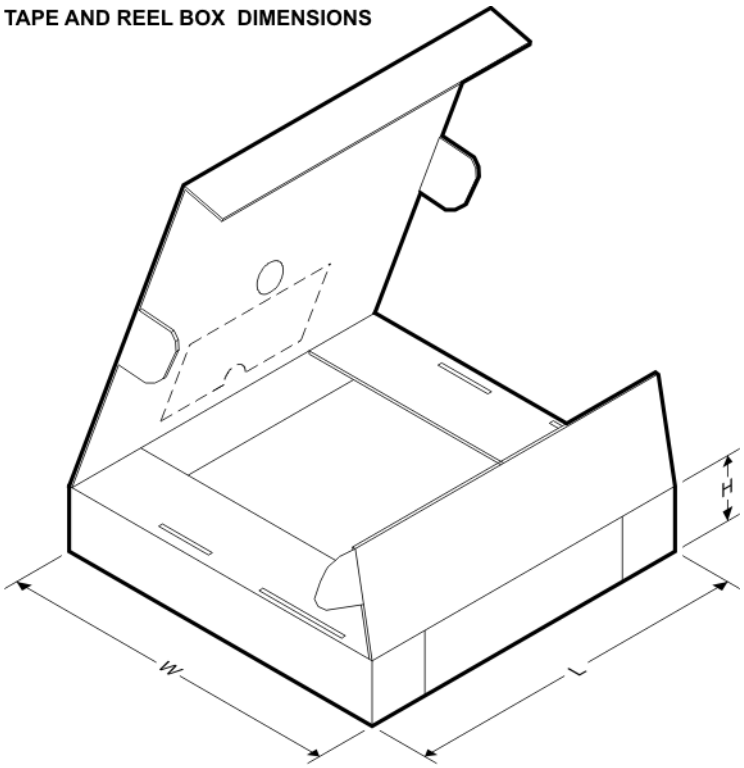
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18502Q5B	VSON-CLIP	DNK	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1
CSD18502Q5B	VSON-CLIP	DNK	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1
CSD18502Q5BT	VSON-CLIP	DNK	8	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18502Q5B	VSON-CLIP	DNK	8	2500	335.0	335.0	32.0
CSD18502Q5B	VSON-CLIP	DNK	8	2500	367.0	367.0	35.0
CSD18502Q5BT	VSON-CLIP	DNK	8	250	210.0	210.0	52.0

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265