

# CSD19531KCS 100-V N-Channel NexFET™ Power MOSFET

## 1 Features

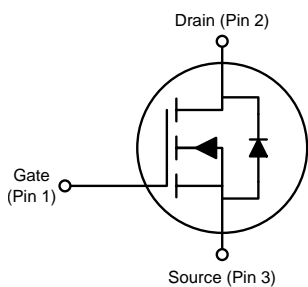
- Ultra-Low  $Q_g$  and  $Q_{gd}$
- Low-Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- TO-220 Plastic Package

## 2 Applications

- Secondary Side Synchronous Rectifier
- Hot Swap Telecom
- Motor Control

## 3 Description

This 100-V, 6.4-m $\Omega$ , TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	100		V
$Q_g$	Gate Charge Total (10 V)	37		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	7.5		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{ V}$	7.3	m $\Omega$
		$V_{GS} = 10\text{ V}$	6.4	
$V_{GS(th)}$	Threshold Voltage	2.7		V

### Device Information<sup>(1)</sup>

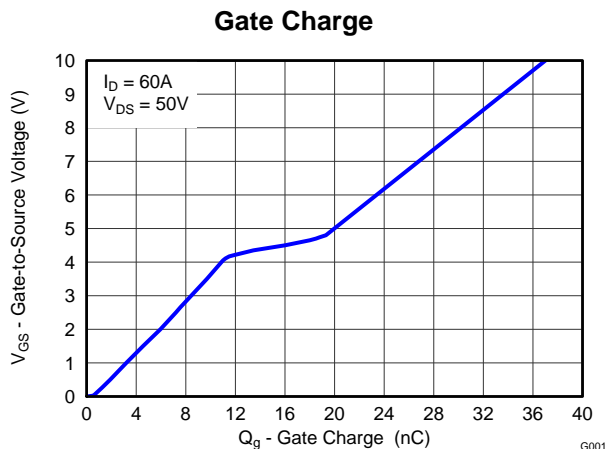
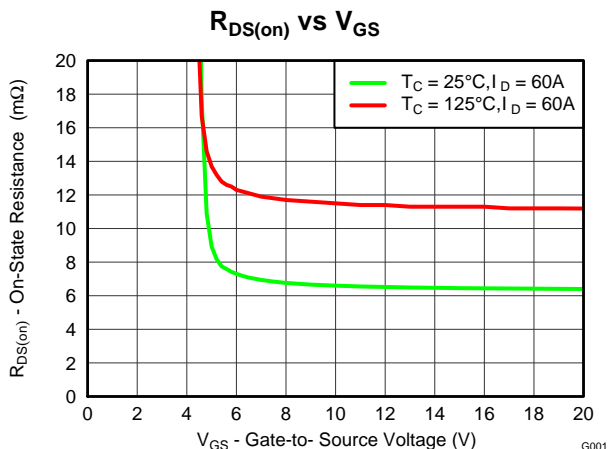
DEVICE	PACKAGE	MEDIA	QTY	SHIP
CSD19531KCS	TO-220 Plastic Package	Tube	50	Tube

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current (Package Limited)	100	A
	Continuous Drain Current (Silicon Limited), $T_C = 25^\circ\text{C}$	110	
	Continuous Drain Current (Silicon Limited), $T_C = 100^\circ\text{C}$	78	
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	285	A
$P_D$	Power Dissipation	214	W
$T_J, T_{stg}$	Operating Junction, Storage Temperature	-55 to 175	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, Single Pulse $I_D = 60\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	180	mJ

(1) Max  $R_{\theta JC} = 0.7^\circ\text{C/W}$ , pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$ .



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## 4 Revision History

### Changes from Revision B (June 2014) to Revision C Page

• Added <i>Receiving Notification of Documentation Updates</i> section and <i>Community Resources</i> section to the <i>Device and Documentation Support</i> section .....	7
• Changed package drawing in <i>KCS Package Dimensions</i> section .....	8

### Changes from Revision A (May 2014) to Revision B Page

• Added value for max $Q_g$ .....	3
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### Changes from Original (September 2013) to Revision A Page

• Updated the silicon limited currents to reflect increase in device operating temperature range .....	1
• Increased pulsed current to reflect new conditions .....	1
• Increased max power dissipation to reflect new conditions .....	1
• Increased operating and junction temperature range to 175°C .....	1
• Updated the pulsed drain current conditions .....	1
• Changed <a href="#">Figure 1</a> from a normalized $R_{\theta JA}$ curve to a normalized $R_{\theta JC}$ curve .....	4
• Updated <a href="#">Figure 6</a> to reflect increase in device operating temperature range .....	5
• Updated <a href="#">Figure 8</a> to reflect increase in device operating temperature range .....	5
• Updated <a href="#">Figure 10</a> to reflect measured SOA data .....	6
• Updated <a href="#">Figure 12</a> to reflect increase in device operating temperature range .....	6

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.2	2.7	3.3	V
$R_{DS(on)}$	Drain-to-source on resistance	$V_{GS} = 6\text{ V}, I_D = 60\text{ A}$		7.3	8.8	m $\Omega$
		$V_{GS} = 10\text{ V}, I_D = 60\text{ A}$		6.4	7.7	
$g_{fs}$	Transconductance	$V_{DS} = 10\text{ V}, I_D = 60\text{ A}$		137		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}, f = 1\text{ MHz}$		2980	3870	pF
$C_{oss}$	Output capacitance			560	728	pF
$C_{rss}$	Reverse transfer capacitance			13	17	pF
$R_G$	Series gate resistance			1.3	2.6	$\Omega$
$Q_g$	Gate charge total (10 V)	$V_{DS} = 50\text{ V}, I_D = 60\text{ A}$		38	49	nC
$Q_{gd}$	Gate charge gate-to-drain			7.5		nC
$Q_{gs}$	Gate charge gate-to-source			11.9		nC
$Q_{g(th)}$	Gate charge at $V_{th}$			7.3		nC
$Q_{oss}$	Output charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		98		nC
$t_{d(on)}$	Turnon delay time	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 60\text{ A}, R_G = 0\ \Omega$		8.4		ns
$t_r$	Rise Time			7.2		ns
$t_{d(off)}$	Turnoff delay time			16		ns
$t_f$	Fall time			4.1		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_{SD} = 60\text{ A}, V_{GS} = 0\text{ V}$		0.9	1	V
$Q_{rr}$	Reverse recovery charge	$V_{DS} = 50\text{ V}, I_F = 60\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		270		nC
$t_{rr}$	Reverse recovery time			83		ns

### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.7	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	$^\circ\text{C}/\text{W}$

### 5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

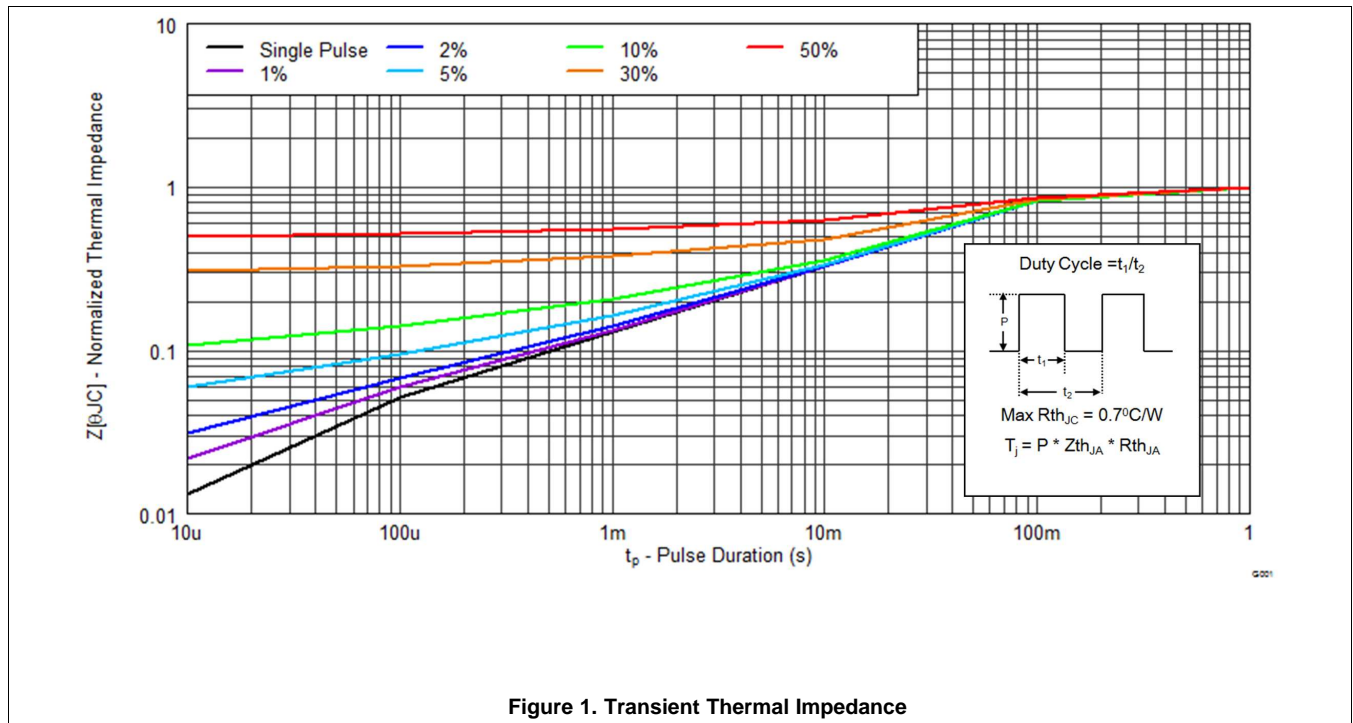


Figure 1. Transient Thermal Impedance

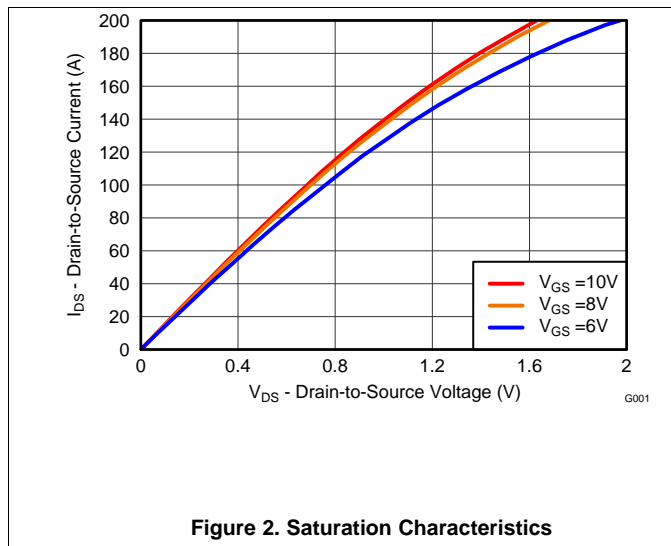


Figure 2. Saturation Characteristics

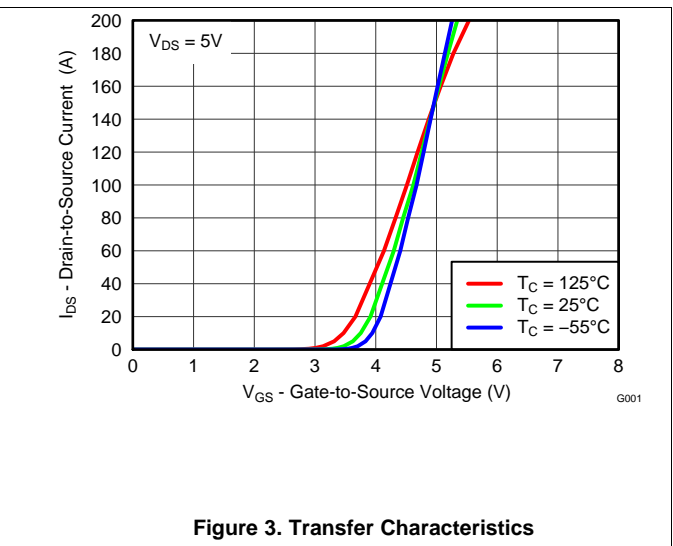
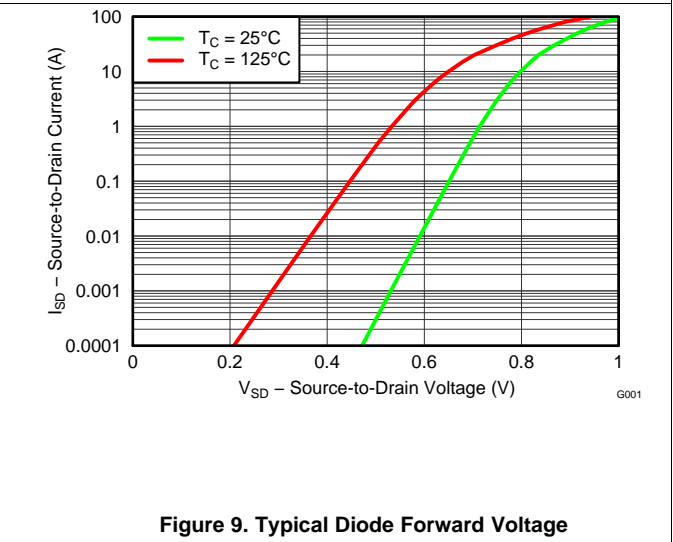
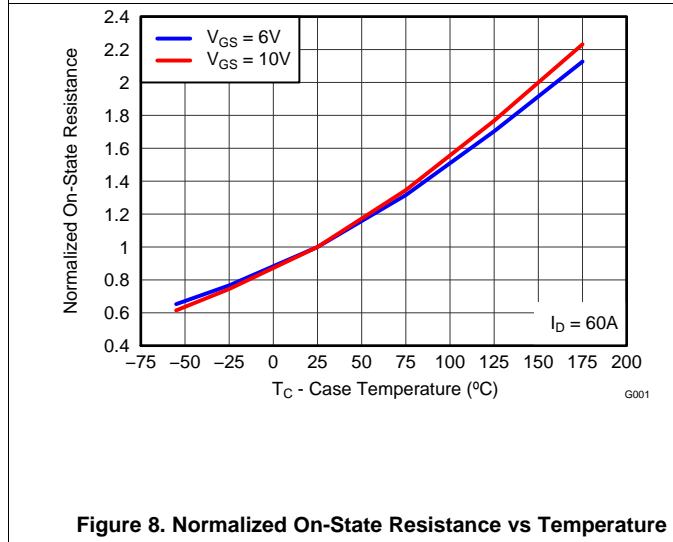
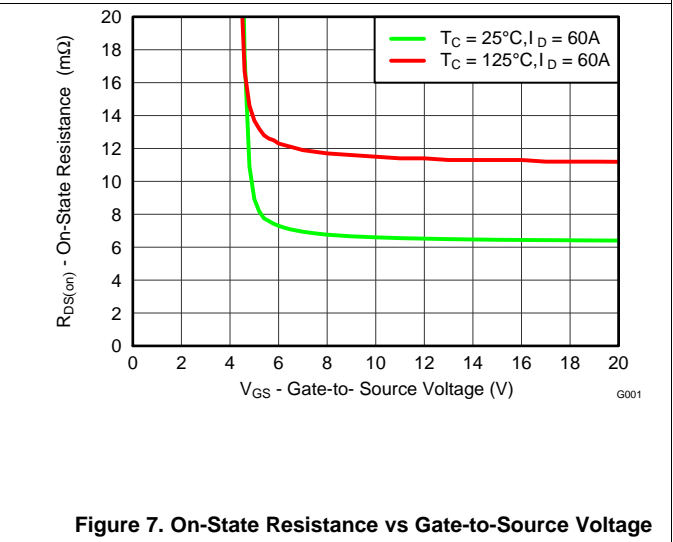
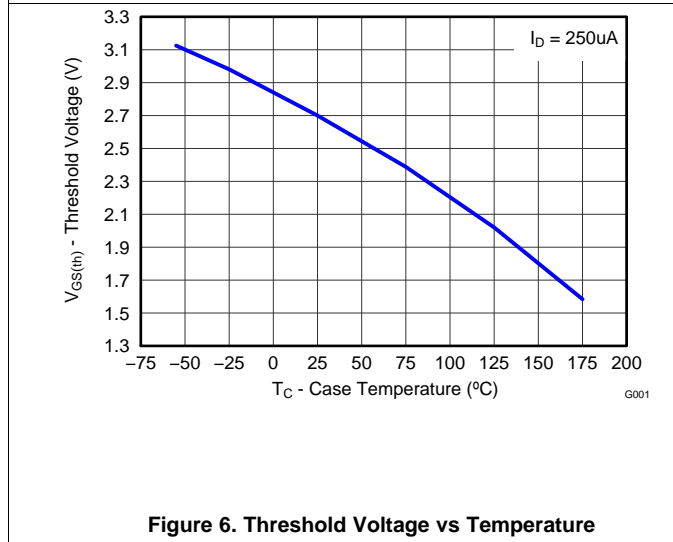
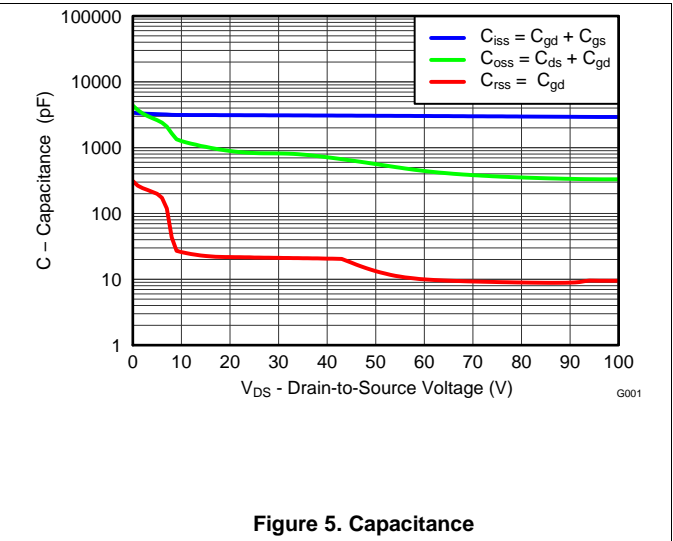
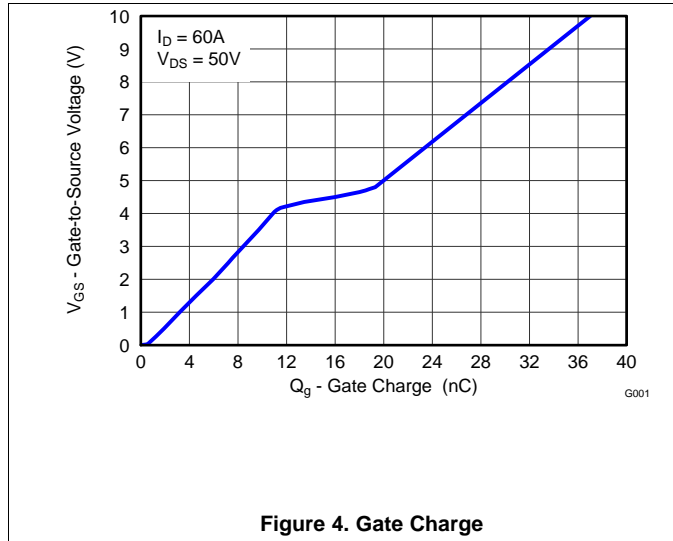


Figure 3. Transfer Characteristics

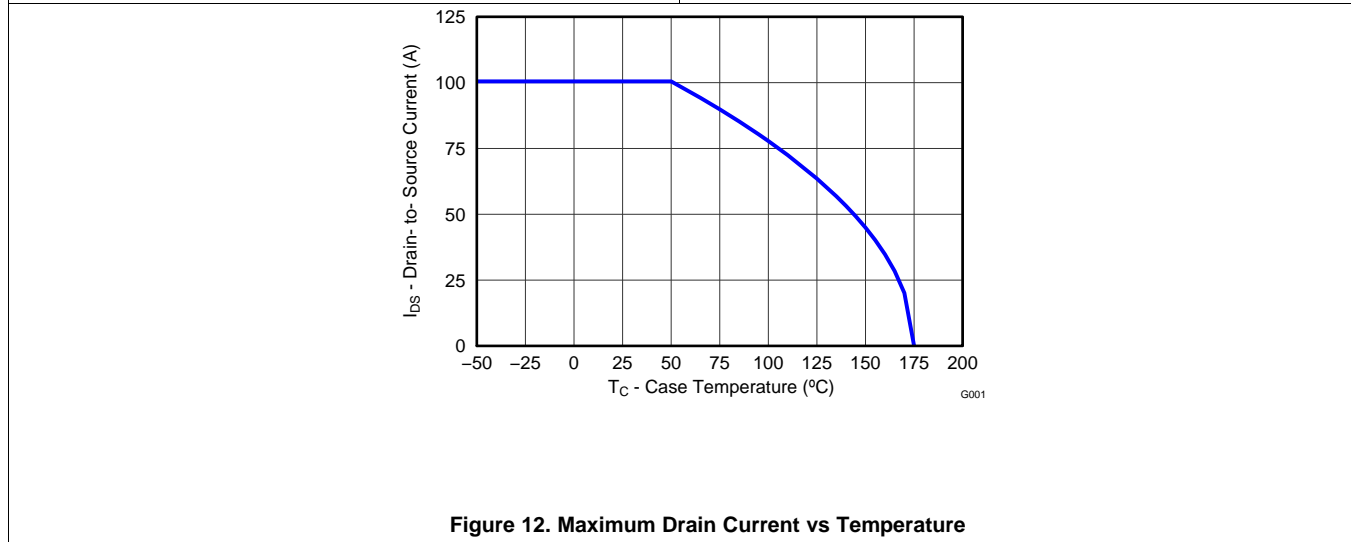
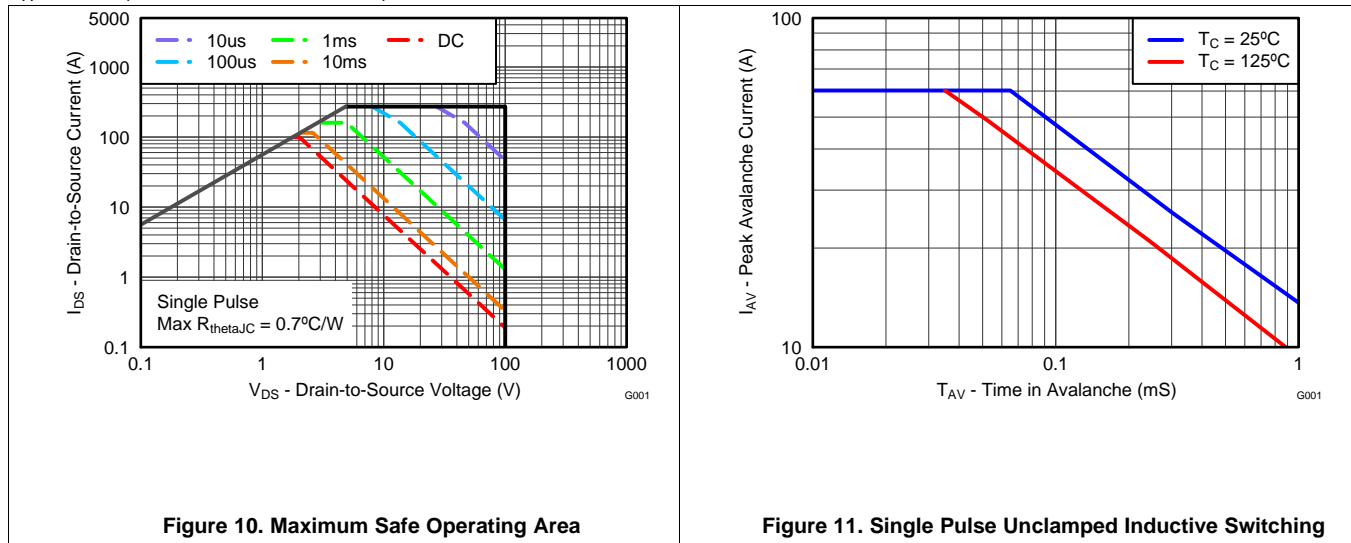
Typical MOSFET Characteristics (continued)

T<sub>A</sub> = 25°C (unless otherwise stated)



**Typical MOSFET Characteristics (continued)**

$T_A = 25^\circ\text{C}$  (unless otherwise stated)



## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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### 6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.  
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### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.5 Glossary

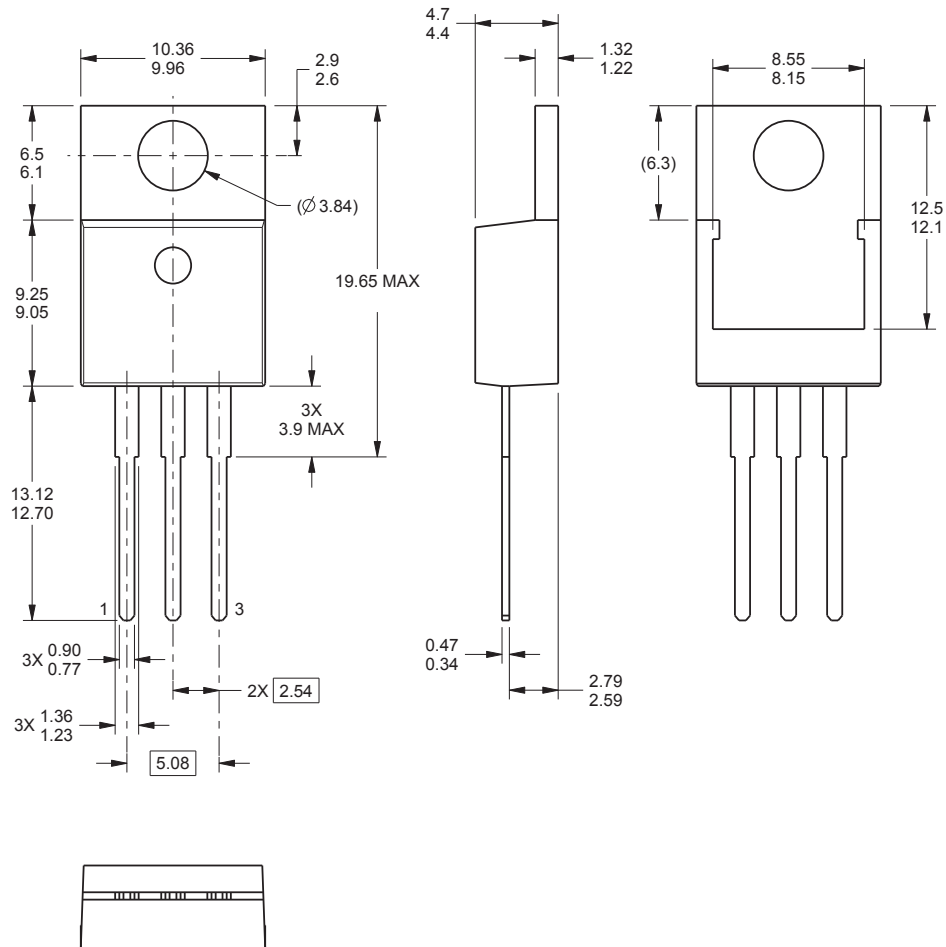
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 KCS Package Dimensions



4222214/A 10/2015

#### Notes:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.

**Table 1. Pin Configuration**

POSITION	DESIGNATION
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19531KCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-55 to 175	CSD19531KCS	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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