CSD95490Q5MC Synchronous Buck NexFET™ Smart Power Stage

1 Features
- 75-A Continuous Operating Current Capability
- Over 95% System Efficiency at 30 A
- High-Frequency Operation (up to 1.25 MHz)
- Diode Emulation Function
- Temperature Compensated Bi-Directional Current Sense
- Analog Temperature Output
- Fault Monitoring
- 3.3-V and 5-V PWM Signal Compatible
- Tri-State PWM Input
- Integrated Bootstrap Switch
- Optimized Dead Time for Shoot-Through Protection
- High-Density QFN 5-mm × 6-mm Footprint
- Ultra-Low-Inductance Package
- System Optimized PCB Footprint
- Thermally Enhanced Topside Cooling
- RoHS Compliant – Lead-Free Terminal Plating
- Halogen Free

2 Applications
- Multiphase Synchronous Buck Converters
  - High-Frequency Applications
  - High-Current, Low-Duty Cycle Applications
- POL DC-DC Converters
- Memory and Graphic Cards
- Desktop and Server VR12.x / VR13.x V-Core Synchronous Buck Converters
- High-Current POL for Network Communications

3 Description
The CSD95490Q5MC NexFET™ power stage is a highly optimized design for use in a high-power, high-density synchronous buck converter. This product integrates the driver IC and power MOSFETs to complete the power stage switching function. This combination produces high-current, high-efficiency, and high-speed switching capability in a small 5-mm × 6-mm outline package. It also integrates the accurate current sensing and temperature sensing functionality to simplify system design and improve accuracy. In addition, the PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design.

Application Diagram

Device Information

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>MEDIA</th>
<th>QTY</th>
<th>PACKAGE</th>
<th>SHIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSD95490Q5MC</td>
<td>13-Inch Reel</td>
<td>2500</td>
<td>QFN</td>
<td>Tape and Reel</td>
</tr>
<tr>
<td>CSD95490Q5MCT</td>
<td>7-Inch Reel</td>
<td>250</td>
<td>5.00-mm × 6.00-mm Package</td>
<td></td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Power Stage Efficiency and Power Loss

V_{DD} = 5 V
V_{IN} = 12 V
V_{OUT} = 1.8 V
L_{OUT} = 150 nH
f_{SW} = 600 kHz
T_{A} = 25°C

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

Changes from Original (March 2017) to Revision A Page

• Updated Mechanical Drawing section .......................................................... 7
5 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>REFIN</td>
<td>External reference voltage input for current sensing amplifier.</td>
</tr>
<tr>
<td>IOUT</td>
<td>Output of current sensing amplifier. V(IOUT) – V(REFIN) is proportional to the phase current.</td>
</tr>
<tr>
<td>LSET</td>
<td>A resistor from this pin to PGND pin sets the inductor value for the internal current sensing circuitry.</td>
</tr>
<tr>
<td>VDD</td>
<td>Supply voltage for gate drivers and internal circuitry.</td>
</tr>
<tr>
<td>VOS</td>
<td>Output voltage sensing pin for the internal current sensing circuitry.</td>
</tr>
<tr>
<td>SW</td>
<td>Phase node connecting the HS MOSFET source and LS MOSFET drain – pin connection to the output inductor.</td>
</tr>
<tr>
<td>VIN</td>
<td>Input voltage pin. Connect input capacitors close to this pin.</td>
</tr>
<tr>
<td>BOOTR</td>
<td>Return path for HS gate driver. It is connected to VSW internally.</td>
</tr>
<tr>
<td>BOOT</td>
<td>Bootstrap capacitor connection. Connect a minimum 0.1-µF, 16-V, X5R ceramic cap from BOOT to BOOTR pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated.</td>
</tr>
<tr>
<td>PWM</td>
<td>Tri-state input from external controller. Logic low sets control FET gate low and sync FET gate high. Logic high sets control FET gate high and sync FET gate low. Both MOSFET gates are set low if PWM stays in Hi-Z for greater than the tri-state shutdown hold-off time (t_{3HT}).</td>
</tr>
<tr>
<td>EN/FCCM</td>
<td>This dual function pin either enables the diode emulation function or can be used as a simple enable for the device. When this pin is driven into the tri-state window and held there for more than the tri-state holdoff time, Diode Emulation Mode (DEM) is enabled for sync FET. When the pin is high, device operates in Forced Continuous Conduction Mode (FCCM). When the pin is low, both FETs are held off. An internal resistor pulls this pin low if left floating.</td>
</tr>
<tr>
<td>TAO/FAULT</td>
<td>Temperature Amplifier Output. Reports a voltage proportional to the IC temperature. An ORing diode is integrated in the IC. When used in multiphase application, a single wire can be used to connect the TAO pins of all the ICs. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if thermal shutdown, LSOC, or HSS detection circuit is tripped.</td>
</tr>
<tr>
<td>PGND</td>
<td>Power ground.</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

\( T_A = 25^\circ C \) (unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{IN to P}} )</td>
<td>–0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{IN to V}} )</td>
<td>–0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{SW to P}} )</td>
<td>–0.3</td>
<td>23</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{SW to V}} ) (10 ns)</td>
<td>23</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{DD to P}} )</td>
<td>–7</td>
<td>23</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{DD to V}} ) (10 ns)</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{DD}} )</td>
<td>( V_{\text{DD}} + 0.3 )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( \text{REFIN} )</td>
<td>–0.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>( \text{BOOT to BOOTR} )</td>
<td>–0.3</td>
<td>( V_{\text{DD}} + 0.3 )</td>
<td>V</td>
</tr>
<tr>
<td>( \text{BOOT to P} )</td>
<td>–0.3</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>( T_J )</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{\text{STG}} )</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Should not exceed 7 V.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>( V_{\text{ESD}} )</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM)</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM)</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

6.3 Recommended Operating Conditions

\( T_A = 25^\circ C \) (unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{DD}} )</td>
<td>Driver supply voltage</td>
<td>4.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{IN}} )</td>
<td>Input supply voltage(1)</td>
<td>4.5</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{OUT}} )</td>
<td>Output voltage</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>PWM</td>
<td>PWM to ( P_{\text{GND}} )</td>
<td>( V_{\text{DD}} + 0.3 )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{OUT}} )</td>
<td>Continuous output current</td>
<td>( V_{\text{IN}} = 12 \text{ V}, V_{\text{DD}} = 5 \text{ V}, V_{\text{OUT}} = 1.2 \text{ V}, f_{\text{SW}} = 500 \text{ kHz} )</td>
<td>75</td>
<td>A</td>
</tr>
<tr>
<td>( I_{\text{OUT-PK}} )</td>
<td>Peak output current(3)</td>
<td>( f_{\text{SW}} = 500 \text{ kHz} )</td>
<td>105</td>
<td>A</td>
</tr>
<tr>
<td>( f_{\text{SW}} )</td>
<td>Switching frequency</td>
<td>( C_{\text{BST}} = 0.1 \mu\text{F} ) (min), ( V_{\text{OUT}} = 2.5 \text{ V} ) (max)</td>
<td>1250</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>On-time duty cycle</td>
<td>( f_{\text{SW}} = 1 \text{ MHz} )</td>
<td>85%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Minimum PWM on-time</td>
<td></td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Operating junction temperature</td>
<td></td>
<td>–40</td>
<td>125</td>
</tr>
</tbody>
</table>

(1) Operating at high \( V_{\text{IN}} \) can create excessive AC voltage overshoots on the switch node (\( V_{\text{SW}} \)) during MOSFET switching transients. For reliable operation, the switch node (\( V_{\text{SW}} \)) to ground voltage must remain at or below the Absolute Maximum Ratings.

(2) Measurement made with six 10-µF (TDK C3216X7R1C106KT or equivalent) ceramic capacitors across \( V_{\text{IN}} \) to \( P_{\text{GND}} \) pins.

(3) System conditions as defined in Note 2. Peak output current is applied for \( t_{\text{p}} = 50 \mu\text{s} \).
7 Application Schematic

Figure 1. Application Schematic

Note: The schematic in Figure 1 is a conceptual drawing only. Actual designs may require additional components not shown.
8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Community Resources
The following links connect to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

TI E2E™ Online Community TI’s Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI’s Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.3 Trademarks
NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.5 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.
9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Mechanical Drawing

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.
4. Exposed tie bar features may vary.
9.2 **Recommended PCB Land Pattern**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is designed to be soldered to thermal pads on the board. For more information, see QFN/SON PCB Attachment (SLUA271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9.3 Recommended Stencil Opening

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSD95490Q5MC</td>
<td>ACTIVE</td>
<td>VSON-CLIP</td>
<td>DMC</td>
<td>12</td>
<td>2500</td>
<td>Pb-Free (RoHS Exempt)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-55 to 150</td>
<td>95490MC</td>
<td>Samples</td>
</tr>
<tr>
<td>CSD95490Q5MCT</td>
<td>ACTIVE</td>
<td>VSON-CLIP</td>
<td>DMC</td>
<td>12</td>
<td>250</td>
<td>Pb-Free (RoHS Exempt)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-55 to 150</td>
<td>95490MC</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# TAPE AND REEL INFORMATION

**TAPE DIMENSIONS**

- **K0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **A0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**REEL DIMENSIONS**

- **Reel Diameter**
- **Reel Width (W1)**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width (W1) (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSD95490Q5MC</td>
<td>VSON-CLIP</td>
<td>DMC</td>
<td>12</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>5.3</td>
<td>6.3</td>
<td>1.2</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>CSD95490Q5MCT</td>
<td>VSON-CLIP</td>
<td>DMC</td>
<td>12</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>5.3</td>
<td>6.3</td>
<td>1.2</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSD95490Q5MC</td>
<td>VSON-CLIP</td>
<td>DMC</td>
<td>12</td>
<td>2500</td>
<td>370.0</td>
<td>355.0</td>
<td>55.0</td>
</tr>
<tr>
<td>CSD95490Q5MCT</td>
<td>VSON-CLIP</td>
<td>DMC</td>
<td>12</td>
<td>250</td>
<td>195.0</td>
<td>200.0</td>
<td>45.0</td>
</tr>
</tbody>
</table>
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