• Function, Pinout, and Drive Compatible
  With FCT, F Logic, and AM29823

• Reduced \( V_{OH} \) (Typically = 3.3 V) Version of
  Equivalent FCT Functions

• Edge-Rate Control Circuitry for
  Significantly Improved Noise
  Characteristics

• \( I_{\text{off}} \) Supports Partial-Power-Down Mode
  Operation

• Matched Rise and Fall Times

• Fully Compatible With TTL Input and
  Output Logic Levels

• ESD Protection Exceeds JESD 22
  – 2000-V Human-Body Model (A114-A)
  – 200-V Machine Model (A115-A)
  – 1000-V Charged-Device Model (C101)

• 64-mA Output Sink Current
  32-mA Output Source Current

• High-Speed Parallel Register With
  Positive-Edge-Triggered D-Type Flip-Flops

• Buffered Common Clock-Enable (\( EN \)) and
  Asynchronous-Clear (\( CLR \)) Inputs

• 3-State Outputs

description

This bus-interface register is designed to eliminate the extra packages required to buffer existing registers and
provide extra data width for wider address/data paths or buses carrying parity. The CY74FCT823T is a
9-bit-wide buffered register with clock-enable (\( EN \)) and clear (\( CLR \)) inputs that are ideal for parity bus interfacing
in high-performance microprogrammed systems. It is ideal for use as an output port requiring high \( I_{OL}/I_{OH} \).

This device is designed for high-capacitance load drive capability, while providing low-capacitance bus loading
at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state.

This device is fully specified for partial-power-down applications using \( I_{\text{off}} \). The \( I_{\text{off}} \) circuitry disables the outputs,
preventing damaging current backflow through the device when it is powered down.
ORDERING INFORMATION

<table>
<thead>
<tr>
<th>TA</th>
<th>PACKAGE†</th>
<th>SPEED (ns)</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40°C to 85°C</td>
<td>QSOP – Q</td>
<td>Tape and reel</td>
<td>6</td>
<td>CY74FCT823CTQCT</td>
</tr>
<tr>
<td></td>
<td>SOIC – SO</td>
<td>Tube</td>
<td>6</td>
<td>CY74FCT823CTSOC</td>
</tr>
<tr>
<td></td>
<td>Tape and reel</td>
<td>6</td>
<td>CY74FCT823CTSOCT</td>
<td>FCT823C</td>
</tr>
<tr>
<td></td>
<td>DIP – P</td>
<td>Tube</td>
<td>7.5</td>
<td>CY74FCT823BTPCR</td>
</tr>
<tr>
<td></td>
<td>DIP – P</td>
<td>Tube</td>
<td>10</td>
<td>CY74FCT823ATPC</td>
</tr>
<tr>
<td></td>
<td>QSOP – Q</td>
<td>Tape and reel</td>
<td>10</td>
<td>CY74FCT823ATQCT</td>
</tr>
<tr>
<td></td>
<td>SOIC – SO</td>
<td>Tube</td>
<td>10</td>
<td>CY74FCT823ATSOC</td>
</tr>
<tr>
<td></td>
<td>Tape and reel</td>
<td>10</td>
<td>CY74FCT823ATSOCT</td>
<td>FCT823A</td>
</tr>
</tbody>
</table>

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PIN DESCRIPTION

<table>
<thead>
<tr>
<th>NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>I</td>
<td>D flip-flop data inputs</td>
</tr>
<tr>
<td>CLR</td>
<td>I</td>
<td>When CLR is low and OE is low, Q outputs are low. When CLR is high, data can be entered into the register.</td>
</tr>
<tr>
<td>CP</td>
<td>O</td>
<td>Clock pulse for the register. Enters data into the register on the low-to-high clock transition.</td>
</tr>
<tr>
<td>Y</td>
<td>O</td>
<td>Register 3-state outputs</td>
</tr>
<tr>
<td>EN</td>
<td>I</td>
<td>Clock enable. When EN is low, data on the D input is transferred to the Q output on the low-to-high clock transition. When EN is high, the Q outputs do not change state, regardless of the data or clock input transitions.</td>
</tr>
<tr>
<td>OE</td>
<td>I</td>
<td>Output control. When OE is high, the Y outputs are in the high-impedance state. When OE is low, true register data is present at the Y outputs.</td>
</tr>
</tbody>
</table>

FUNCTION TABLE

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>INTERNAL OUTPUTS</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OE</td>
<td>CLR</td>
<td>EN</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
</tbody>
</table>

H = High logic level, L = Low logic level, X = Don’t care, NC = No change, ↑ = Low-to-high transition, Z = High-impedance state
logic diagram (positive logic)

To Eight Other Channels

absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential .......................................................... –0.5 V to 7 V
DC input voltage range ...................................................................................... –0.5 V to 7 V
DC output voltage range .................................................................................... –0.5 V to 7 V
DC output current (maximum sink current/pin) ...................................................... 120 mA
Package thermal impedance, θJA (see Note 1): P package ......................................... 67°C/W
(see Note 2): Q package .................................................................................. 61°C/W
(see Note 2): SO package ............................................................................... 46°C/W
Ambient temperature range with power applied, TA ........................................ −65°C to 135°C
Storage temperature range, Tstg ........................................................................ −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The package thermal impedance is calculated in accordance with JESD 51-3.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply voltage</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
</tr>
<tr>
<td>VIH</td>
<td>High-level input voltage</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Low-level input voltage</td>
<td></td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td>IOH</td>
<td>High-level output current</td>
<td></td>
<td></td>
<td>–32</td>
</tr>
<tr>
<td>IOL</td>
<td>Low-level output current</td>
<td></td>
<td></td>
<td>64</td>
</tr>
<tr>
<td>TA</td>
<td>Operating free-air temperature</td>
<td></td>
<td></td>
<td>–40</td>
</tr>
</tbody>
</table>

NOTE 3: All unused inputs of the device must be held at VCC or GND to ensure proper device operation.
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP†</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I&lt;sub&gt;V&lt;/sub&gt;K</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 4.75 V, I&lt;sub&gt;IN&lt;/sub&gt; = –18 mA</td>
<td>–0.7</td>
<td>–1.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 4.75 V</td>
<td>2</td>
<td>3.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 4.75 V, I&lt;sub&gt;OL&lt;/sub&gt; = 64 mA</td>
<td>0.3</td>
<td>0.55</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;hys&lt;/sub&gt;</td>
<td>All inputs</td>
<td>0.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;I&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.25 V, V&lt;sub&gt;IN&lt;/sub&gt; = V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>5</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.25 V, V&lt;sub&gt;IN&lt;/sub&gt; = 2.7 V</td>
<td>±1</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.25 V, V&lt;sub&gt;IN&lt;/sub&gt; = 0.5 V</td>
<td>±1</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;OZH&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.25 V, V&lt;sub&gt;OUT&lt;/sub&gt; = 2.7 V</td>
<td>10</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;OZL&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.25 V, V&lt;sub&gt;OUT&lt;/sub&gt; = 0.5 V</td>
<td>–10</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;OS&lt;/sub&gt;‡</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.25 V, V&lt;sub&gt;OUT&lt;/sub&gt; = 0 V</td>
<td>–60</td>
<td>–120</td>
<td>–225</td>
<td>mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;off&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5 V, V&lt;sub&gt;IN&lt;/sub&gt; = 3.4 V, f&lt;sub&gt;1&lt;/sub&gt; = 0, Outputs open</td>
<td>–1</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.25 V, V&lt;sub&gt;IN&lt;/sub&gt; ≤ 0.2 V, V&lt;sub&gt;IN&lt;/sub&gt; ≥ V&lt;sub&gt;CC&lt;/sub&gt; – 0.2 V</td>
<td>0.1</td>
<td>0.2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>∆I&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.25 V, V&lt;sub&gt;IN&lt;/sub&gt; = 3.4 V or GND</td>
<td>0.5</td>
<td>2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;CCD&lt;/sub&gt;¶</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.25 V, One bit switching at 50% duty cycle, Outputs open,</td>
<td>0.06</td>
<td>0.12</td>
<td>mA/</td>
<td>MHz</td>
</tr>
</tbody>
</table>

| I<sub>C</sub># | V<sub>CC</sub> = 5.25 V, Outputs open, O<sub>E</sub> = EN = GND | 0.7  | 1.4  | mA  |
|              | at f<sub>1</sub> = 5 MHz at 50% duty cycle | V<sub>IN</sub> ≤ 0.2 V or V<sub>IN</sub> ≥ V<sub>CC</sub> – 0.2 V |      |      |
|              | V<sub>IN</sub> = 3.4 V or GND | 1.2  | 3.4  | mA  |
|              | Eight bits switching at f<sub>1</sub> = 2.5 MHz at 50% duty cycle | 1.6  | 3.2  | mA  |
|              | V<sub>IN</sub> ≤ 0.2 V or V<sub>IN</sub> ≥ V<sub>CC</sub> – 0.2 V | 3.9  | 12.2 | mA  |
|              | V<sub>IN</sub> = 3.4 V or GND | 2.5  | 3.4  | mA  |

| C<sub>1</sub> | 5  | 10  | pF   |
| C<sub>0</sub> | 9  | 12  | pF   |

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.
‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
§ Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND
¶ This parameter is derived for use in total power-supply calculations.
# I<sub>C</sub> = I<sub>CC</sub> + ∆I<sub>CC</sub> × D<sub>H</sub> × N<sub>T</sub> + I<sub>CCD</sub> (f<sup>0</sup>/2 + f<sub>1</sub> × N<sub>1</sub>)

Where:
- I<sub>C</sub> = Total supply current
- I<sub>CC</sub> = Power-supply current with CMOS input levels
- ∆I<sub>CC</sub> = Power-supply current for a TTL high input (V<sub>IN</sub> = 3.4 V)
- D<sub>H</sub> = Duty cycle for TTL inputs high
- N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>
- I<sub>CCD</sub> = Dynamic current caused by an input transition pair (HLH or LHL)
- f<sup>0</sup> = Clock frequency for registered devices, otherwise zero
- f<sub>1</sub> = Input signal frequency
- N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I<sub>CC</sub> formula.
timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST LOAD</th>
<th>CY74FCT823AT</th>
<th>CY74FCT823BT</th>
<th>CY74FCT823CT</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_w$</td>
<td>Pulse duration</td>
<td>CP</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CLR low</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>$t_{su}$</td>
<td>Setup time, before CP↑</td>
<td>Data</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EN</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>$t_h$</td>
<td>Hold time, after CP↑</td>
<td>Data</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>2</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EN</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>$t_{rec}$</td>
<td>Recovery time</td>
<td>CLR before CP↑</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>6</td>
<td>6</td>
</tr>
</tbody>
</table>

switching characteristics over operating free-air temperature range (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST LOAD</th>
<th>CY74FCT823AT</th>
<th>CY74FCT823BT</th>
<th>CY74FCT823CT</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>CP</td>
<td>Y</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>10</td>
<td>7.5</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>CP</td>
<td>Y</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>10</td>
<td>7.5</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>CP</td>
<td>Y</td>
<td>$C_L = 300 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>20</td>
<td>15</td>
<td>12.5</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHH}$</td>
<td>CP</td>
<td>Y</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>20</td>
<td>15</td>
<td>12.5</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>CLR</td>
<td>Y</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>14</td>
<td>9</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZH}$</td>
<td>OE</td>
<td>Y</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>12</td>
<td>8</td>
<td>7</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZH}$</td>
<td>OE</td>
<td>Y</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>12</td>
<td>8</td>
<td>7</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZH}$</td>
<td>OE</td>
<td>Y</td>
<td>$C_L = 300 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>23</td>
<td>15</td>
<td>12.5</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>OE</td>
<td>Y</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>23</td>
<td>15</td>
<td>12.5</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>OE</td>
<td>Y</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>7</td>
<td>6.5</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>OE</td>
<td>Y</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>7</td>
<td>6.5</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>OE</td>
<td>Y</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>8</td>
<td>7.5</td>
<td>6.5</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>OE</td>
<td>Y</td>
<td>$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$</td>
<td>8</td>
<td>7.5</td>
<td>6.5</td>
<td>ns</td>
</tr>
</tbody>
</table>
PARAMETER MEASUREMENT INFORMATION

From Output Under Test

From Output Under Test

<table>
<thead>
<tr>
<th>TEST</th>
<th>S1</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPLH / tPHL</td>
<td>Open</td>
</tr>
<tr>
<td>tPLZ / tPZL</td>
<td>7 V</td>
</tr>
<tr>
<td>tPHZ / tPZH</td>
<td>Open</td>
</tr>
</tbody>
</table>

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE OUTPUTS

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY74FCT823ATQCT</td>
<td>ACTIVE</td>
<td>SSOP</td>
<td>DBQ</td>
<td>24</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>FCT823A</td>
<td></td>
</tr>
<tr>
<td>CY74FCT823ATSOC</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>24</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>FCT823A</td>
<td></td>
</tr>
<tr>
<td>CY74FCT823CTSOC</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>24</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>FCT823C</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBsolete**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.**: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish**: Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY74FCT823ATQCT</td>
<td>SSOP</td>
<td>DBQ</td>
<td>24</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>9.0</td>
<td>2.1</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

**[Diagram of TAPE DIMENSIONS](#)**

**[Diagram of REEL DIMENSIONS](#)**

**[Diagram of QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE](#)**

**Definitions:***

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers
### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY74FCT823ATQCT</td>
<td>SSOP</td>
<td>DBQ</td>
<td>24</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>38.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion nor exceed 0.006 (0.15) per side.
D. Falls within JEDEC MO-137 variation AE.
**DBQ (R-PDSO-G24) PLASTIC SMALL OUTLINE PACKAGE**

**Example Board Layout**

**Stencil Openings**  
Based on a stencil thickness of .127mm (.005inch).

**NOTES:**
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
NOTES:  
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994. 
B. This drawing is subject to change without notice. 
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15). 
D. Falls within JEDEC MS-013 variation AD.
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