DP83825I Low Power 10/100 Mbps Ethernet Physical Layer Transceiver

1 Features

- Smallest 10/100 Mbps PHY : QFN 3x3 mm2
- MAC Interface : RMII (Master and Slave Mode)
- Cable Reach > 150 meters
- Voltage Mode Line Driver
- Very Low Power Consumption < 135 mW
- Smallest System Solution : Integrated MDI and MAC Termination Resistors
- Programmable Energy Saving Modes
  - Active Sleep with Very Low Power Consumption < 40 mW
  - Deep Power Down Mode < 9 mW
  - Energy Efficient Ethernet (EEE) IEEE 802.3az
  - Wake-on-LAN (WoL)
- Single 3.3V power supply
- I/O Voltages: 1.8V, 3.3V
- Repeater Mode : RMII Back to Back Mode in unmanaged mode
- MDC/MDIO Interface for configuration and status
- Fast Link Drop Modes
- Cable Diagnostics
- Hardware Interrupt pin
- +/-5 KV HBM ESD Protection
- Operating Temperature Range: –40°C to 85°C
- Compliant to IEEE 802.3 10BASE-Te, 100BASE-TX Specification

2 Applications

- Building Automation
  - IP Cameras
  - HMI
- Consumer Electronics
  - STB, OTT, IPTV
  - Game Consoles
  - Smart TVs
- Printers
- Electronic Point of Sale
- Factory Automation

3 Description

The DP83825I is the smallest form factor, lowest power Ethernet Physical Layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX Ethernet protocols. The DP83825I interfaces directly to twisted pair media via an external transformer. It interfaces to the MAC layer through Reduced MII (RMII) both in Master and Slave mode. The 50 MHz clock in RMII Master mode is synchronized to MDI derived clock to reduce the jitter in the system.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DP83825I	QFN (24) RMQ	3 mm x 3 mm, 0.4 mm pitch

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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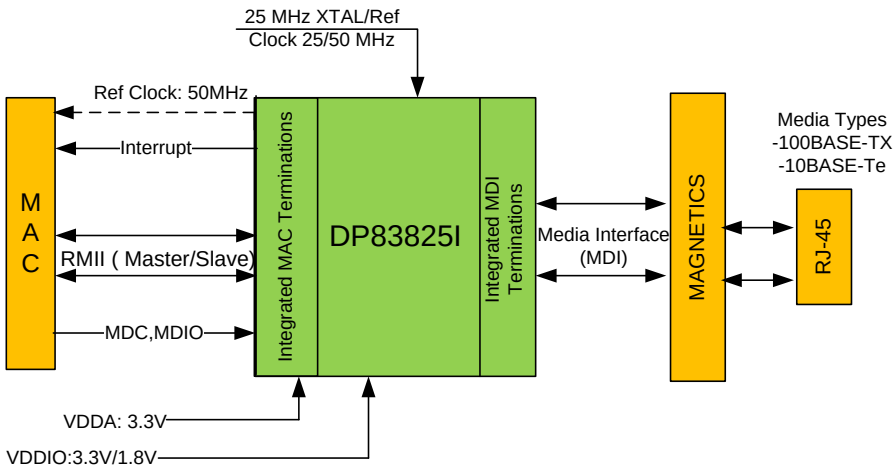
DP83825I Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2018	*	Initial Release

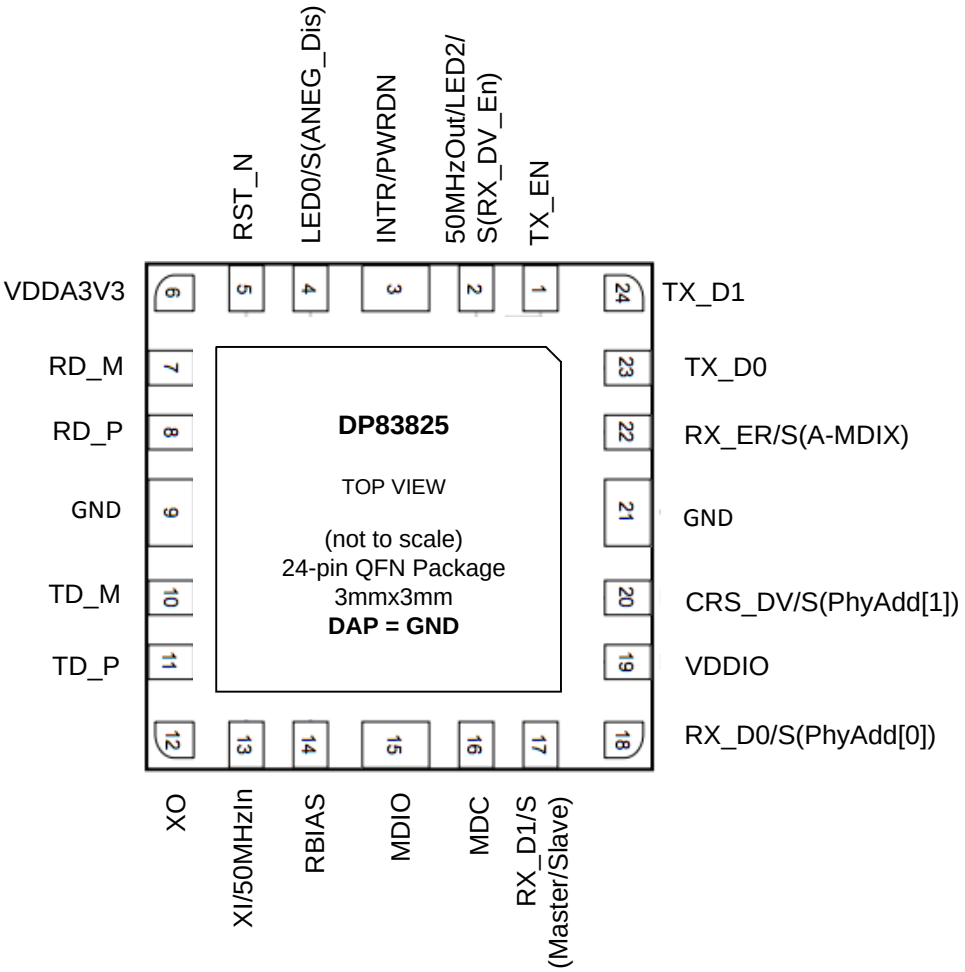
5 Description (continued)

The DP83825I offers integrated cable diagnostic tools, built-in self-test and loopback capabilities for ease of use. It supports multiple industrial buses with its fast link-down timing.

The DP83825I also supports Energy Efficient Ethernet, Wake on LAN and MAC isolation to further lower the system power consumption. DP83825I can operate in unmanaged repeater mode. In this mode, DP83825I works as a repeater without register configuration.

6 Pin Configuration and Functions

DP83825
24 Pin QFN RMQ Package
Top View



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DP83825I Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO		
TX_EN	1	Reset: I, PD ;Active: I, PD	RMII Transmit Enable: TX_EN is active high signal and is presented on the rising edge of the TX_CLK. TX_EN indicates the presence of valid data inputs on TX_D [1:0].
50MHzOut/LED2	2	Reset: I, PD ;Active: O	RMII Master Mode: 50 MHz Clock Out(default). RMII Slave Mode: LED_2(default). This pin can be configured as GPIO using register configuration.
		Strap : RX_DV_En	Strap : RX_DV_En : This pin has strap to configure pin 20 as RX_DV for repeater function 0 : CRS_DV (default) 1 : RX_DV
INTR/PWRDN	3	Reset: I, PU; Active: I, PU	Interrupt / Power Down(default): The default function of this pin is power down. Register access is required to configure this pin as an interrupt. In power down function, an active low signal on this pin places the device in power down mode. When this pin is configured as an interrupt pin, this pin is asserted low when an interrupt condition occurs. The pin has an open-drain output with a weak internal pullup (9.5K). Some applications may require an external PU resistor.
LED0	4	Reset: I, PD ; Active: O	LED0 : Activity Indication LED indicates transmit and receive activity in addition to the status of the Link. The LED is ON when Link is good. The LED blinks when the transmitter or receiver is active. This pin can also act as GPIO thru register configuration. This pin is at 3V3 always and not linked to voltage supplied to VIO pin. This is to avoid external components when operating PHY at VDDIO 1V8
		Strap : ANEG_Dis	Strap : ANEG_Dis: Auto Neg This pin has strap function to disable Auto Negotiation. 0 A-Neg enabled(default) 1: A-Neg Disable
RST_N	5	Reset: I, PU Active: I, PU	RST_N: This pin is an active low reset input. Asserting this pin low for at least 1μs will force a reset process to occur. Initiation of reset causes strap pins to be re-scanned and resets all the internal registers of the PHY to default value.
VDDA3V3	6	Power	Input Analog Supply: 3V3. For decoupling capacitor requirements, refer to Application section of datasheet.
RD_M	7	A	Differential Receive Input (PMD): These differential inputs are automatically configured to accept either 10BASE-Te, 100BASE-TX specific signaling mode
RD_P	8	A	
GND	9	GND	Ground: Connect to Ground
TD_M	10	A	Differential Transmit Output (PMD): These differential outputs are configured to either 10BASE-Te, 100BASE-TX signaling mode based on configuration chosen for PHY.
TD_P	11	A	
XO	12	A	Crystal Output: Reference Clock output. XO pin is used for crystal only. This pin should be left floating when a CMOS-level oscillator is connected to XI.
XI/50MHzIn	13	A	Crystal / Oscillator Input Clock RMII Master mode: 25-MHz ±50 ppm-tolerance crystal or oscillator clock RMII Slave mode: 50-MHz ±50 ppm-tolerance CMOS-level oscillator clock
RBIAS	14	A	RBIAS value 6.49K Ohm 1% connected to ground
MDIO	15	Reset: I, PU-10K Active: IO, PU-10K	Management Data I/O: Bi-directional management data signal that may be source by the management station or the PHY. This pin has internal pull of 10K. External pull up can be added if needed
MDC	16	Reset: I, PD Active: I, PD	Management Data Clock: Synchronous clock to the MDIO serial management input/output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 25-MHz. There is no minimum clock rate.
RX_D1	17	Reset: I, PD Active: O	RMII Receive Data: Symbols received on the cable are decoded and presented on these pins synchronous to reference clock. They contain valid data when RX_DV is asserted.
		Strap: Master/Slave	Strap: Master/Slave : This pin has strap to configure RMII Master or Slave mode 0 : RMII Master (default) 1 : RMII Slave

DP83825I Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO		
RX_D0	18	Reset: I, PD Active: O	RMII Receive Data: Symbols received on the cable are decoded and presented on these pins synchronous to reference clock. They contain valid data when RX_DV is asserted.
		Strap: PhyAdd[0]	Strap: PhyAdd[0] : This pin has strap to configure PHY Address [0] 0 : PHY Address bit 0 as 0 (default) 1 : PHY Address bit 0 as 1 PHY Address strap is 2 bit strap on pin 20 and 18 and shall be read as [1:0] respectively as 00 01 10 11. Default PHY Address is 00
VDDIO	19	Power	I/O Supply : 3.3V/1.8V. For decoupling capacitor requirements, refer to Application section of datasheet.
CRS_DV	20	Reset: I, PD Active: O	Carrier Sense / Receive Data Valid: This pin combines the RMII Carrier and Receive Data Valid indications.
		Strap: PhyAdd[1]	Strap: PhyAdd[1] : This pin has strap to configure PHY Address [1] 0 : PHY Address bit 1 as 0 (default) 1 : PHY Address bit 1 as 1 PHY Address strap is 2 bit strap on pin 20 and 18 and shall be read as [1:0] respectively as 00, 01, 10 or 11. Default PHY Address is 00
GND	21	GND	Ground pin
RX_ER	22	Reset: I, PD Active: O	RMII Receive Error: This pin indicates an error symbol has been detected within a received packet in RMII mode. RX_ER is asserted high synchronously to the rising edge of the reference clock. This pin is not required to be used by the MAC in RMII because the PHY will automatically corrupting data on a receive error.
		Strap :A-MDIX	Strap :A-MDIX : This pin has strap to configure Auto MDIX mode 0 : A-MDIX Enabled (default) 1 : A-MDIX disabled
TX_D0	23	Reset: I, PD Active: I, PD	RMII Transmit Data: TX_D[1:0] received from the MAC and shall be synchronous to the rising edge of the reference clock.
TX_D1	24	Reset: I, PD Active: I, PD	

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
Analog supply voltage	AVDD3V3	–0.3	4	V
IO supply voltage	VDDIO3V3	–0.3	4	V
	VDDIO1V8	–0.3	2.1	V
Junction Temperature	Tj		105	°C
Storage Temperature	Tstg	–65	150	°C

7.2 ESD Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (HBM)	All Pins (except MDI)	±2		kV
	MDI (Media Dependent Interface) pins	±5		kV
ESD (CDM)	All Pins	TBD		V

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Analog supply voltage	AVDD3V3	3	3.3	3.6	V
IO supply voltage	VDDIO3V3	3	3.3	3.6	V
	VDDIO1V8	1.62	1.8	1.98	V
Operating Free Air Temperature (DP83825I)	Ta	–40	25	85	C

7.4 Thermal Information

THERMAL METRIC(1)			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	28.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.3	°C/W
Y_{JT}	Junction-to-top characterization parameter	28.5	°C/W
Y_{JB}	Junction-to-board characterization parameter	14.9	°C/W

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7.5 Electrical Characteristics

over operating free-air temperature range with VDDA = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IEEE Tx CONFORMANCE (100BaseTx)						
	Differential Output Voltage	100 Base Tx idle transmission		1000		mV
IEEE Tx CONFORMANCE (10BaseTe)						
	Differential Voltage	10BaseTe data transmission		1.75		V
Crystal oscillator						
	Load Capacitance			15	30	pF
IO						
3V3	3V3 Vih		1.7			V
	Vil				0.8	V
	Voh 3V3		2.4			V
	Vol 3V3				0.8	V
1V8	Vih		1.3			V
	Vil				0.5	V
	Voh 1V8		1.3			V
	Vol 1V8				0.4	V
	Cin (Input Capaticance)				5	pF
	R Pull Down		8	10	13	Kohms
	R Pull UP		8	10	13	Kohms
	LED_0 drive strength				8	mAmp
	GPIO Driver Strength				8	mAmp
	XI input osc clock pk-pk VDDIO 1V8		1.62	1.8	1.98	V
	XI input osc clock pk-pk VDDIO 3V3		3	3.3	3.6	V
	XI input osc clock common mode VDDIO 3V3			1.65		V
	XI input osc clock common mode VDDIO 1V8			0.9		V

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7.6 Timing Requirements

PARAMETER		MIN	NOM	MAX	UNIT
POWER-UP TIMING					
T2	POR release time / Powerup to SMI ready: Post power-up stabilization time prior to MDC preamble for register access			50	ms
T3	Powerup to FLP		1500		ms
RESET TIMING					
T2	Reset to SMI ready: Post reset stabilization time prior to MDC preamble for register access			2	ms
T1	RESET PULSE Width: Miminum Reset pulse width to be able to reset (w/o debouncing caps)	25			us
T3	Reset to FLP		1500		ms
	Reset to 100M signaling (strapped mode)		0.5		ms
	Reset to RMII Master clock		0.2		ms
RMII Master TIMING (100M)					
	RMII Master Clock Period		20		ns
	RMII Master Clock Duty Cycle	35		65	%
RMII TIMING (100M)					
T1	Input Reference Clock Period		20		ns
	Reference Clock Duty Cycle	35		65	%
T2	TX_D[1:0], TX_ER, TX_EN Setup to XI Clock rising	4			ns
T3	TX_D[1:0], TX_ER, TX_EN Hold from XI Clock rising	2			ns
T4	RX_D[1:0], RX_ER, CRS_DV Delay from XI Clock rising	4		14	ns
SMI TIMING					
T1	MDC to MDIO (Output) Delay Time	0		10	ns
T2	MDIO (Input) to MDC Setup Time	10			ns
T3	MDIO (Input) to MDC Hold Time	10			ns
T4	MDC Frequency		2.5	20	MHz
25MHz INPUT CLOCK tolerance					
	Frequency Tolerance	-100		100	ppm
	Rise / Fall Time			5	ns
	Jitter Tolerance (Accumulated over 100,000 cycles)			1.75	ns
	Duty Cycle	40		60	%

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7.7 Timing Diagrams

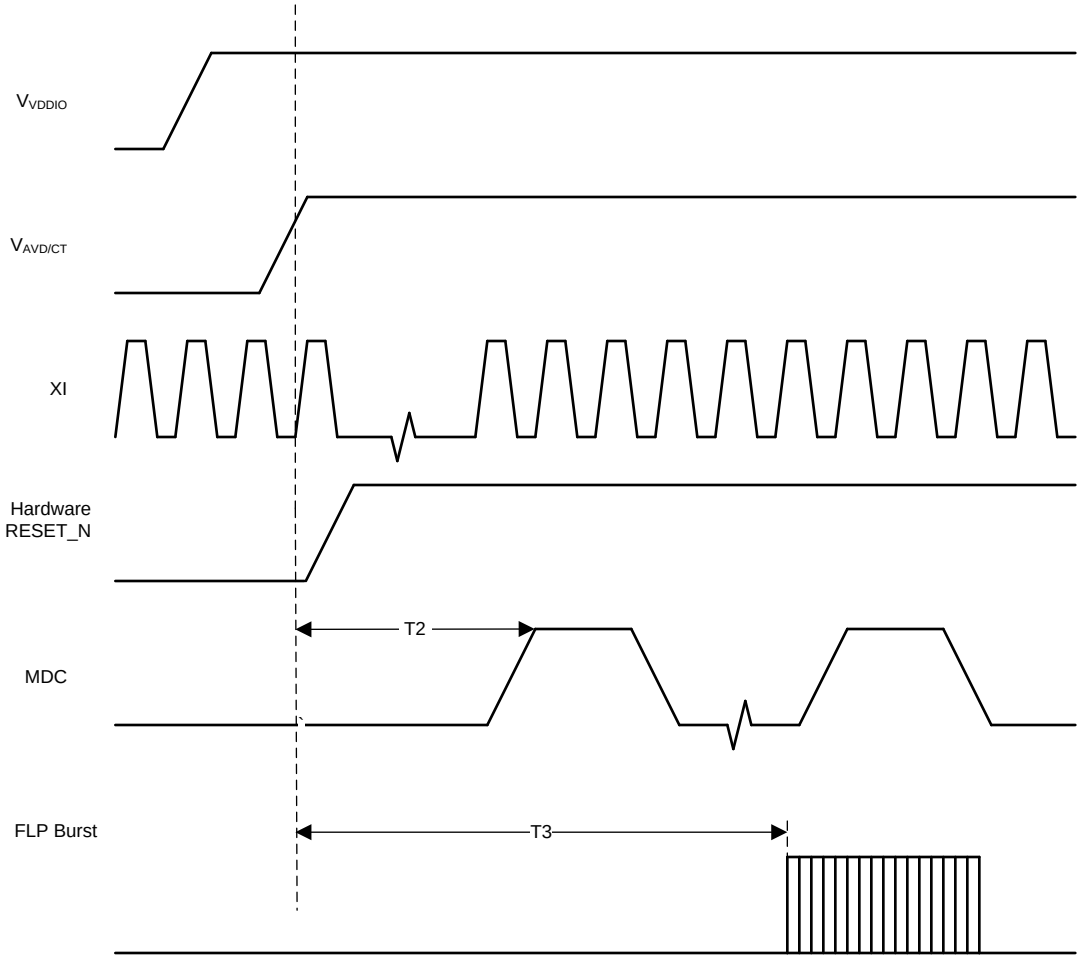

Figure 1. Power-Up Timing

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Timing Diagrams (continued)

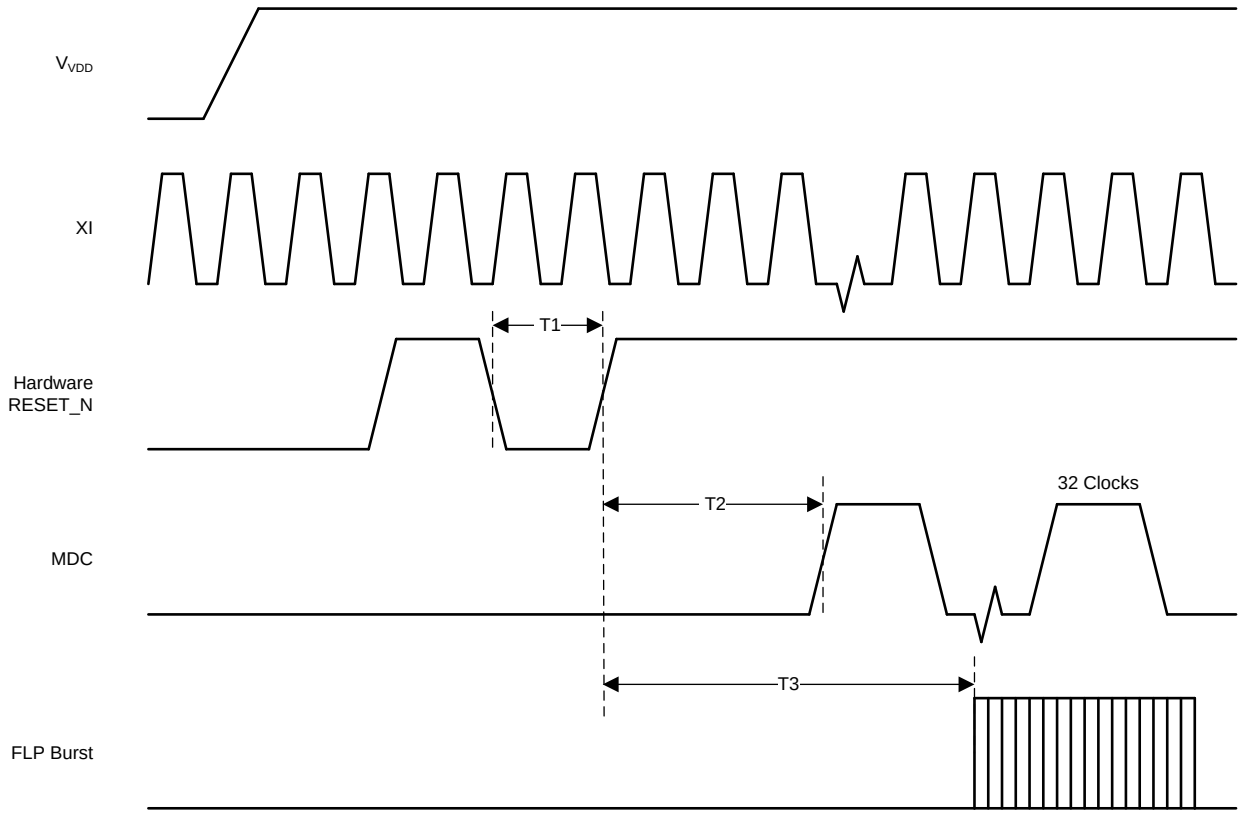

Figure 2. Reset Timing

Timing Diagrams (continued)

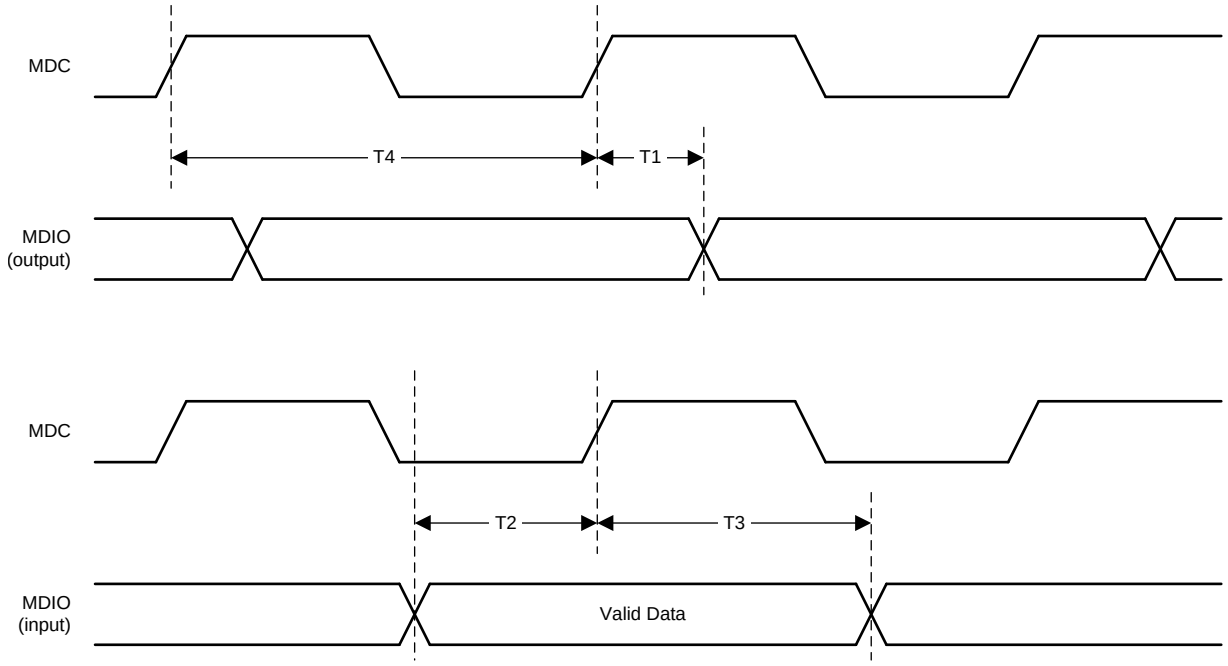

Figure 3. Serial Management Timing

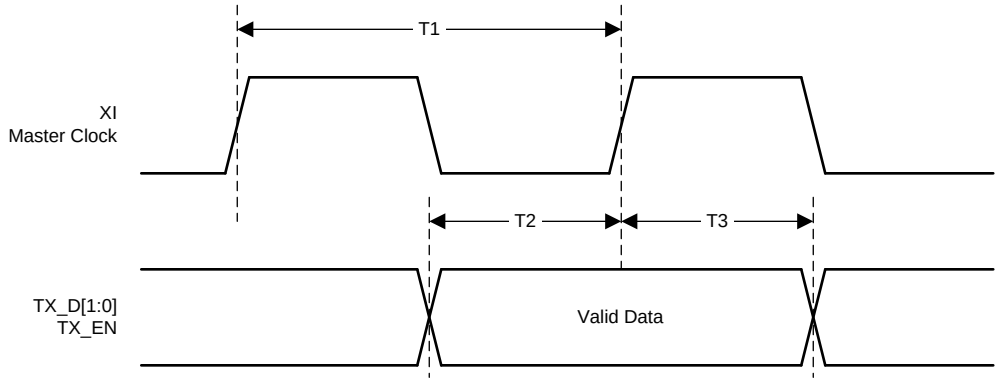

Figure 4. RMII Transmit Timing

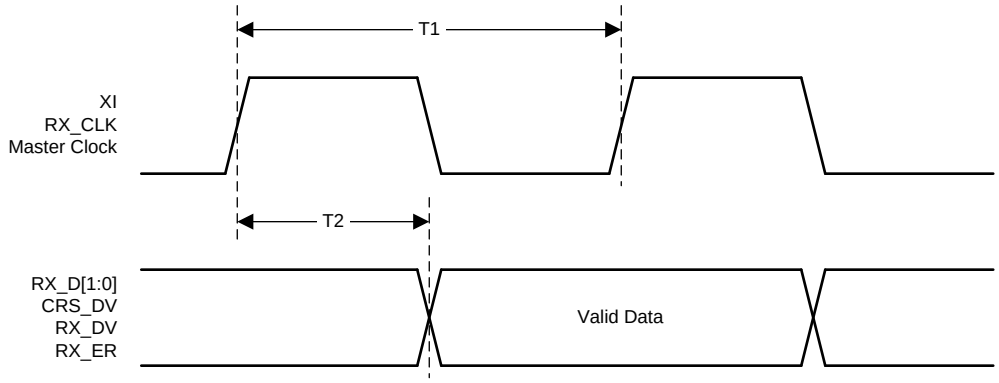

Figure 5. RMII Receive Timing

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8 Detailed Description

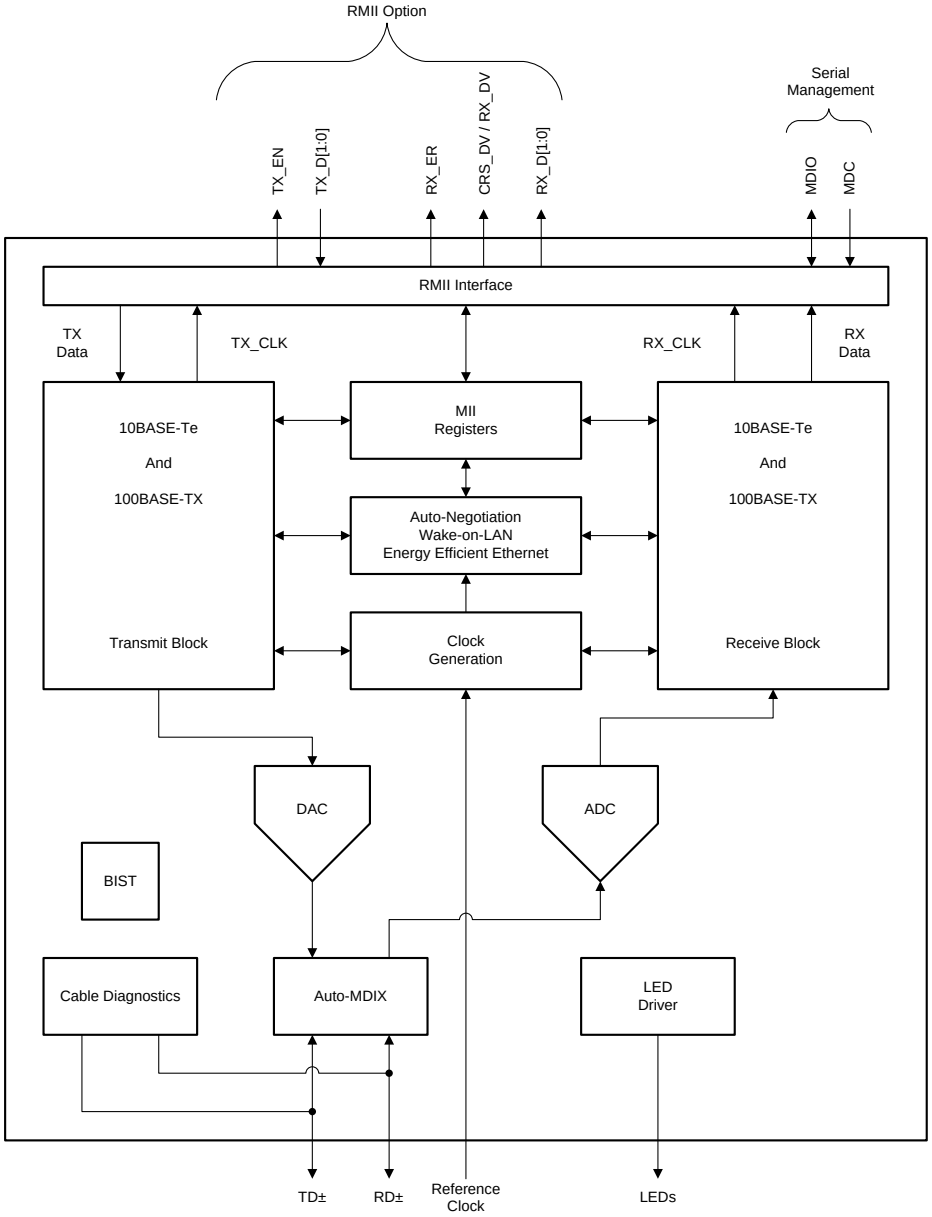
8.1 Overview

The DP83825I is a fully featured single-port Physical Layer transceiver compliant to IEEE802.3 10BASE-Te and 100BASE-TX standards. The device supports the standard Reduced Media Independent Interface (RMII) for direct connection to Media Access Controller (MAC).

The device is designed for single 3.3 V power supply with integrated LDO to provide voltage rails needed for internal blocks. The device allows I/O voltage interfaces for 3.3 V or 1.8 V. Automatic supply configuration within the DP83825I allows for any combination of VDDIO supply and AVDD supply without the need for additional configuration settings.

The DP83825I uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over CAT5e twisted-pair cable greater than 150 meters.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Auto-Negotiation (Speed / Duplex Selection)

Auto-Negotiation provides a mechanism for exchanging configuration information between the two ends of a link segment. This mechanism is implemented by exchanging Fast Link Pulses (FLP). FLPs are burst pulses that provide the information used to communicate the abilities between two devices at each end of a link segment. The DP83825I supports 100BASE-TX and 10BASE-Te modes of operation for Auto-Negotiation. Auto-Negotiation ensures that the highest common speed is selected based on the advertised abilities of the Link Partner and the local device. Auto-Negotiation can be enabled or disabled in hardware, using the bootstrap, or by register configuration, using bit[12] in the Basic Mode Control Register (BMCR, address 0x0000). For further details regarding Auto-Negotiation, refer to Clause 28 of the IEEE 802.3 specification.

8.3.2 Auto-MDIX Resolution

The DP83825I can determine if a “straight” or “crossover” cable is used to connect to the link partner. It can automatically re-assign channel A and B to establish link with the link partner. Auto-MDIX resolution precedes the actual Auto-Negotiation process that involves exchange of FLPs to advertise capabilities. Automatic MDI/MDIX is described in IEEE 802.3 Clause 40, section 40.8.2. It is not a required implementation for 10BASE-Te and 100BASE-TX. Auto-MDIX can also be used when operating the PHY in Forced modes.

Auto-MDIX can be enabled or disabled in hardware, using the hardware bootstrap, or by register configuration, using bit[15] of the PHY Control Register (PHYCR, address 0x0019). When Auto-MDIX is disabled, the PMA is forced to either MDI (“straight”) or MDIX (“crossover”). Manual configuration of MDI or MDIX can also be accomplished using register configuration, using bit[14] of the PHYCR. In Force Mode, Robust Auto Crossover, using bit[5] of Register 0x0009.shall be enabled.

8.3.3 Energy Efficient Ethernet

8.3.3.1 EEE Overview

Energy Efficient Ethernet (EEE), defined by IEEE 802.3az, is a capability integrated into Layer 1 (Physical Layer) and Layer 2 (Data Link Layer) to operate in Low Power Idle (LPI) mode. In LPI mode, power is saved during periods of low packet utilization. EEE defines the protocol to enter and exit LPI mode without dropping the link or corrupting packets.

The DP83825I EEE supports 100 Mbps and 10 Mbps speeds. In 10BASE-Te operation, EEE operates with a reduced transmit amplitude that is fully interoperable with a 10BASE-T PHY.

8.3.3.2 EEE Negotiation

EEE is advertised during Auto-Negotiation. Auto-Negotiation is performed at power up, on management command, after link failure, or due to user intervention. EEE is supported if and only if both link partners advertise EEE capabilities. If EEE is not supported, all EEE functions are disabled and the MAC should not assert LPI. To advertise EEE capabilities, the PHY needs to exchange an additional formatted next page and unformatted next page in sequence.

EEE Negotiation can be activated using Register Access. The DP83825I offers two different ways of accessing EEE control registers within the PHY register set. IEEE 802.3az defines MMD3 and MMD7 as the locations for EEE control and status registers. The MMD3 and MMD7 registers 0x1014, 0x1001, 0x1016, 0x203C, 0x203D contain all the required controls and status indications for operating EEE. The Energy Efficient Ethernet Configuration Register #3 (EEECFG3, address 0x04D1) contains controls for EEE configuration bypass.

8.3.4 Wake-on-LAN Packet Detection

Wake-on-LAN provides a mechanism to detect specific frames and notify the connected controller through either register status change, GPIO indication or an interrupt flag. The WoL feature within the DP83825I allows for connected devices residing above the Physical Layer to remain in a low power state until frames with the qualifying credentials are detected. Supported WoL frame types include: Magic Packet and Magic Packet with Secure-ON Match. When a qualifying WoL frame is received, the DP83825I WoL logic circuit is able to generate a user defined event (either pulses or level change) through any of the GPIO pins or a status interrupt flag to inform a connected controller that a wake event has occurred. Additionally, the DP83825I includes a CRC Gate to prevent invalid packets from triggering a wake-up event.

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Feature Description (continued)

The Wake-on-LAN feature set includes:

- Identification of WoL frames in all supported speeds (100BASE-TX and 10BASE-Te).
- Wakeup interrupt generation upon reception of a WoL frame.
- CRC error checking of WoL frames to prevent interrupt generation from invalid frames.
- Magic Packets with Secure-ON password.

8.3.4.1 Magic Packet Structure

When configured for Magic Packet detection, the DP83825I scans all incoming frames addressed to the node for a specific data sequence. This sequence identifies the frame as a Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which may be the receiving station's IEEE address or a BROADCAST ADDRESS), and CRC.

The specific Magic Packet sequence consists of 16 duplications of the MAC address of this node, with no breaks or interruptions, followed by Secure-ON password if security is enabled. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6-bytes of 0xFF.

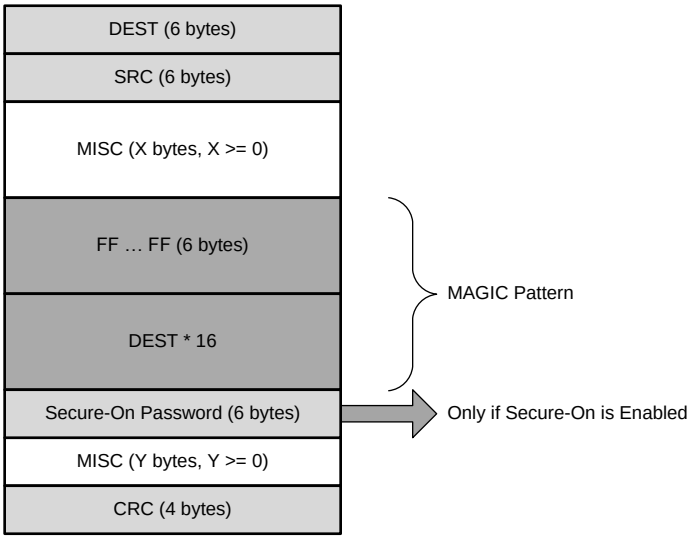

Figure 6. Magic Packet Structure

8.3.4.2 Magic Packet Example

The following is an example Magic Packet for a Destination Address of 11h 22h 33h 44h 55h 66h and a secure-on password 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh:

```
DESTINATION SOURCE MISC FF FF FF FF FF FF
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
11 22 33 44 55 66 2A 2B 2C 2D 2E 2F MISC CRC
```

8.3.4.3 Wake-on-LAN Configuration and Status

Wake-on-LAN functionality is configured through the Receive Configuration Register (RXFCFG, address 0x04A0). Wake-on-LAN status is reported in the Recieve Status Register (RXFS, address 0x04A1). Wake-on-LAN interrupt flag configuration and status is located in the MII Interrupt Status Register #2 (MISR2, address 0x0013).

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Feature Description (continued)

8.3.5 RMII Repeater Mode

The DP83825I provides option to enable repeater mode functionality to extend the cable reach. Two DP83825 can be connected in back 2 back mode without need of any external configuration. It provides a Hardware Strap to configure the CRS_DV pin of RMII interface to RX_DV pin for back to back operation. See below for RMII pin connection to enable DP83825I Repeater mode

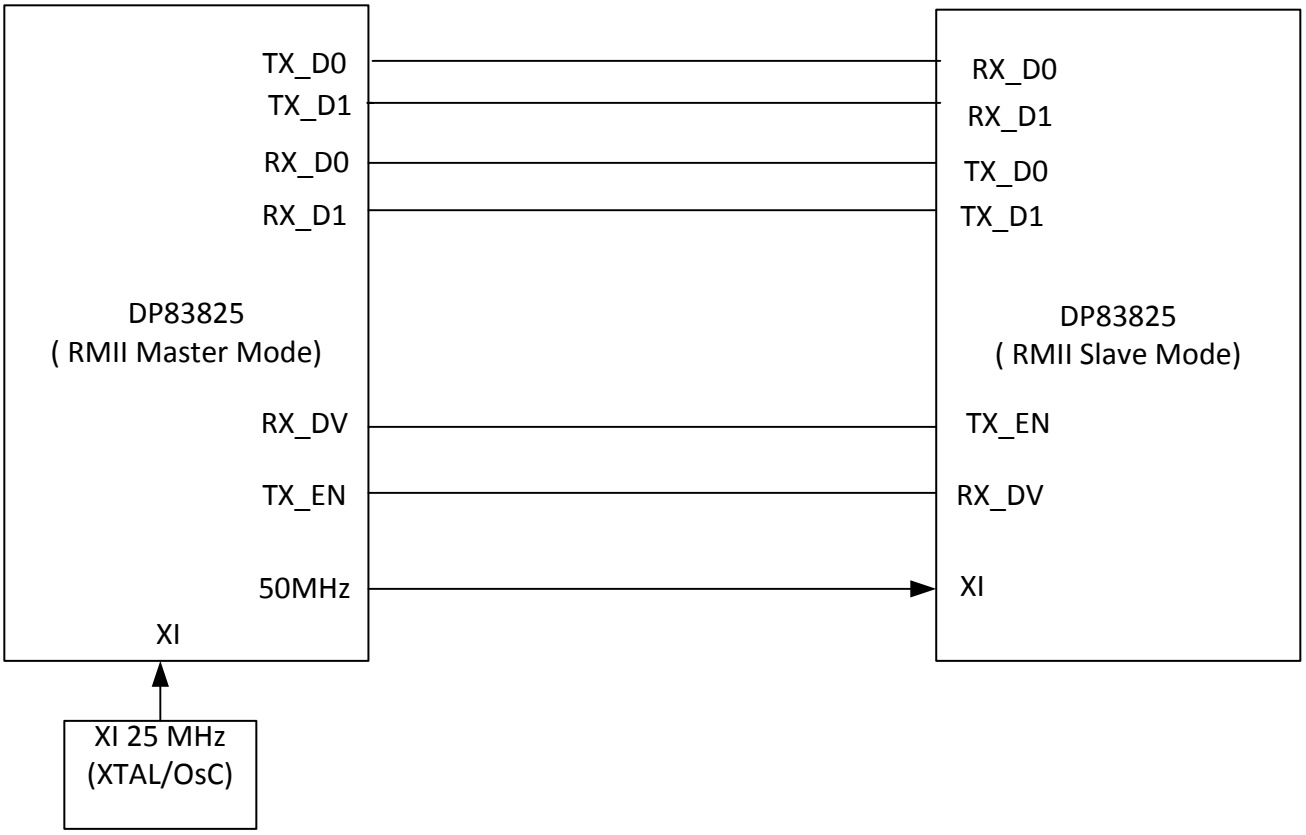

Figure 7. RMII Repeater Mode

8.3.6 Clock Output

The DP8325 has several clock output configuration options. An external crystal or CMOS-level oscillator provides the stimulus for the internal PHY reference clock. The local reference clock acts as the central source for all clocking within the device.

All clock configuration options are enabled using the IO MUX GPIO Control : 0x0303.[5:0] (LED 0), and 0x0305.[5:0] (LED 2) .

Clock options supported by the DP83825I include:

- MAC IF Clock
- XI Clock
- Free-Running Clock
- Recovered Clock

MAC IF Clock will operate at the same rate as the MAC interface selected. For RMII operation, MAC IF Clock frequency is 50 MHz. XI Clock is a pass-through option, which allows for the XI pin clock to be passed to a GPIO pin. Please note that the clock is buffered prior to transmission out of the GPIOs, and output clock amplitude will be at the selected VDDIO level. Free-Running Clock is an internally generated 125-MHz free-running clock thru PLL. Recovered Clock is a 125-MHz recovered clock from a connected link partner.

ADVANCE INFORMATION

Feature Description (continued)

8.3.7 Reduced Media Independent Interface (RMII)

The DP83825I incorporates the Reduced Media Independent Interface (RMII) as specified in the RMII specification v1.2. The purpose of this interface is to provide a reduced pin count alternative to the IEEE 802.3 MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but can be implemented in the absence of an MII. The DP83825I offers two types of RMII operations: RMII Slave and RMII Master. In RMII Master operation, the DP83825I operates off of either a 25-MHz CMOS-level oscillator connected to XI pin or a 25-MHz crystal connected across XI and XO pins. A 50-MHz output clock referenced from DP83825I can be connected to the MAC. In RMII Slave operation, the DP83825I operates off of a 50-MHz CMOS-level oscillator connected to the XI pin and shares the same clock as the MAC. Alternatively, in RMII Slave mode, the PHY can run from 50MHz clock provided by the Host MAC

The RMII specification has the following characteristics:

- Supports 100BASE-TX and 10BASE-Te.
- Single clock reference sourced from the MAC to PHY (or from an external source)
- Provides independent 2-bit wide transmit and receive data paths
- Uses CMOS signal levels, the same levels as the MII interface

In this mode, data transfers are two bits for every clock cycle using the internal 50-MHz reference clock for both transmit and receive paths.

The RMII signals are summarized below:

Table 1. RMII Signals

FUNCTION	PINS
Receive Data Lines	TX_D[1:0]
Transmit Data Lines	RX_D[1:0]
Receive Control Signal	TX_EN
Transmit Control Signal	CRS_DV

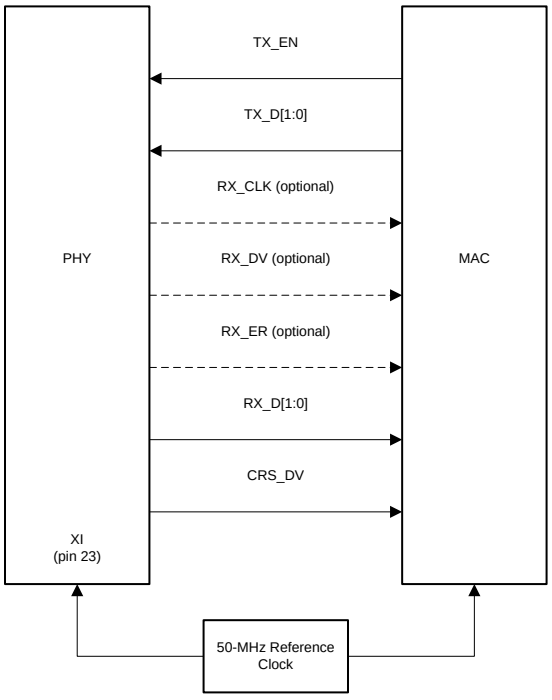

Figure 8. RMII Slave Signaling

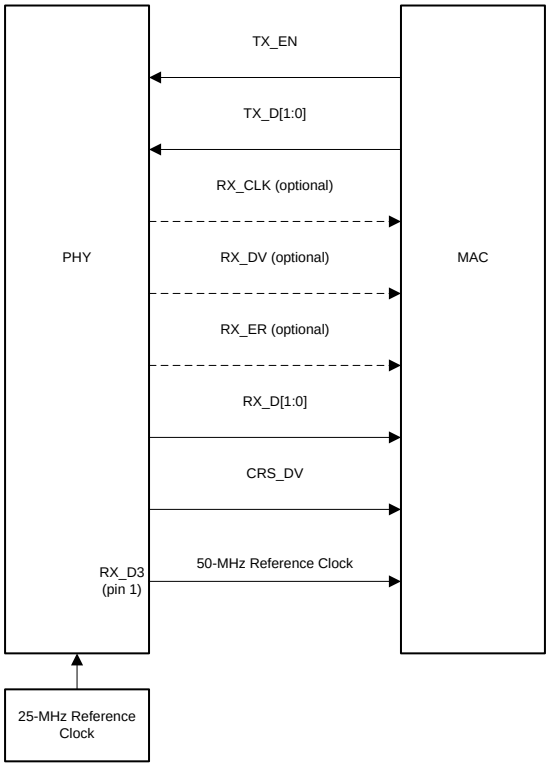

Figure 9. RMII Master Signaling

Data on TX_D[1:0] are latched at the PHY with reference to the clock edges on the XI pin. Data on RX_D[1:0] are latched at the MAC with reference to the same clock edges on the XI pin.

In addition, CRX_DV can be configured as RX_DV signal. It allows a simpler method of recovering receive data without the need to separate RX_DV from the CRS_DV indication.

RMII includes a programmable elastic buffer to adjust for the frequency differences between the reference clock and the recovered receive clock. The programmable elastic buffer minimizes internal propagation delay based on expected maximum packet size and clock accuracy.

Table below indicates how to program the buffer FIFO based on the expected maximum packet size and clock accuracy. It assumes that the RMII reference clock and the far-end transmitter clock have the same accuracy. Recevie buffer size is controlled via RCSR register (0x17[1:0]).

Table 2. Recommended RMII Packet Sizes

START THRESHOLD 0x17[1:0]	LATENCY TOLERANCE	RECOMMENDED PACKET SIZE AT ±50 ppm	RECOMMENDED PACKET SIZE AT ±100 ppm
1 (4-bits)	2 bits	2400 bytes	1200 bytes
2 (8-bits)	6 bits	7200 bytes	3600 bytes
3 (12-bits)	10 bits	12000 bytes	6000 bytes
4 (16-bits)	14 bits	16800 bytes	8400 bytes

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8.3.8 Serial Management Interface

The Serial Management Interface provides access to the DP83825I internal register space for status information and configuration. The SMI is compatible with IEEE 802.3 clause 22 and clause 45. The implemented register set consists of the registers required by the IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83825I.

The SMI includes the management clock (MDC) and the management input/output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 25 MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. MDIO pin requires a pullup resistor (2.2 KΩ or 1.5KΩ), which pulls MDIO high during IDLE and turnaround.

Up to 4 PHYs can share a common SMI bus. To distinguish between the PHYs, during power up or hardware reset, the DP83825I latches the Phy_Address[1:0] configuration pins to determine its address.

The management entity must not start an SMI transaction in the first cycle after power up or hardware reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after reset is de-asserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of turnaround. The addressed DP83825I drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83825I, thus eliminating the requirement for MDIO Turnaround. The turnaround time is filled by the management entity by inserting <10>.

Table 3. SMI Protocol

SMI PROTOCOL	<idle><start><op code><PHY address><reg addr><turnaround><data><idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle>

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8.3.8.1 Extended Register Space Access

The DP83825I SMI function supports read and write access to the extended register set using the Register Control Register (REGCR, address 0x000D), the Data Register (ADDAR, address 0x000E), and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah draft for Clause 22 for accessing the Clause 45 extended register set.

The standard register set, MDIO registers 0 to 31, is accessed using the normal direct-MDIO access or the indirect method, except for register REGCR and register ADDAR, which are accessed only using the normal MDIO transaction. The SMI function will ignore indirect access to these registers.

REGCR is the MMD access control. In general, register REGCR[4:0] is the device address DEVAD that directs any accesses of the ADDAR register to the appropriate MMD.

The DP83825I supports three MMD device addresses:

1. The Vendor-Specific device address DEVAD[4:0] = 11111 is used for general MMD register accesses.
2. DEVAD[4:0] = 00011 is used for Energy Efficient Ethernet MMD register accesses. Register names for registers accessible at this device address are preceded by MMD3.
3. DEVAD[4:0] = 00111 is used for Energy Efficient Ethernet MMD registers accesses. Register names for registers accessible at this device address are preceded by MMD7.

All accesses through register REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVAD are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

- ADDAR is the address/data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:14] is (00), then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to (00), accesses to register ADDAR modify the extended register set address register. This address register must always be initialized in order to access any of the registers within the extended register set.
- When REGCR[15:14] is set to (01), accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
- When REGCR[15:14] is set to (10), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- When REGCR[15:14] is set to (11), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write access only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR. The descriptions use the device address for general MMD register accesses (DEVAD[4:0] = 11111). For register accesses to the MMD3 or MMD7 registers the corresponding device address would be used.

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8.3.8.2 Write Address Operation

To set the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

8.3.8.3 Read Address Operation

To read the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Read the register address from register ADDAR.

Subsequent reads to register ADDAR (step 2) continue to read the address register.

8.3.8.4 Write (No Post Increment) Operation

To write a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

NOTE

Steps (1) and (2) can be skipped if the address register was previously configured.

8.3.8.5 Read (No Post Increment) Operation

To read a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) continue to reading the register selected by the value in the address register.

NOTE

Steps (1) and (2) can be skipped if the address register was previously configured.

8.3.8.6 Write (Post Increment) Operation

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = 31) or the value 0xC01F (data, post increment on writes function field = 11, DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) write the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

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8.3.8.7 Read (Post Increment) Operation

To read a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) read the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

8.3.8.8 Example Write Operation (No Post Increment)

The following example will demonstrate a write operation with no post increment. In this example, the MAC impedance will be adjusted to 99.25 Ω using the IO MUX GPIO Control Register (IOCTRL, address 0x0461).

1. Write the value 0x001F to register 0x000D.
2. Write the value 0x0461 to register 0x000E. (Sets desired register to the IOCTRL)
3. Write the value 0x401F to register 0x000D.
4. Write the value 0x0400 to register 0x000E. (Sets MAC impedance to 99.25 Ω)

8.3.8.9 Example Read Operation (No Post Increment)

The following example will demonstrate a read operation with no post increment. In this example, the MMD7 Energy Efficient Ethernet Link Partner Ability Register (MMD7_EEE_LP_ABILITY, address 0x703D) will be read.

1. Write the value 0x0007 to register 0x000D.
2. Write the value 0x003D to register 0x000E. (Sets desired register to the MMD7_EEE_LP_ABILITY)
3. Write the value 0x4007 to register 0x000D.
4. Read the value of register 0x000E. (Data read is the value contained within the MMD7_EEE_LP_ABILITY)

8.3.9 100BASE-TX

8.3.9.1 100BASE-TX Transmitter

The 100BASE-TX transmitter consists of several functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a scrambled MLT-3 125 Mbps serial data stream on the MDI. 4B5B encoding and decoding is detailed in Table 4 below.

The transmitter section consists of the following functional blocks:

1. Code-Group Encoder and Injection Block
2. Scrambler Block with Bypass Option
3. NRZ to NRZI Encoder Block
4. Binary to MLT-3 Converter / Common Driver Block

The bypass option for the functional blocks within the 100BASE-TX transmitter provides flexibility for applications where data conversion is not always required. The DP83825I implements the 100BASE-TX transmit state machine diagram as specified in the IEEE 802.3 Standard, Clause 24.

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Table 4. 4B5B Code-Group Encoding / Decoding

NAME	PCS 5B CODE-GROUP	MII 4B NIBBLE CODE
DATA CODES		
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
IDLE AND CONTROL CODES(1)		
H	00100	HALT code-group - Error code
I	11111	Inter-Packet IDLE - 0000
J	11000	First Start of Packet - 0101
K	10001	Second Start of Packet - 0101
T	01101	First End of Packet - 0000
R	00111	Second End of Packet - 0000
P	00000	EEE LPI - 0001(2)
INVALID CODES		
V	00001	
V	00010	
V	00011	
V	00101	
V	00110	
V	01000	
V	01100	
V	10000	
V	11001	

(1) Control code-groups I, J, K, T and R in data fields will be mapped as invalid codes, together with RX_ER asserted.
(2) Energy Efficient Ethernet LPI must also have TX_ER / RX_ER asserted and TX_EN / RX_DV deasserted.

8.3.9.1.1 Code-Group Encoding and Injection

The code-group encoder converts 4-bit (4B) nibble data generated by the MAC into 5-bit (5B) code-groups for transmission. This conversion is required to allow control data to be combined with packet data code-groups. Refer to Table 4 for 4B to 5B code-group mapping details.

The code-group encoder substitutes the first 8-bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmission. The code-group encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of transmit enable (TX_EN) signal from the MAC, the code-group encoder injects the T/R code-group pair (01101 00111) indicating the end of the frame.

After the T/R code-group pair, the code-group encoder continuously injects IDLEs into the transmit data stream until the next transmit packet is detected (reassertion of transmit enable).

8.3.9.1.2 Scrambler

The scrambler is required to control the radiated emissions at the media connector and on the twisted-pair cable. By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels at the MDI and on the cable could peak beyond FCC limitations at frequencies related to repeating 5B sequences (that is, continuous transmission of IDLEs).

The scrambler is configured as a closed loop linear feedback shift register (LFSR) with an 11-bit polynomial. The output of the closed loop LFSR is X-ORd with the serial NRZ data from the code-group encoder. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at certain frequencies by as much as 20 dB.

8.3.9.1.3 NRZ to NRZI Encoder

After the transmit data stream has been serialized and scrambled, the data must be NRZI encoded in order to comply with the TP-PMD standard for 100BASE-TX transmission over Category-5 unshielded twisted pair cable. There is no ability to bypass this block within the DP83825I. The NRZI data is sent to the 100 Mbps Driver.

8.3.9.1.4 Binary to MLT-3 Converter

The binary to MLT-3 conversion is accomplished by converting the serial binary data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events. These two binary streams are then fed to the twisted pair output driver which converts the voltage to current and alternately drives either side of the transmit transformer primary winding, resulting in a minimal current MLT-3 signal.

The 100BASE-TX MLT-3 signal sourced by the PMD output Pair common driver is slew rate controlled. This should be considered when selecting AC coupling magnetics to ensure TP-PMD standard compliant transition times (3 ns < Trise/fall < 5 ns).

The 100BASE-TX transmit TP-PMD function within the DP83825I is capable of sourcing only MLT-3 encoded data. Binary output from the PMD Output Pair is not possible in 100 Mbps mode. Fully encoded MLT-3 on both Tx+ and Tx- and can be configured by configuring Register 0x0404 (for example, in transformer-less designs).

8.3.9.2 100BASE-TX Receiver

The 100BASE-TX receiver consists of several functional blocks which convert the scrambled MLT-3 125 Mbps serial data stream to synchronous 2-bit wide data that is provided to the RMII.

The receive section consists of the following functional blocks:

1. Input and BLW Compensation
2. Signal Detect
3. Digital Adaptive Equalization
4. MLT-3 to Binary Decoder
5. Clock Recovery Module
6. NRZI to NRZ Decoder
7. Descrambler
8. Serial to Parallel
9. Code-Group Alignment

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10. 4B/5B Decoder
11. Link Integrity Monitor
12. Bad SSD Detection

8.3.10 10BASE-Te

The 10BASE-Te transceiver module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision detection, heartbeat, loopback, jabber, and link integrity functions, as defined in the standard.

8.3.10.1 Squelch

Squelch is responsible for determining when valid data is present on the differential receive inputs. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10BASE-Te standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of a packet is checked by the squelch, and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) are rejected. When this first squelch level is exceeded correctly, the opposite squelch level must then be exceeded no earlier than 50ns. Finally, the signal must again exceed the original squelch level no earlier than 50ns to qualify as a valid input waveform, and not be rejected. This checking procedure results in the typical loss of three preamble bits at the beginning of each packet. When the transmitter is operating, five consecutive transitions are checked before indicating that valid data is present. At this time, the squelch circuitry is reset.

8.3.10.2 Normal Link Pulse Detection and Generation

The link pulse generator produces pulses as defined in the IEEE 802.3 10BASE-Te standard. Each link pulse is nominally 100 ns in duration and transmitted every 16 ms in the absence of transmit data. Link pulses are used to check the integrity of the connection with the remote end.

8.3.10.3 Jabber

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition. The jabber function monitors the DP83825I output and disables the transmitter if it attempts to transmit a packet of longer than legal size. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active for approximately 100ms. When disabled by the Jabber function, the transmitter stays disabled for the entire time that the module's internal transmit enable is asserted. This signal must be de-asserted for approximately 500ms (unjab time) before the Jabber function re-enables the transmit outputs. The Jabber function is only available and active in 10BASE-Te mode.

8.3.10.4 Active Link Polarity Detection and Correction

Swapping the wires within the twisted-pair causes polarity errors. Wrong polarity affects 10BASE-Te connections. 100BASE-TX is immune to polarity problems because it uses MLT-3 encoding. 10BASE-Te receive block automatically detects reversed polarity.

8.3.11 Loopback Modes

There are several loopback options within the DP83825I that test and verify various functional blocks within the PHY. Enabling loopback modes allow for in-circuit testing of the digital and analog data paths. The DP83825I may be configured to any one of the Near-End Loopback modes or to the Far-End (reverse) Loopback mode. MII Loopback is configured using the Basic Mode Control Register (BMCR, address 0x0000). All other loopback modes are enabled using the BIST Control Register (BISCR, address 0x0016). Except where otherwise noted, loopback modes are supported for all speeds (10/100 Mbps and all MAC interfaces).

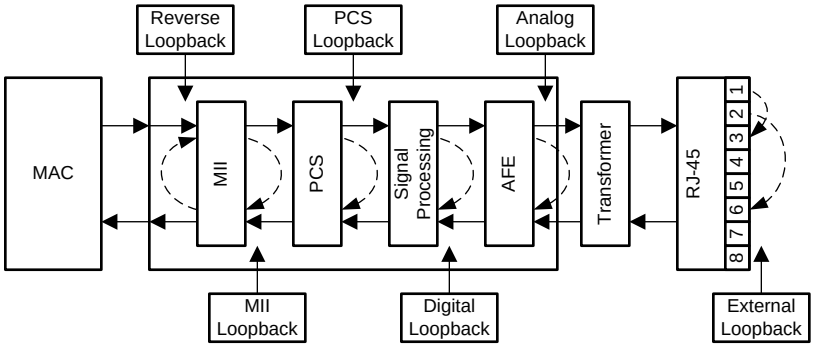

Figure 10. Loopback Test Modes

8.3.11.1 Near-End Loopback

Near-End Loopback provides the ability to loop the transmitted data back to the receiver via the digital or analog circuitry. The point at which the signal is looped back is selected using loopback control bits[3:0] in the BISCR register. Auto-Negotiation should be disabled before selecting the Near-End Loopback modes. This constraint does not apply for external-loopback mode.

8.3.11.2 MII Loopback

MII Loopback is the shallowest loop through the PHY. It is a useful test mode to validate communications between the MAC and the PHY. When in MII Loopback, data transmitted from a connected MAC on the TX path is internally looped back in the DP83825I to the RX pins where it can be checked by the MAC.

MII Loopback is enabled by setting bit[14] in the BMCR and bit[2] in BISCR.

8.3.11.3 PCS Loopback

PCS Loopback occurs in the PCS layer of the PHY. No signal processing is performed when using PCS Loopback.

PCS Input Loopback is enabled by setting bit[0] in the BISCR.

PCS Output Loopback is enabled by setting bit[1] in the BISCR.

8.3.11.4 Digital Loopback

Digital Loopback includes the entire digital transmit and receive paths. Data is looped back prior to the analog circuity.

Digital Loopback is enabled by setting bit[2] in the BISCR.

8.3.11.5 Analog Loopback

When operating in 10BASE-Te or 100BASE-TX mode, signals can be looped back after the analog front-end. Analog Loopback requires 100-Ω terminations across pins #1 and #2 as well as 100-Ω terminations across pins #3 and #6 at the RJ45.

Analog Loopback is enabled by setting bit[3] in the BISCR.

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8.3.11.6 Far-End (Reverse) Loopback

Far-End (Reverse) loopback is a special test mode to allow PHY testing with a link partner. In this mode, data that is received from the Link Partner passes through the PHY's receiver, is looped back at the MAC interface and then transmitted back to the Link Partner. While in Reverse Loopback mode, all data signals that come from the MAC are ignored.

Reverse Loopback is enabled by setting bit[4] in the BISCR.

8.3.12 BIST Configurations

The DP83825I incorporates an internal PRBS Built-in Self-Test (BIST) circuit to accommodate in-circuit testing and diagnostics. The BIST circuit can be used to test the integrity of transmit and receive data paths. The BIST can be performed using both internal loopbacks (digital or analog) or external loopback using a cable fixture. The BIST simulates pseudo-random data transfer scenarios in format of real packets and Inter-Packet Gap (IPG) on the lines. The BIST allows full control of the packet lengths and the IPG.

The BIST Packet Length is controlled using bits[10:0] in the BIST Control and Status Register #2 (BICSR2, address 0x001C). The BIST IPG Length is controlled using bits[7:0] in the BIST Control and Status Register #1 (BICSR1, address 0x001B).

The BIST is implemented with independent transmit and receive paths, with the transmit clock generating a continuous stream of a pseudo-random sequence. The device generates a 15-bit pseudo-random sequence for BIST. Received data is compared to the generated pseudo-random data to determine pass/fail status. The number of error bytes that the PRBS checker received is stored in bits[15:8] of the BICSR1. PRBS lock status and sync can be read from the BIST Control Register (BISCR, address 0x0016).

The PRBS test can be put in a continuous mode by using bit[14] in the BISCR. In continuous mode, when the BIST error counter reaches the maximum value, the counter starts counting from zero again. To read the BIST error count, bit[15] in the BICSR1 must be set to '1'. This will lock the current value of the BIST errors for reading. Please note that setting bit[15] also clears the BIST Error Counter.

8.3.13 Cable Diagnostics

With the vast deployment of Ethernet devices, the need for a reliable, comprehensive and user-friendly cable diagnostic tool is more important than ever. The wide variety of cables, topologies and connectors deployed results in the need to non-intrusively identify and report cable faults. The DP83825I offers Time Domain Reflectometry (TDR) capabilities in its Cable Diagnostic tool kit.

8.3.13.1 TDR

The DP83825I uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors and terminations in addition to estimating the cable length. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatches, cross faults, cross shorts and any other discontinuities along the cable.

The DP83825I transmits a test pulse of known amplitude (1 V) down each of the two pairs of an attached cable. The transmitted signal continues down the cable and reflects from each cable imperfection, fault, connector and from the end of the cable itself. After the pulse transmission, the DP83825I measures the return time and amplitude of all these reflected pulses. This technique enables measuring the distance and magnitude (impedance) of non-terminated cables (open or short), discontinuities (bad connectors) and improperly terminated cables with ±1m accuracy.

For all TDR measurements, the transformation between time of arrival and physical distance is done by the external host using minor computations (such as multiplication, addition and lookup tables). The host must know the expected propagation delay of the cable, which depends, among other things, on the cable category (for example, CAT5, CAT5e, or CAT6).

TDR measurement is allowed in the following scenarios:

- While the Link Partner is disconnected – cable is unplugged at the other side
- Link Partner is connected but remains “quiet” (for example, in power down mode)
- TDR could be automatically activated when the link fails or is dropped

TDR Auto-Run can be enabled by using bit[8] in the Control Regsiter #1 (CR1, address 0x0009). When a link drops, TDR will automatically execute and store the results in the respective TDR Cable Diagnostic Location Result Registers #1 - #5 (CDLRR, addresses 0x0180 to 0x0184) and the Cable Diagnostic Amplitude Result Registers #1 - #5 (CDLAR, addresses 0x0185 to 0x0189). TDR can also be run manually using bit[15] in the Cable Diagnostic Control Register (CDCR, address 0x001E). Cable diagnostic status is obtained by reading bits[1:0] in the CDCR. Additional TDR functions including cycle averaging and crossover disable can be found in the Cable Diagnostic Specific Control Register (CDSCR, address 0x0170).

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8.3.13.2 Fast Link Down Functionality

The DP83825I includes advanced link-down capabilities that support various real-time applications. The link-down mechanism is configurable and includes enhanced modes that allow extremely fast link-drop reaction times.

The DP83825I supports an enhanced link drop mechanism, also called Fast Link Drop (FLD), which shortens the observation window for determining link. There are multiple ways of determining link status, which can be enabled or disabled based on user preference. Fast Link Drop can be enabled in software using register configuration. FLD can be configured using the Control Register #3 (CR3, address 0x000B). Bits[3:0] and bit[10] allow for various FLD conditions to be enabled. When link drop occurs, indication of a particular fault condition can be read from the Fast Link Down Status Register (FLDS, address 0x000F).

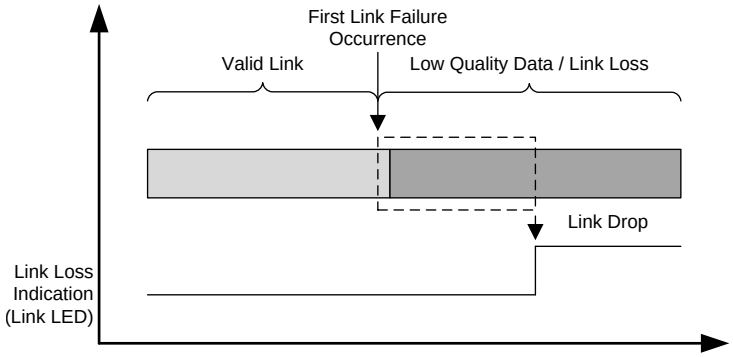

Figure 11. Fast Link Down

Fast Link Down criteria include:

- RX Error Count - when a predefined number of 32 RX_ERs occur in a 10μs window, the link will be dropped.
- MLT3 Error Count - when a predefined number of 20 MLT3 errors occur in a 10μs window, the link will be dropped.
- Low SNR Threshold - when a predefined number of 20 threshold crossings occur in a 10μs window, the link will be dropped.
- Signal/Energy Loss - when the energy detector indicates energy loss, the link will be dropped.

The Fast Link Down functionality allows the use of each of these options separately or in any combination.

NOTE

Because this mode enables extremely quick reaction time, it is more exposed to temporary bad link-quality scenarios.

8.3.14 Single Voltage Supply

The DP83825I integrates the LDO to generate internal power rails needed for the device

8.4 Device Functional Modes

DP83825I can be used in RMII Master Mode and Slave Mode. Refer to RMII section for connection diagram.

8.5 Programming

DP83825I provide IEEE defined register set for programming and status. It also provide additional register set to configure other feature not supported thru IEEE registers.

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8.6 Register Maps

8.6.1 DP83825I Registers

Table 5 lists the memory-mapped registers for the DP83825i registers. All register offset addresses not listed in Table 5 should be considered as reserved locations and the register contents should not be modified.

Table 5. DP83825I Registers

Offset	Acronym	Register Name	Section
0x0	BMCR_Register		Go
0x1	BMSR_Register		Go
0x2	PHYIDR1_Register		Go
0x3	PHYIDR2_Register		Go
0x4	ANAR_Register		Go
0x5	ALNPAR_Register		Go
0x6	ANER_Register		Go
0x7	ANNPTR_Register		Go
0x8	ANLNPTR_Register		Go
0x9	CR1_Register		Go
0xA	CR2_Register		Go
0xB	CR3_Register		Go
0xC	Register_12		Go
0xD	REGCR_Register		Go
0xE	ADDAR_Register		Go
0xF	FLDS_Register		Go
0x10	PHYSTS_Register		Go
0x11	PHYSCR_Register		Go
0x12	MISR1_Register		Go
0x13	MISR2_Register		Go
0x14	FCSCR_Register		Go
0x15	RECR_Register		Go
0x16	BISCR_Register		Go
0x17	RCSR_Register		Go
0x18	LEDCR_Register		Go
0x19	PHYCR_Register		Go
0x1A	10BTSCR_Register		Go
0x1B	BICSR1_Register		Go
0x1C	BICSR2_Register		Go
0x1D	Reserved_Register		Go
0x1E	CDCR_Register		Go
0x1F	PHYRCR_Register		Go

Complex bit access types are encoded to fit into small table cells. Table 6 shows the codes that are used for access types in this section.

Table 6. DP83825I Access Type Codes

Access Type	Code	Description
Read Type		
H	H	Set or cleared by hardware
R	R	Read
RO	R	Read

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Table 6. DP83825I Access Type Codes (continued)

Access Type	Code	Description
ROH	H R RO	Set or cleared by hardware Read
RW	R W	Read Write
Write Type		
W	W	Write
W, SC	W	Write
W/STRAP	W	Write
WL	L W	Write
WL/COR	L/COR W	Write
WSC	SC W	Write
WSTRAP	STRAP W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.1 BMCR_Register Register (Offset = 0x0) [reset = 0x3100]

BMCR_Register is shown in Figure 12 and described in Table 7.

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Figure 12. BMCR_Register Register

15	14	13	12	11	10	9	8
Reset	MII_Loopback	Speed_Selection	Auto-Negotiation_Enable	IEEE_Power_Down	Isolate	Restart_Auto-Negotiation	Duplex_Mode
W,SC-0x0	R/W-0x0	R/W-0x1	R/W-0x1	R/W-0x0	R/W-0x0	R/W,SC-0x0	R/W-0x1
7	6	5	4	3	2	1	0
Collision_Test	RESERVED						
R/W-0x0	R-0x0						

Table 7. BMCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reset	W,SC	0x0	PHY Software Reset: Writing a 1 to this bit resets the PHY PCS registers. When the reset operation is done, this bit is cleared to 0 automatically. PHY Vendor Specific registers will not be cleared. 0x0 = Normal Operation 0x1 = Initiate software Reset / Reset in Progress
14	MII_Loopback	R/W	0x0	MII Loopback: When MII loopback mode is activated, the transmitted data presented on MII TXD is looped back to MII RXD internally. Applicable for the only available RMII interface 0x0 = Normal Operation 0x1 = MII Loopback enabled

Table 7. BMCR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	Speed_Selection	R/W	0x1	Speed Select: When Auto-Negotiation is disabled (bit [12] = 0 in Register 0x0000), writing to this bit allows the port speed to be selected. DP83825C : Latched by Strap : AN_EN 0x0 = 10 Mbps 0x1 = 100 Mbps
12	Auto-Negotiation_Enable	R/W	0x1	Auto-Negotiation Enable: DP83825, DP83825S : Latched by strap AN_DIS DP83825C : Latched by strap AN_EN 0x0 = Disable Auto-Negotiation - bits [8] and [13] determine the port speed and duplex mode 0x1 = Enable Auto-Negotiation - bits [8] and [13] of this register are ignored when this bit is set
11	IEEE_Power_Down	R/W	0x0	Power Down: The PHY is powered down after this bit is set. Only register access is enabled during this power down condition. To control the power down mechanism, this bit is OR'ed with the input from the INT/PWDN_N pin. When the active low INT/PWDN_N is asserted, this bit is set. 0x0 = Normal Operation 0x1 = IEEE Power Down
10	Isolate	R/W	0x0	Isolate: 0x0 = Normal Operation 0x1 = Isolates the port from the MII with the exception of the serial management interface
9	Restart_Auto-Negotiation	R/W,SC	0x0	Restart Auto-Negotiation: If Auto-Negotiation is disabled (bit [12] = 0), bit [9] is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0x0 = Normal Operation 0x1 = Restarts Auto-Negotiation, Re-initiates the Auto-Negotiation process
8	Duplex_Mode	R/W	0x1	Duplex Mode: When Auto-Negotiation is disabled, writing to this bit allows the port Duplex capability to be selected. 0x0 = Half-Duplex 0x1 = Full-Duplex
7	Collision_Test	R/W	0x0	Collision Test: When set, this bit causes the COL signal to be asserted in response to the assertion of TX_EN within 512 bit times. The COL signal is de-asserted within 4 bit times in response to the de-assertion to TX_EN. 0x0 = Normal Operation 0x1 = Enable COL Signal Test
6-0	RESERVED	R	0x0	Reserved

8.6.1.2 BMSR_Register Register (Offset = 0x1) [reset = 0x7849]

BMSR_Register is shown in Figure 13 and described in Table 8.

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Figure 13. BMSR_Register Register

15	14	13	12	11	10	9	8
100Base-T4	100Base-TX_Full-Duplex	100Base-TX_Half-Duplex	10Base-T_Full-Duplex	10Base-T_Half-Duplex	RESERVED		
0x0	0x1	0x1	0x1	0x1	R-0x0		

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7	6	5	4	3	2	1	0
RESERVED	SMI_Preamble_Suppression	Auto-Negotiation_Complete	Remote_Fault	Auto-Negotiation_Ability	Link_Status	Jabber_Detect	Extended_Capability
R-0x0	0x1	0x0	H-0x0	0x1	0x0	H-0x0	0x1

Table 8. BMSR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	100Base-T4		0x0	100Base-T4 Capable: This protocol is not available. Always reads as 0.
14	100Base-TX_Full-Duplex		0x1	100Base-TX Full-Duplex Capable: 0x0 = Device not able to perform Full-Duplex 100Base-TX 0x1 = Device able to perform Full-Duplex 100Base-TX
13	100Base-TX_Half-Duplex		0x1	100Base-TX Half-Duplex Capable: 0x0 = Device not able to perform Half-Duplex 100Base-TX 0x1 = Device able to perform Half-Duplex 100Base-TX
12	10Base-T_Full-Duplex		0x1	10Base-T Full-Duplex Capable: 0x0 = Device not able to perform Full-Duplex 10Base-T 0x1 = Device able to perform Full-Duplex 10Base-T
11	10Base-T_Half-Duplex		0x1	10Base-T Half-Duplex Capable: 0x0 = Device not able to perform Half-Duplex 10Base-T 0x1 = Device able to perform Half-Duplex 10Base-T
10-7	RESERVED	R	0x0	Reserved
6	SMI_Preamble_Suppression		0x1	Preamble Suppression Capable: If this bit is set to 1, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround. 0x0 = Device not able to perform management transaction with preambles suppressed 0x1 = Device able to perform management transaction with preamble suppressed
5	Auto-Negotiation_Complete		0x0	Auto-Negotiation Complete: 0x0 = Device not able to perform management transaction with preambles suppressed 0x1 = Device able to perform management transaction with preamble suppressed
4	Remote_Fault	H	0x0	Remote Fault: Far End Fault indication or notification from Link Partner of Remote Fault. This bit is cleared on read or reset. 0x0 = No remote fault condition detected 0x1 = Remote fault condition detected
3	Auto-Negotiation_Ability		0x1	Auto-Negotiation Ability: 0x0 = Device is not able to perform Auto-Negotiation 0x1 = Device is able to perform Auto-Negotiation
2	Link_Status		0x0	Link Status: 0x0 = Link not established 0x1 = Valid link established (for either 10 Mbps or 100 Mbps operation)
1	Jabber_Detect	H	0x0	Jabber Detect: 0x0 = No jabber condition detected This bit only has meaning for 10Base-T operation. 0x1 = Jabber condition detected

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Table 8. BMSR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	Extended_Capability		0x1	Extended Capability: 0x0 = Basic register set capabilities only 0x1 = Extended register capabilities

8.6.1.3 PHYIDR1_Register Register (Offset = 0x2) [reset = X]

PHYIDR1_Register is shown in Figure 14 and described in Table 9.

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Figure 14. PHYIDR1_Register Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Organizationally_Unique_Identifier_Bits_21:6															
X															

Table 9. PHYIDR1_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Organizationally_Unique_Identifier_Bits_21:6		X	PHY Identifier Register #1

8.6.1.4 PHYIDR2_Register Register (Offset = 0x3) [reset = X]

PHYIDR2_Register is shown in Figure 15 and described in Table 10.

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Figure 15. PHYIDR2_Register Register

15	14	13	12	11	10	9	8
Organizationally_Unique_Identifier_Bits_5:0						Model_Number	
X						X	
7	6	5	4	3	2	1	0
Model_Number				Revision_Number			
X				0x0			

Table 10. PHYIDR2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Organizationally_Unique_Identifier_Bits_5:0		X	PHY Identifier Register #2
9-4	Model_Number		X	Vendor Model Number: The six bits of vendor model number are mapped from bits [9] to [4]
3-0	Revision_Number		0x0	Model Revision Number: Four bits of the vendor model revision number are mapped from bits [3:0]. This field is incremented for all major device changes.

8.6.1.5 ANAR_Register Register (Offset = 0x4) [reset = X]

ANAR_Register is shown in Figure 16 and described in Table 11.

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Figure 16. ANAR_Register Register

15	14	13	12	11	10	9	8
Next_Page	RESERVED	Remote_Fault	RESERVED	Asymmetric_Pause	Pause	100Base-T4	100Base-TX_Full-Duplex
R/W-0x0	R-0x0	R/W-0x0	R-0x0	R/W-0x0	R/W-0x0	0x0	R/W-X
7	6	5	4	3	2	1	0
100Base-TX_Half-Duplex	10Base-T_Full-Duplex	10Base-T_Half-Duplex	Selector_Field				
R/W-X	R/W-X	R/W-X	R/W-X				

Table 11. ANAR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next_Page	R/W	0x0	Next Page Indication: 0x0 = Next Page Transfer not desired 0x1 = Next Page Transfer desired
14	RESERVED	R	0x0	Reserved
13	Remote_Fault	R/W	0x0	Remote Fault: 0x0 = No Remote Fault detected 0x1 = Advertises that this device has detected a Remote Fault
12	RESERVED	R	0x0	Reserved
11	Asymmetric_Pause	R/W	0x0	Asymmetric Pause Support For Full-Duplex Links: 0x0 = Do not advertise asymmetric pause ability 0x1 = Advertise asymmetric pause ability
10	Pause	R/W	0x0	Pause Support for Full-Duplex Links: 0x0 = Do not advertise pause ability 0x1 = Advertise pause ability
9	100Base-T4		0x0	100Base-T4 Support: 0x0 = Do not advertise 100Base-T4 ability 0x1 = Advertise 100Base-T4 ability
8	100Base-TX_Full-Duplex	R/W	X	100Base-TX Full-Duplex Support: Values does not matter in forced-mode DP83825, DP83825S : Latched by strap AN_DIS DP83825C : Latched by strap AN_EN 0x0 = Do not advertise 100Base-TX Full-Duplex ability Values does not matter in forced-mode 0x1 = Advertise 100Base-TX Full-Duplex ability
7	100Base-TX_Half-Duplex	R/W	X	100Base-TX Half-Duplex Support: Values does not matter in forced-mode DP83825, DP83825S : Latched by strap AN_DIS DP83825C : Latched by strap AN_EN 0x0 = Do not advertise 100Base-TX Half-Duplex ability Values does not matter in forced-mode 0x1 = Advertise 100Base-TX Half-Duplex ability
6	10Base-T_Full-Duplex	R/W	X	10Base-T Full-Duplex Support: Values does not matter in forced-mode DP83825, DP83825S : Latched by strap AN_DIS DP83825C : Latched by strap AN_EN 0x0 = Do not advertise 10Base-T Full-Duplex ability Values does not matter in forced-mode 0x1 = Advertise 10Base-T Full-Duplex ability

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Table 11. ANAR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	10Base-T_Half-Duplex	R/W	X	10Base-T Half-Duplex Support: Values does not matter in forced-mode DP83825, DP83825S : Latched by strap AN_DIS DP83825C : Latched by strap AN_EN 0x0 = Do not advertise 10Base-T Half-Duplex ability Values does not matter in forced-mode 0x1 = Advertise 10Base-T Half-Duplex ability
4-0	Selector_Field	R/W	X	Protocol Selection Bits: Technology selector field (IEEE802.3u <00001>)

8.6.1.6 ALNPAR_Register Register (Offset = 0x5) [reset = X]

ALNPAR_Register is shown in Figure 17 and described in Table 12.

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Figure 17. ALNPAR_Register Register

15	14	13	12	11	10	9	8
Next_Page	Acknowledge	Remote_Fault	RESERVED	Asymmetric_Pause	Pause	100Base-T4	100Base-TX_Full-Duplex
0x0	0x0	0x0	R-0x0	0x0	0x0	0x0	0x0
7	6	5	4	3	2	1	0
100Base-TX_Half-Duplex	10Base-T_Full-Duplex	10Base-T_Half-Duplex	Selector_Field				
0x0	0x0	0x0	X				

Table 12. ALNPAR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next_Page		0x0	Next Page Indication: 0x0 = Link partner does not desire Next Page Transfer 0x1 = Link partner desires Next Page Transfer
14	Acknowledge		0x0	Acknowledge: 0x0 = Link partner does not acknowledge reception of link code word 0x1 = Link partner acknowledges reception of link code word
13	Remote_Fault		0x0	Remote Fault: 0x0 = Link partner does not advertise remote fault event detection 0x1 = Link partner advertises remote fault event detection
12	RESERVED	R	0x0	Reserved
11	Asymmetric_Pause		0x0	Asymmetric Pause: 0x0 = Link partner does not advertise asymmetric pause ability 0x1 = Link partner advertises asymmetric pause ability
10	Pause		0x0	Pause: 0x0 = Link partner does not advertise pause ability 0x1 = Link partner advertises pause ability
9	100Base-T4		0x0	100Base-T4 Support: 0x0 = Link partner does not advertise 100Base-T4 ability 0x1 = Link partner advertises 100Base-T4 ability

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Table 12. ALNPAR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	100Base-TX_Full-Duplex		0x0	100Base-TX Full-Duplex Support: 0x0 = Link partner does not advertise 100Base-TX Full-Duplex ability 0x1 = Link partner advertises 100Base-TX Full-Duplex ability
7	100Base-TX_Half-Duplex		0x0	100Base-TX Half-Duplex Support: 0x0 = Link partner does not advertise 100Base-TX Half-Duplex ability 0x1 = Link partner advertises 100Base-TX Half-Duplex ability
6	10Base-T_Full-Duplex		0x0	10Base-T Full-Duplex Support: 0x0 = Link partner does not advertise 10Base-T Full-Duplex ability 0x1 = Link partner advertises 10Base-T Full-Duplex ability
5	10Base-T_Half-Duplex		0x0	10Base-T Half-Duplex Support: 0x0 = Link partner does not advertise 10Base-T Half-Duplex ability 0x1 = Link partner advertises 10Base-T Half-Duplex ability
4-0	Selector_Field		X	Protocol Selection Bits: Technology selector field (IEEE802.3 <00001>)

8.6.1.7 ANER_Register Register (Offset = 0x6) [reset = 0x4]

ANER_Register is shown in Figure 18 and described in Table 13.

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Figure 18. ANER_Register Register

15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
RESERVED			Parallel_Detection_Fault	Link_Partner_Next_Page_Able	Local_Device_Next_Page_Able	Page_Received	Link_Partner_Auto-Negotiation_Able
R-0x0			H-0x0	0x0	0x1	H-0x0	0x0

Table 13. ANER_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0x0	Reserved
4	Parallel_Detection_Fault	H	0x0	Parallel Detection Fault: 0x0 = No fault detected 0x1 = A fault has been detected during the parallel detection process
3	Link_Partner_Next_Page_Able		0x0	Link Partner Next Page Ability: 0x0 = Link partner is not able to exchange next pages 0x1 = Link partner is able to exchange next pages
2	Local_Device_Next_Page_Able		0x1	Next Page Ability: 0x0 = Local device is not able to exchange next pages 0x1 = Local device is able to exchange next pages

Table 13. ANER_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	Page_Received	H	0x0	Link Code Word Page Received: 0x0 = A new page has not been received 0x1 = A new page has been received
0	Link_Partner_Auto-Negotiation_Able		0x0	Link Partner Auto-Negotiation Ability: 0x0 = Link partner does not support Auto-Negotiation 0x1 = Link partner supports Auto-Negotiation

8.6.1.8 ANNPTR_Register Register (Offset = 0x7) [reset = X]

ANNPTR_Register is shown in Figure 19 and described in Table 14.

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Figure 19. ANNPTR_Register Register

15	14	13	12	11	10	9	8
Next_Page	RESERVED	Message_Page	Acknowledge_2	Toggle	CODE		
R/W-0x0	R-0x0	R/W-0x1	R/W-0x0	0x0	R/W-X		
7	6	5	4	3	2	1	0
CODE							
R/W-X							

Table 14. ANNPTR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next_Page	R/W	0x0	Next Page Indication: 0x0 = Do not advertise desire to send additional next pages 0x1 = Advertise desire to send additional next pages
14	RESERVED	R	0x0	Reserved
13	Message_Page	R/W	0x1	Message Page: 0x0 = Current page is an unformatted page 0x1 = Current page is a message page
12	Acknowledge_2	R/W	0x0	Acknowledge2: Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received. 0x0 = Cannot comply with message 0x1 = Will comply with message
11	Toggle		0x0	Toggle: Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word. 0x0 = Value of toggle bit in previously transmitted Link Code Word was 1 0x1 = Value of toggle bit in previously transmitted Link Code Word was 0
10-0	CODE	R/W	X	This field represents the code field of the next page transmission. If the Message Page bit is set (bit [13] of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

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8.6.1.9 ANLNPTR_Register Register (Offset = 0x8) [reset = X]

ANLNPTR_Register is shown in Figure 20 and described in Table 15.

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Figure 20. ANLNPTR_Register Register

15	14	13	12	11	10	9	8
Next_Page	Acknowledge	Message_Page	Acknowledge_2	Toggle	Message/Unformatted_Field		
0x0	0x0	0x0	0x0	0x0	X		
7	6	5	4	3	2	1	0
Message/Unformatted_Field							
X							

Table 15. ANLNPTR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Next_Page		0x0	Next Page Indication: 0x0 = Do not advertise desire to send additional next pages 0x1 = Advertise desire to send additional next pages
14	Acknowledge		0x0	Acknowledge: 0x0 = Link partner does not acknowledge reception of link code work 0x1 = Link partner acknowledges reception of link code word
13	Message_Page		0x0	Message Page: 0x0 = Current page is an unformatted page 0x1 = Current page is a message page
12	Acknowledge_2		0x0	Acknowledge2: Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received. 0x0 = Cannot comply with message 0x1 = Will comply with message
11	Toggle		0x0	Toggle: Toggle is used by the Arbiitration function within Auto-Negotiation to synchronize with the Link Parnter during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word. 0x0 = Value of toggle bit in previously transmitted Link Code Word was 1 0x1 = Value of toggle bit in previously transmitted Link Code Word was 0
10-0	Message/Unformatted_Field		X	This field represents the code field of the next page transmission. If the Message Page bit is set (bit 13 of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interperated as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

8.6.1.10 CR1_Register Register (Offset = 0x9) [reset = 0x0]

CR1_Register is shown in Figure 21 and described in Table 16.

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Figure 21. CR1_Register Register

15	14	13	12	11	10	9	8
RESERVED						RESERVED	TDR_Auto-Run
R-0x0						R-0x0	R/W-0x0
7	6	5	4	3	2	1	0
Link_Loss_Recovery	RESERVED	Robust_Auto_MDIX	RESERVED	RESERVED		RESERVED	RESERVED
R/W-0x0	R-0x0	R/W-0x0	R-0x0	R-0x0		R-0x0	R-0x0

Table 16. CR1_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	TDR_Auto-Run	R/W	0x0	TDR Auto-Run at Link Down: 0x0 = Disable automatic execution of TDR 0x1 = Enable execution of TDR procedure after link down event
7	Link_Loss_Recovery	R/W	0x0	Link Loss Recovery: This mode allows recovery from short interference and continue to hold the link up for a period of additional mSec until the short interference is gone and the signal is OK. Under Normal Link Loss operation, Link status will go down approximately 250¿s from signal loss. 0x0 = Normal Link Loss operation 0x1 = Enable Link Loss Recovery mechanism
6	RESERVED	R	0x0	Reserved
5	Robust_Auto_MDIX	R/W	0x0	Robust Auto-MDIX: If link partners are configured for operational modes that are not supported by normal Auto-MDIX, Robust Auto-MDIX allows MDI/MDIX resolution and prevents deadlock. 0x0 = Disable Auto-MDIX 0x1 = Enable Robust Auto-MDIX
4	RESERVED	R	0x0	Reserved
3-2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

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8.6.1.11 CR2_Register Register (Offset = 0xA) [reset = 0x0]

CR2_Register is shown in Figure 22 and described in Table 17.

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Figure 22. CR2_Register Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED					
R-0x0	R-0x0	R-0x0					
7	6	5	4	3	2	1	0
RESERVED	RESERVED	Extended_Full-Duplex_Ability	Enhanced_LED_Link	RESERVED	RESERVED	Odd-Nibble_Detection_Disable	RMII_Receive_Clock
R-0x0	R-0x0	R/W-0x0	R/W-0x0	R-0x0	R-0x0	R/W-0x0	R/W-0x0

Table 17. CR2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R	0x0	Reserved
13-7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	Extended_Full-Duplex_Ability	R/W	0x0	Extended Full-Duplex Ability: 0x0 = Diable Extended Full-Duplex Ability. Decision to work in Full-Duplex or Half-Duplex mode follows IEEE specification 0x1 = Enable Full-Duplex while working with link partner in forced 100Base-TX. When the PHY is set to Auto-Negotiation or Force 100Base-TX and the link partner is operated in Force 100Base-TX, the link is always Full-Duplex
4	Enhanced_LED_Link	R/W	0x0	Enhanced LED Link: In Enhanced LED Link mode, TX/RX BLINK on activity is disabled for this LED pin. LED will only indicate LINK for established 100Base-TX Full-Duplex links. 0x0 = LED Link is ON when link is established 0x1 = LED Link is ON only when link is established in 100Base-TX Full-Duplex mode
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	Odd-Nibble_Detection_Disable	R/W	0x0	Detection of Transmit Error: 0x0 = Enable detection of de-assertion of TX_EN on an odd-nibble boundary. In this case TX_EN is extended by one additional TX_CLK cycle and behaves as if TX_ER were asserted during that additional cycle 0x1 = Disable detection of transmit error in odd-nibble boundary
0	RMII_Receive_Clock	R/W	0x0	RMII Receive Clock: 0x0 = RMII Data (RXD[1:0]) is sampled and referenced to XI 0x1 = RMII Data (RXD[1:0]) is sampled and referenced to RX_CLK

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8.6.1.12 CR3_Register Register (Offset = 0xB) [reset = 0x0]

CR3_Register is shown in Figure 23 and described in Table 18.

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Figure 23. CR3_Register Register

15	14	13	12	11	10	9	8
RESERVED					Descrambler_Fast_Link_Down_Mode	RESERVED	cfg_pbo_mode_en
R-0x0					R/W-0x0	R-0x0	R/W-0x0
7	6	5	4	3	2	1	0
cfg_quick_pbo_mode	Polarity_Swap	MDI/MDIX_Swap	RESERVED	Fast_Link_Down_Mode			
R/W-0x0	R/W-0x0	R/W-0x0	R-0x0	R/W-0x0			

Table 18. CR3_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved
10	Descrambler_Fast_Link_Down_Mode	R/W	0x0	Descrambler Fast Link Drop: This option can be enabled in parallel to the other fast link down modes in bits [3:0]. 0x0 = Do not drop the link on descrambler link loss 0x1 = Drop the link on descrambler link loss
9	RESERVED	R	0x0	Reserved
8	cfg_pbo_mode_en	R/W	0x0	Control Register #3
7	cfg_quick_pbo_mode	R/W	0x0	Control Register #3
6	Polarity_Swap	R/W	0x0	Polarity Swap: Port Mirror Function: To enable port mirroring, set this bit and bit [5] high. 0x1 = Inverted polarity on both pairs: TD+ and TD-, RD+ and RD- 0h = Normal polarity
5	MDI/MDIX_Swap	R/W	0x0	MDI/MDIX Swap: Port Mirror Function: To enable port mirroring, set this bit and bit [6] high. 0x0 = MDI pairs normal (Receive on RD pair, Transmit on TD pair) 0x1 = Swap MDI pairs (Receive on TD pair, Transmit on RD pair)
4	RESERVED	R	0x0	Reserved
3-0	Fast_Link_Down_Mode	R/W	0x0	Fast Link Down Modes: Bit 3 Drop the link based on RX Error count of the MII interface. When a predefined number of 32 RX Error occurences in a 10us interval is reached, the link will be dropped. Bit 2 Drop the link based on MLT3 Error count (Violation of the MLT3 coding in the DSP output). When a predefined number of 20 MLT3 Error occurences in10us interval is reached, the link will be dropped. Bit 1 Drop the link based on Low SNR Threshold. When a predefined number of 20 Threshold crossing occurences in a 10us interval is reached, the link will be dropped. Bit 0 Drop the link based on Signal/Energy Loss indication. When the Energy detector indicates Energy Loss, the link will be dropped. Typical reaction time is 10us. The Fast Link Down function is an OR of all 5 options (bits [10] and [3:0]), the designer can enable any combination of these conditions.

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8.6.1.13 Register_12 Register (Offset = 0xC) [reset = 0x0]

Register_12 is shown in Figure 24 and described in Table 19.

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Figure 24. Register_12 Register

15	14	13	12	11	10	9	8
Link_Quality_interrupt	energy_detect_interrupt	link_interrupt	speed_interrupt	duplex_interrupt	auto_negotiation_complete_interrupt	false_carrier_half_full_interrupt	rhf_interrupt
0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
7	6	5	4	3	2	1	0
Link_Quality_interrupt_enable	energy_detect_interrupt_enable	link_interrupt_enable	speed_interrupt_enable	duplex_interrupt_enable	auto_negotiation_complete_interrupt_enable	false_carrier_half_full_interrupt_enable	rhf_interrupt_enable
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 19. Register_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Link_Quality_interrupt		0x0	interrupt for Link quality indication
14	energy_detect_interrupt		0x0	interrupt for energy detect indication
13	link_interrupt		0x0	Interrupt for link status
12	speed_interrupt		0x0	interrupt for speed status
11	duplex_interrupt		0x0	interrupt for duplex
10	auto_negotiation_complete_interrupt		0x0	interrupt for autonegotiation
9	false_carrier_half_full_interrupt		0x0	interrupt for false carrier
8	rhf_interrupt		0x0	interrupt for rhf
7	Link_Quality_interrupt_enable	R/W	0x0	interrupt enable for Link quality indication
6	energy_detect_interrupt_enable	R/W	0x0	interrupt enable for energy detect indication
5	link_interrupt_enable	R/W	0x0	Interrupt enable for link status
4	speed_interrupt_enable	R/W	0x0	interrupt enalble for speed status
3	duplex_interrupt_enable	R/W	0x0	interrupt enable for duplex
2	auto_negotiation_complete_interrupt_enable	R/W	0x0	interrupt enable for autonegotiation
1	false_carrier_half_full_interrupt_enable	R/W	0x0	interrupt enable for false carrier
0	rhf_interrupt_enable	R/W	0x0	interrupt enable for rhf

8.6.1.14 REGCR_Register Register (Offset = 0xD) [reset = 0x0]

REGCR_Register is shown in Figure 25 and described in Table 20.

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Figure 25. REGCR_Register Register

15	14	13	12	11	10	9	8
Extended_Register_Command		RESERVED					
R/W-0x0		R-0x0					
7	6	5	4	3	2	1	0
RESERVED			DEVAD				
R-0x0			R/W-0x0				

Table 20. REGCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	Extended_Register_Command	R/W	0x0	Extended Register Command: 0x0 = Address 0x1 = Data, no post increment 0x2 = Data, post increment on read and write 0x3 = Data, post increment on write only
13-5	RESERVED	R	0x0	Reserved

Table 20. REGCR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	DEVAD	R/W	0x0	Device Address: Bits [4:0] are the device address, DEVAD, that directs any accesses of ADDAR register (0x000E) to the appropriate MMD. It uses the vendor specific DEVAD [4:0] = '11111' for accesses to registers 0x04D1 and lower. For MMD3 access, the DEVAD[4:0] = '00011'. For MMD7 access, the DEVAD[4:0] = '00111'. All accesses through registers REGCR and ADDAR should use the DEVAD for either MMD, MMD3 or MMD7. Transactions with other DEVAD are ignored.

8.6.1.15 ADDAR_Register Register (Offset = 0xE) [reset = 0x0]

ADDAR_Register is shown in Figure 26 and described in Table 21.

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Figure 26. ADDAR_Register Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address/Data															
R/W-0x0															

Table 21. ADDAR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Address/Data	R/W	0x0	If REGCR register bits [15:14] = '00', holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data.

8.6.1.16 FLDS_Register Register (Offset = 0xF) [reset = 0x0]

FLDS_Register is shown in Figure 27 and described in Table 22.

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Figure 27. FLDS_Register Register

15	14	13	12	11	10	9	8
RESERVED							Fast_Link_Down_Status
R-0x0							H-0x0
7	6	5	4	3	2	1	0
Fast_Link_Down_Status				RESERVED			
H-0x0				R-0x0			

Table 22. FLDS_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0x0	Reserved
8-4	Fast_Link_Down_Status	H	0x0	Fast Link Down Status: Status Registers that latch high each time a given Fast Link Down mode is activated and causes a link drop (assuming the modes were enabled) 0x1 = Signal/Energy Lost 0x2 = SNR Level 0x4 = MLT3 Errors 0x8 = RX Errors 0x10 = Descrambler Loss Sync
3-0	RESERVED	R	0x0	Reserved

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8.6.1.17 PHYSTS_Register Register (Offset = 0x10) [reset = 0x0]

PHYSTS_Register is shown in Figure 28 and described in Table 23.

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Figure 28. PHYSTS_Register Register

15	14	13	12	11	10	9	8
RESERVED	MDI/MDIX_Mode	Receive_Error_Latch	Polarity_Status	False_Carrier_Sense_Latch	Signal_Detect	Descrambler_Lock	Page_Received
R-0x0	0x0	H-0x0	H-0x0	H-0x0	0x0	0x0	0x0
7	6	5	4	3	2	1	0
MII_Interrupt	Remote_Fault	Jabber_Detect	Auto-Negotiation_Status	MII_Loopback_Status	Duplex_Status	Speed_Status	Link_Status
H-0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 23. PHYSTS_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	MDI/MDIX_Mode		0x0	MDI/MDIX Mode Status: 0x0 = MDI Pairs normal (Receive on RD pair, Transmit on TD pair) 0x1 = MDI Pairs swapped (Receive on TD pair, Transmit on RD pair)
13	Receive_Error_Latch	H	0x0	Receive Error Latch: This bit will be cleared upon a read of the RECR register 0x0 = No receive error event has occurred 0x1 = Receive error event has occurred since last read of RXERCNT register (0x0015)
12	Polarity_Status	H	0x0	Polarity Status: This bit is a duplication of bit [4] in the 10BTSCR register (0x001A). This bit will be cleared upon a read of the 10BTSCR register, but not upon a read of the PHYSTS register. 0x0 = Correct Polarity detected 0x1 = Inverted Polarity detected
11	False_Carrier_Sense_Latch	H	0x0	False Carrier Sense Latch: This bit will be cleared upon a read of the FCSR register. 0x0 = No False Carrier event has occurred 0x1 = False Carrier even has occurred since last read of FCSCR register (0x0014)
10	Signal_Detect		0x0	Signal Detect: Active high 100Base-TX unconditional Signal Detect indication from PMD
9	Descrambler_Lock		0x0	Descrambler Lock: Active high 100Base-TX Descrambler Lock indication from PMD
8	Page_Received		0x0	Link Code Word Page Received: This bit is a duplicate of Page Received (bit [1]) in the ANER register and it is cleared on read of the ANER register (0x0006). 0x0 = Link Code Word Page has not been received 0x1 = A new Link Code Word Page has been received
7	MII_Interrupt	H	0x0	MII Interrupt Pending: Interrupt source can be determined by reading the MISR register (0x0012). Reading the MISR will clear this interrupt bit indication. 0x0 = No interrupt pending 0x1 = Indicates that an internal interrupt is pending

Table 23. PHYSTS_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	Remote_Fault		0x0	Remote Fault: Cleared on read of BMSR register (0x0001) or by reset. 0x1 = Remote Fault condition detected. Fault criteria: notification from link partner of Remote Fault via Auto-Negotiation 0h = No Remote Fault condition detected
5	Jabber_Detect		0x0	Jabber Detection: This bit is only for 10 Mbps operation. This bit is a duplicate of the Jabber Detect bit in the BMSR register (0x0001) and will not be cleared upon a read of the PHYSTS register. 0x0 = No Jabber 0x1 = Jabber condition detected
4	Auto-Negotiation_Status		0x0	Auto-Negotiation Status: 0x0 = Auto-Negotiation not complete 0x1 = Auto-Negotiation complete
3	MII_Loopback_Status		0x0	MII Loopback Status: 0x0 = Normal operation 0x1 = Loopback enabled
2	Duplex_Status		0x0	Duplex Status: 0x0 = Half-Duplex mode 0x1 = Full-Duplex mode
1	Speed_Status		0x0	Speed Status: 0x0 = 100 Mbps mode 0x1 = 10 Mbps mode
0	Link_Status		0x0	Link Status: This bit is duplicated from the Link Status bit in the BMSR register (0x0001) and will not be cleared upon a read of the PHYSTS register. 0x0 = No link established 0x1 = Valid link established (for either 10 Mbps or 100 Mbps)

8.6.1.18 PHYSCR_Register Register (Offset = 0x11) [reset = 0x108]

PHYSCR_Register is shown in Figure 29 and described in Table 24.

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Figure 29. PHYSCR_Register Register

15	14	13	12	11	10	9	8
Disable_PLL	Power_Save_Mode_Enable	Power_Save_Modes		Scrambler_Bypass	RESERVED	Loopback_FIFO_Depth	
R/W-0x0	R/W-0x0	R/W-0x0		R/W-0x0	R-0x0	R/W-0x1	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			COL_Full-Duplex_Enable	Interrupt_Polarity	Test_Interrupt	Interrupt_Enable	Interrupt_Output_Enable
R-0x0			R/W-0x0	R/W-0x1	R/W-0x0	R/W-0x0	R/W-0x0

Table 24. PHYSCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Disable_PLL	R/W	0x0	Disable PLL: Note: clock circuitry can be disabled only in IEEE power down mode. 0x0 = Normal operation 0x1 = Disable internal clocks circuitry

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Table 24. PHYSCR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	Power_Save_Mode_Enable	R/W	0x0	Power Save Mode Enable: 0x0 = Normal operation 0x1 = Enable power save modes
13-12	Power_Save_Modes	R/W	0x0	Power Save Mode: 0x0 = Normal operation mode. PHY is fully functional 0x1 = Reserved 0x2 = Active Sleep, Low Power Active Energy Saving mode that shuts down all internal circuitry besides SMI and energy detect functionalities. In this mode the PHY sends NLP every 1.4 seconds to wake up link partner. Automatic power-up is done when link partner is detected. 0x3 = Passive Sleep, Low Power Passive Energy Saving mode that shuts down all internal circuitry besides SMI and energy detect functionalities. Automatic power-up is done when link partner is detected.
11	Scrambler_Bypass	R/W	0x0	Scrambler Bypass: 0x0 = Scrambler bypass disabled 0x1 = Scrambler bypass enabled
10	RESERVED	R	0x0	Reserved
9-8	Loopback_FIFO_Depth	R/W	0x1	Far-End Loopback FIFO Depth: This FIFO is used to adjust RX (receive) clock rate to TX clock rate. FIFO depth needs to be set based on expected maximum packet size and clock accuracy. Default value sets to 5 nibbles. 0x0 = 4 nibbles FIFO 0x1 = 5 nibbles FIFO 0x2 = 6 nibbles FIFO 0x3 = 8 nibbles FIFO
7-5	RESERVED	R	0x0	Reserved
4	COL_Full-Duplex_Enable	R/W	0x0	Collision in Full-Duplex Mode: 0x0 = Disable Collision in Full-Duplex mode. Collision will be active in Half-Duplex only. 0x1 = Enable generating Collision signaling in Full-Duplex mode
3	Interrupt_Polarity	R/W	0x1	Interrupt Polarity: 0x0 = Steady state (normal operation) is 0 logic and during interrupt is 1 logic 0x1 = Steady state (normal operation) is 1 logic and during interrupt is 0 logic
2	Test_Interrupt	R/W	0x0	Test Interrupt: Forces the PHY to generate an interrupt to facilitate interrupt testing. Interrupts will continue to be generated as long as this bit remains set. 0x0 = Do not generate interrupt 0x1 = Generate an interrupt
1	Interrupt_Enable	R/W	0x0	Interrupt Enable: Enable interrupt dependent on the event enables in the MISR register (0x0012). 0x0 = Disable event based interrupts 0x1 = Enable event based interrupts

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Table 24. PHYSCR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	Interrupt_Output_Enable	R/W	0x0	Interrupt Output Enable: Enable active low interrupt events via the INT/PWDN_N pin by configuring the INT/PWDN_N pin as an output. 0x0 = INT/PWDN_N is a Power Down pin 0x1 = INT/PWDN_N is an interrupt output

8.6.1.19 MISR1_Register Register (Offset = 0x12) [reset = 0x0]

MISR1_Register is shown in Figure 30 and described in Table 25.

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Figure 30. MISR1_Register Register

15	14	13	12	11	10	9	8
Link_Quality_Interrupt	Energy_Detect_Interrupt	Link_Status_Changed_Interrupt	Speed_Changed_Interrupt	Duplex_Mode_Changed_Interrupt	Auto-Negotiation_Completed_Interrupt	False_Carrier_Counter_Half-Full_Interrupt	Receive_Error_Counter_Half-Full_Interrupt
H-0x0	H-0x0	H-0x0	H-0x0	H-0x0	H-0x0	H-0x0	H-0x0
7	6	5	4	3	2	1	0
Link_Quality_Interrupt_Enable	Energy_Detect_Interrupt_Enable	Link_Status_Changed_Enable	Speed_Changed_Interrupt_Enable	Duplex_Mode_Changed_Interrupt_Enable	Auto-Negotiation_Completed_Enable	False_Carrier_HF_Enable	Receive_Error_HF_Enable
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 25. MISR1_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Link_Quality_Interrupt	H	0x0	Change of Link Quality Status Interrupt: 0x0 = Link quality is Good 0x1 = Change of link quality when link is ON
14	Energy_Detect_Interrupt	H	0x0	Change of Energy Detection Status Interrupt: 0x0 = No change of energy detected 0x1 = Change of energy detected
13	Link_Status_Changed_Interrupt	H	0x0	Change of Link Status Interrupt: 0x0 = No change of link status 0x1 = Change of link status interrupt is pending
12	Speed_Changed_Interrupt	H	0x0	Change of Speed Status Interrupt: 0x0 = No change of speed status 0x1 = Change of speed status interrupt is pending
11	Duplex_Mode_Changed_Interrupt	H	0x0	Change of Duplex Status Interrupt: 0x0 = No change of duplex status 0x1 = Change of duplex status interrupt is pending
10	Auto-Negotiation_Completed_Interrupt	H	0x0	Auto-Negotiation Complete Interrupt: 0x0 = No Auto-Negotiation complete event is pending 0x1 = Auto-Negotiation complete interrupt is pending
9	False_Carrier_Counter_Half-Full_Interrupt	H	0x0	False Carrier Counter Half-Full Interrupt: 0x0 = False Carrier half-full event is not pending 0x1 = False Carrier counter (Register FCSCR, address 0x0014) exceeds half-full interrupt is pending

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Table 25. MISR1_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	Receive_Error_Counter_Half-Full_Interrupt	H	0x0	Receiver Error Counter Half-Full Interrupt: 0x0 = Receive Error half-full event is not pending 0x1 = Receive Error counter (Register RECR, address 0x0015) exceeds half-full interrupt is pending
7	Link_Quality_Interrupt_Enable	R/W	0x0	Enable interrupt on change of link quality
6	Energy_Detect_Interrupt_Enable	R/W	0x0	Enable interrupt on change of energy detection
5	Link_Status_Changed_Enable	R/W	0x0	Enable interrupt on change of link status
4	Speed_Changed_Interrupt_Enable	R/W	0x0	Enable Interrupt on change of speed status
3	Duplex_Mode_Changed_Interrupt_Enable	R/W	0x0	Enable Interrupt on change of duplex status
2	Auto-Negotiation_Completed_Enable	R/W	0x0	Enable Interrupt on Auto-negotiation complete event
1	False_Carrier_HF_Enable	R/W	0x0	Enable Interrupt on False Carrier Counter Register half-full event
0	Receive_Error_HF_Enable	R/W	0x0	Enable Interrupt on Receive Error Counter Register half-full event

8.6.1.20 MISR2_Register Register (Offset = 0x13) [reset = 0x0]

MISR2_Register is shown in Figure 31 and described in Table 26.

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Figure 31. MISR2_Register Register

15	14	13	12	11	10	9	8
EEE_Error_Interrupt	Auto-Negotiation_Error_Interrupt	Page_Received_Interrupt	Loopback_FIFO_OF/UF_Event_Interrupt	MDI_Crossover_Change_Interrupt	Sleep_Mode_Interrupt	Polarity_Changed_Interrupt_/_WoL_Packet_Received_Interrupt	Jabber_Detect_Interrupt
H-0x0	H-0x0	H-0x0	H-0x0	H-0x0	H-0x0	H-0x0	H-0x0
7	6	5	4	3	2	1	0
EEE_Error_Interrupt_Enable	Auto-Negotiation_Error_Interrupt_Enable	Page_Received_Interrupt_Enable	Loopback_FIFO_OF/UF_Enable	MDI_Crossover_Change_Enable	Sleep_Mode_Event_Enable	Polarity_Changed_/_WoL_Packet_Enable	Jabber_Detect_Enable
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 26. MISR2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	EEE_Error_Interrupt	H	0x0	Energy Efficient Ethernet Error Interrupt: 0x0 = EEE error has not occurred 0x1 = EEE error has occurred
14	Auto-Negotiation_Error_Interrupt	H	0x0	Auto-Negotiation Error Interrupt: 0x0 = No Auto-Negotiation error even pending 0x1 = Auto-Negotiation error interrupt is pending

Table 26. MISR2_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	Page_Received_Interrupt	H	0x0	Page Receiver Interrupt: 0x0 = Page has not been received 0x1 = Page has been received
12	Loopback_FIFO_OF/UF_Event_Interrupt	H	0x0	Loopback FIFO Overflow/Underflow Event Interrupt: 0x0 = No FIFO Overflow/Underflow event pending 0x1 = FIFO Overflow/Underflow event interrupt pending
11	MDI_Crossover_Change_Interrupt	H	0x0	MDI/MDIX Crossover Status Change Interrupt: 0x0 = MDI crossover status has not changed 0x1 = MDI crossover status changed interrupt is pending
10	Sleep_Mode_Interrupt	H	0x0	Sleep Mode Event Interrupt: 0x0 = No Sleep mode event pending 0x1 = Sleep mode event interrupt is pending
9	Polarity_Changed_Interrupt_/_WoL_Packet_Received_Interrupt	H	0x0	Polarity Change Interrupt / WoL Packet Received Interrupt: 0x0 = No Data polarity even pending / No WoL oacket received 0x1 = Data polarity changed interrupt pending / WoL packet was recieved
8	Jabber_Detect_Interrupt	H	0x0	Jabber Detect Event Interrupt: 0x0 = No Jabber detect event pending 0x1 = Jabber detect even interrupt pending
7	EEE_Error_Interrupt_Enable	R/W	0x0	Enable interrupt on EEE Error
6	Auto-Negotiation_Error_Interrupt_Enable	R/W	0x0	Enable Interrupt on Auto-Negotiation error event
5	Page_Received_Interrupt_Enable	R/W	0x0	Enable Interrupt on page receive event
4	Loopback_FIFO_OF/UF_Enable	R/W	0x0	Enable Interrupt on loopback FIFO Overflow/Underflow event
3	MDI_Crossover_Change_Enable	R/W	0x0	Enable Interrupt on change of MDI/X status
2	Sleep_Mode_Event_Enable	R/W	0x0	Enable Interrupt on sleep mode event
1	Polarity_Changed_/_WoL_Packet_Enable	R/W	0x0	Enable Interrupt on change of polarity status
0	Jabber_Detect_Enable	R/W	0x0	Enable Interrupt on Jabber detection event

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8.6.1.21 FCSCR_Register Register (Offset = 0x14) [reset = 0x0]

FCSCR_Register is shown in Figure 32 and described in Table 27.

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Figure 32. FCSCR_Register Register

15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
False_Carrier_Event_Counter							
0x0							

Table 27. FCSCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0x0	Reserved
7-0	False_Carrier_Event_Counter		0x0	False Carrier Event Counter: This 8-bit counter increments on every false carrier event. This counter stops when it reaches its maximum count (FFh). When the counter exceeds half-full (7Fh), an interrupt event is generated. This register is cleared on read.

8.6.1.22 RECR_Register Register (Offset = 0x15) [reset = 0x0]

RECR_Register is shown in Figure 33 and described in Table 28.

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Figure 33. RECR_Register Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Receive_Error_Counter															
0x0															

Table 28. RECR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Receive_Error_Counter		0x0	RX_ER Counter: When a valid carrier is presented (only while RXDV is set), and there is at least one occurrence of an invalid data symbol, this 16-bit counter increments for each receive error detected. The RX_ER counter does not count in MII loopback mode. The counter stops when it reaches its maximum count (FFh). When the counter exceeds half-full (7Fh), an interrupt is generated. This register is cleared on read.

8.6.1.23 BISCR_Register Register (Offset = 0x16) [reset = 0x100]

BISCR_Register is shown in Figure 34 and described in Table 29.

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Figure 34. BISCR_Register Register

15	14	13	12	11	10	9	8
RESERVED	BIST_Error_Counter_Mode	PRBS_Packet_Type	Packet_Generation_Enable	PRBS_Checker_Lock/Sync	PRBS_Checker_Sync_Loss	Packet_Generator_Status	Power_Mode
R-0x0	R/W-0x0	R/W-0x0	R/W-0x0	0x0	H-0x0	0x0	0x1
7	6	5	4	3	2	1	0
RESERVED	Transmit_in_MII_Loopback	RESERVED	Loopback_Mode				
R-0x0	R/W-0x0	R-0x0	R/W-0x0				

Table 29. BISCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	BIST_Error_Counter_Mode	R/W	0x0	BIST Error Counter Mode: 0x0 = Single mode, when BIST Error Counter reaches its max value, PRBS checker stops counting. 0x1 = Continuous mode, when the BIST Error counter reaches its max value, a pulse is generated and the counter starts counting from zero again.

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Table 29. BISCR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	PRBS_Packet_Type	R/W	0x0	PRBS Packet Type: 0x1 = When packet generator is enabled (bit [12] : '1'), generate continuous packets with PRBS data. When packet generator is disabled, PRBS checker is still enabled.
12	Packet_Generation_Enable	R/W	0x0	Packet Generation Enable: 0x0 = Disable packet generator 0x1 = Enable packet generator with PRBS data
11	PRBS_Checker_Lock/Sync		0x0	PRBS Checker Lock/Sync Indication: 0x0 = PRBS checker is not locked 0x1 = PRBS checker is locked and synced on received bit stream
10	PRBS_Checker_Sync_Loss	H	0x0	PRBS Checker Sync Loss Indication: 0x0 = PRBS checker has not lost sync 0x1 = PRBS checker has lost sync
9	Packet_Generator_Status		0x0	Packet Generation Status Indication: 0x0 = Packet Generator is off 0x1 = Packet Generator is active and generating packets
8	Power_Mode		0x1	Sleep Mode Indication: 0x0 = Indicates that the PHY is in one of the sleep modes, either active or passive 0x1 = Indicates that the PHY is in normal power mode
7	RESERVED	R	0x0	Reserved
6	Transmit_in_MII_Loopback	R/W	0x0	Transmit Data in MII Loopback Mode (valid only at 100 Mbps) 0x0 = Data is not transmitted to the line in MII loopback 0x1 = Enable transmission of data from the MAC received on the TX pins to the line in parallel to the MII loopback to RX pins. This bit may be set only in MII Loopback mode - setting bit [14] in in BMCR register (0x0000)
5	RESERVED	R	0x0	Reserved
4-0	Loopback_Mode	R/W	0x0	Loopback Mode Select: The PHY provides several options for loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the digital and analog data paths 0x1 = PCS Input Loopback 0x2 = PCS Output Loopback 0x4 = Digital Loopback 0x8 = Analog Loopback (requires 100Ω termination) 0x10 = Reverse Loopback

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8.6.1.24 RCSR_Register Register (Offset = 0x17) [reset = 0x1]

RCSR_Register is shown in Figure 35 and described in Table 30.

Return to Summary Table.

Figure 35. RCSR_Register Register

15	14	13	12	11	10	9	8
RESERVED			RESERVED	RESERVED	RESERVED	RESERVED	RMII_TX_Clock_Shift
R-0x0			R-0x0	R-0x0	R-0x0	R-0x0	R/W-0x0
7	6	5	4	3	2	1	0
RMII_Clock_Select	RESERVED	RESERVED	RMII_Revision_Select	RMII_Overflow_Status	RMII_Underflow_Status	Receive_Elasticity_Buffer_Size	
0x0	R-0x0	R-0x0	R/W-0x0	0x0	0x0	R/W-0x1	

Table 30. RCSR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	Reserved
12	RESERVED	R	0x0	Reserved
11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	RMII_TX_Clock_Shift	R/W	0x0	RMII TX Clock Shift: 0x0 = Transmit path internal clock shift is disabled 0x1 = Transmit path internal clock shift is enabled
7	RMII_Clock_Select		0x0	RMII Reference Clock Select: Strap XI_50 determines the clock reference requirement. 0x0 = 25MHz clock reference, crystal or CMOS-level oscillator 0x1 = 50MHz clock reference, CMOS-level oscillator
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RMII_Revision_Select	R/W	0x0	RMII Revision Select: 0x0 = (RMII revision 1.2) CRS_DV will toggle at the end of a packet to indicate de-assertion of CRS 0x1 = (RMII revision 1.0) CRS_DV will remain asserted until final data is transferred. CRS_DV will not toggle at the end of a packet
3	RMII_Overflow_Status		0x0	RX FIFO Overflow Status: 0x0 = Overflow detected 0x1 = Normal
2	RMII_Underflow_Status		0x0	RX FIFO Underflow Status: 0x0 = Underflow detected 0x1 = Normal
1-0	Receive_Elasticity_Buffer_Size	R/W	0x1	Receive Elasticity Buffer Size: This field controls the Receive Elasticity Buffer which allows for frequency variation tolerance between the 50MHz RMII clock and the recovered data. The following values indicate the tolerance in bits for a single packet. The minimum setting allows for standard Ethernet frame sizes at ±50ppm accuracy. For greater frequency tolerance, the packet lengths may be scaled (for ±100ppm), divide the packet lengths by 2). 0x0 = 14 bit tolerance (up to 16800 byte packets) 0x1 = 2 bit tolerance (up to 2400 byte packets) 0x2 = 6 bit tolerance (up to 7200 byte packets) 0x3 = 10 bit tolerance (up to 12000 byte packets)

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8.6.1.25 LEDCR_Register Register (Offset = 0x18) [reset = X]

LEDCR_Register is shown in Figure 36 and described in Table 31.

Return to Summary Table.

Figure 36. LEDCR_Register Register

15	14	13	12	11	10	9	8
RESERVED					Blink_Rate		RESERVED
R-0x2					R/W-0x2		R-0x0
7	6	5	4	3	2	1	0
LED_Link_Polarity	RESERVED		Drive_Link_LED	RESERVED		Link_LED_ON/OFF_Setting	RESERVED
R/W-X	R-0x0		R/W-0x0	R-0x0		R/W-0x0	R-0x0

Table 31. LEDCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x2	Reserved
10-9	Blink_Rate	R/W	0x2	LED Blinking Rate (ON/OFF duration): 0x0 = 20Hz (50 ms) 0x1 = 10Hz (100 ms) 0x2 = 5Hz (200 ms) 0x3 = 2Hz (500 ms)
8	RESERVED	R	0x0	Reserved
7	LED_Link_Polarity	R/W	X	LED Link Polarity Setting: Link LED polarity defined by strapping value of this pin. This register allows for override of this strap value. 0x0 = Active Low polarity setting 0x1 = Active High polarity setting
6-5	RESERVED	R	0x0	Reserved
4	Drive_Link_LED	R/W	0x0	Drive Link LED Select: 0x0 = Normal operation 0x1 = Drive value of ON/OFF bit [1] onto LED_0 output pin
3-2	RESERVED	R	0x0	Reserved
1	Link_LED_ON/OFF_Setting	R/W	0x0	Value to force on Link LED output
0	RESERVED	R	0x0	Reserved

8.6.1.26 PHYCR_Register Register (Offset = 0x19) [reset = X]

PHYCR_Register is shown in Figure 37 and described in Table 32.

Return to Summary Table.

Figure 37. PHYCR_Register Register

15	14	13	12	11	10	9	8
Auto_MDI/X_Enable	Force_MDI/X	Pause_RX_Status	Pause_TX_Status	MII_Link_Status	RESERVED		
R/W-0x1	R/W-0x0	0x0	0x0	0x0	R-0x0		
7	6	5	4	3	2	1	0
Bypass_LED_Stretching	RESERVED	LED_Configuration	PHY_Address				
R/W-0x0	R-0x0	R/W-0x0	X				

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Table 32. PHYCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Auto_MDI/X_Enable	R/W	0x1	Auto-MDIX Enable: DP83825, DP83825S : Latched by strap A-MDIX 0x0 = Disable Auto-Negotiation Auto-MDIX capability 0x1 = Enable Auto-Negotiation Auto-MDIX capability
14	Force_MDI/X	R/W	0x0	Force MDIX: 0x0 = Normal operation (Receive on RD pair, Transmit on TD pair) 0x1 = Force MDI pairs to cross (Receive on TD pair, Transmit on RD pair)
13	Pause_RX_Status		0x0	Pause Receive Negotiation Status: Indicates that pause receive should be enabled in the MAC. Based on bits [11:10] in ANAR register and bits [11:10] in ANLPAR register settings. The function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, 'Pause Resolution', only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.
12	Pause_TX_Status		0x0	Pause Transmit Negotiated Status: Indicates that pause should be enabled in the MAC. Based on bits [11:10] in ANAR register and bits [11:10] in ANLPAR register settings. This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, 'Pause Resolution', only if the Auto-Negotiation highest common denominator is a Full-Duplex technology.
11	MII_Link_Status		0x0	MII Link Status: 0x0 = No active 100Base-TX Full-Duplex link, established using Auto-Negotiation 0x1 = 100Base-TX Full-Duplex link is active and it was established using Auto-Negotiation
10-8	RESERVED	R	0x0	Reserved
7	Bypass_LED_Stretching	R/W	0x0	Bypass LED Stretching: Set this bit to '1' to bypass the LED stretching, the LED reflects the internal value. 0x0 = Normal LED operation 0x1 = Bypass LED stretching
6	RESERVED	R	0x0	Reserved
5	LED_Configuration	R/W	0x0	
4-0	PHY_Address		X	PHY Address: Strapping configuration for PHY Address 825/825S : 2'B10 (digpad11, digpad10) 825C : 2'B00 (digpad10, digpad10)

8.6.1.27 10BTSCR_Register Register (Offset = 0x1A) [reset = 0x0]

10BTSCR_Register is shown in Figure 38 and described in Table 33.

Return to Summary Table.

Figure 38. 10BTSCR_Register Register

15	14	13	12	11	10	9	8
RESERVED		Receiver_Threshold_Enable	Squelch				RESERVED
R-0x0		R/W-0x0	R/W-0x0				R-0x0
7	6	5	4	3	2	1	0
NLP_Disable	RESERVED		Polarity_Status	RESERVED			Jabber_Disable
R/W-0x0	R-0x0		0x0	R-0x0			R/W-0x0

Table 33. 10BTSCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13	Receiver_Threshold_Enable	R/W	0x0	Lower Receiver Threshold Enable: 0x0 = Normal 10Base-T operation 0x1 = Enable 10Base-T lower receiver threshold to allow operation with longer cables
12-9	Squelch	R/W	0x0	Squelch Configuration: Used to set the Peak Squelch 'ON' threshold for the 10Base-T receiver. Starting from 200mV to 600mV, step size of 50mV with some overlapping as shown below: 0x0 = 200mV 0x1 = 250mV 0x2 = 300mV 0x3 = 350mV 0x4 = 400mV 0x5 = 450mV 0x6 = 500mV 0x7 = 550mV 0x8 = 600mV
8	RESERVED	R	0x0	Reserved
7	NLP_Disable	R/W	0x0	NLP Transmission Control: 0x0 = Enable transmission of NLPs 0x1 = Disable transmission of NLPs
6-5	RESERVED	R	0x0	Reserved
4	Polarity_Status		0x0	Polarity Status: This bit is a duplication of bit [12] in the PHYSTS register (0x0010). Both bits will be cleared upon a read of 10BTSCR register, but not upon a read of the PHYSTS register. 0x0 = Correct Polarity detected 0x1 = Inverted Polarity detected
3-1	RESERVED	R	0x0	Reserved
0	Jabber_Disable	R/W	0x0	Jabber Disable: Note: This function is only applicable in 10Base-T operation. 0x0 = Jabber function enabled 0x1 = Jabber function disabled

8.6.1.28 BICSR1_Register Register (Offset = 0x1B) [reset = X]

BICSR1_Register is shown in Figure 39 and described in Table 34.

Return to Summary Table.

Figure 39. BICSR1_Register Register

15	14	13	12	11	10	9	8
BIST_Error_Count							
0x0							
7	6	5	4	3	2	1	0
BIST_IPG_Length							
R/W-X							

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Table 34. BICSR1_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	BIST_Error_Count		0x0	BIST Error Count: Holds number of errored bytes received by the PRBS checker. Value in this register is locked and cleared when write is done to bit [15]. When BIST Error Counter Mode is set to '0', count stops on 0xFF (see register 0x0016) Note: Writing '1' to bit [15] will lock the counter's value for successive read operation and clear the BIST Error Counter.
7-0	BIST_IPG_Length	R/W	X	BIST IPG Length: Inter Packet Gap (IPG) Length defines the size of the gap (in bytes) between any 2 successive packets generated by the BIST. Default value is 0x7D (equal to 125 bytes).

8.6.1.29 BICSR2_Register Register (Offset = 0x1C) [reset = X]

BICSR2_Register is shown in Figure 40 and described in Table 35.

Return to Summary Table.

Figure 40. BICSR2_Register Register

15	14	13	12	11	10	9	8
RESERVED					BIST_Packet_Length		
R-0x0					R/W-X		
7	6	5	4	3	2	1	0
BIST_Packet_Length							
R/W-X							

Table 35. BICSR2_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved
10-0	BIST_Packet_Length	R/W	X	BIST Packet Length: Length of the generated BIST packets. The value of this register defines the size (in bytes) of every packet that is generated by the BIST. Default value is 0x5DC, which is equal to 1500 bytes.

8.6.1.30 Reserved_Register Register (Offset = 0x1D) [reset = 0x0]

Reserved_Register is shown in Figure 41 and described in Table 36.

Return to Summary Table.

Figure 41. Reserved_Register Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R-0x0															

Table 36. Reserved_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0x0	Reserved

8.6.1.31 CDCR_Register Register (Offset = 0x1E) [reset = 0x4000]

CDCR_Register is shown in Figure 42 and described in Table 37.

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Figure 42. CDCR_Register Register

15	14	13	12	11	10	9	8
Cable_Diagnostic_Start	cfg_rescal_en	RESERVED					
R/W-0x0	R/W-0x1	R-0x0					
7	6	5	4	3	2	1	0
RESERVED						Cable_Diagnostic_Status	Cable_Diagnostic_Test_Fail
R-0x0						0x0	0x0

Table 37. CDCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Cable_Diagnostic_Start	R/W	0x0	Cable Diagnostic Process Start: Diagnostic Start bit is cleared once Diagnostic Done indication bit is triggered. 0x0 = Cable Diagnostic is disabled 0x1 = Start cable measurement
14	cfg_rescal_en	R/W	0x1	Resistor calibration Start
13-2	RESERVED	R	0x0	Reserved
1	Cable_Diagnostic_Status		0x0	Cable Diagnostic Process Done: 0x0 = Cable Diagnostic had not completed 0x1 = Indication that cable measurement process is complete
0	Cable_Diagnostic_Test_Fail		0x0	Cable Diagnostic Process Fail: 0x0 = Cable Diagnostic has not failed 0x1 = Indication that cable measurement process failed

8.6.1.32 PHYRCR_Register Register (Offset = 0x1F) [reset = 0x0]

PHYRCR_Register is shown in Figure 43 and described in Table 38.

Return to Summary Table.

Figure 43. PHYRCR_Register Register

15	14	13	12	11	10	9	8
Software_Reset	Digital_reset	SOR_debug_option	RESERVED				
R/W,SC-0x0	R/W,SC-0x0	R/W-0x0	R-0x0				
7	6	5	4	3	2	1	0
RESERVED							
R-0x0							

Table 38. PHYRCR_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Software_Reset	R/W,SC	0x0	Software Reset: 0x0 = Normal Operation 0x1 = Reset PHY. This bit is self cleared and has the same effect as Hardware reset pin.
14	Digital_reset	R/W,SC	0x0	Software Restart: 0x0 = Normal Operation 0x1 = Restart PHY. This bit is self cleared and resets all PHY circuitry except the registers.
13	SOR_debug_option	R/W	0x0	PHY Reset Control Register

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Table 38. PHYRCR_Register Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-0	RESERVED	R	0x0	Reserved

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DP83825I is a single-port 10/100 Mbps Ethernet PHY. It supports connections to an Ethernet MAC through RMII. Connections to the Ethernet media are made via the IEEE 802.3 defined Media Dependent Interface.

When using the device for Ethernet applications, it is necessary to meet certain requirements for normal operation. The following subsections are intended to assist in appropriate component selection and required circuit connections.

9.2 Typical Applications

Figure 44 shows a typical application for the DP83825I.

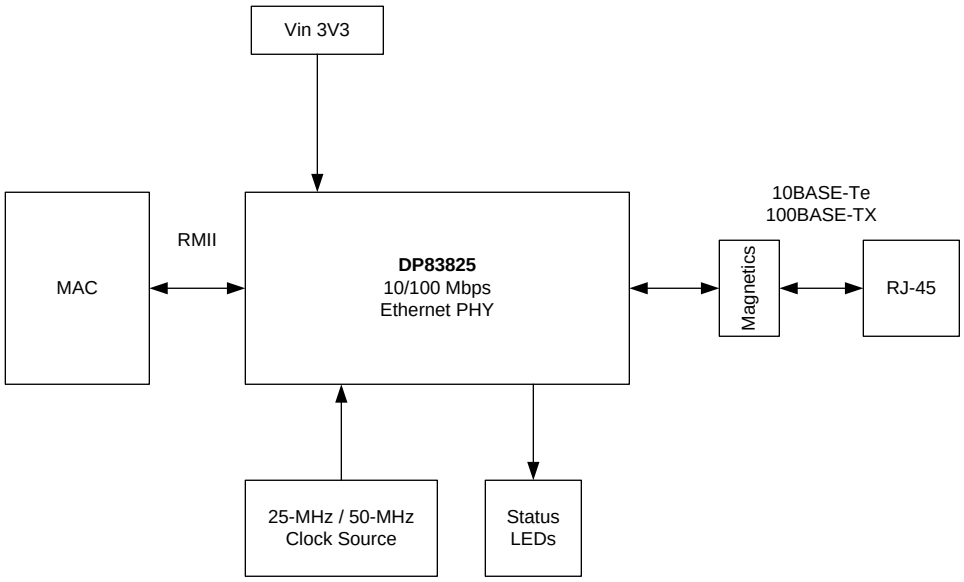

Figure 44. Typical DP83825I Application

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Typical Applications (continued)

9.2.1 TPI Network Circuit

Figure 45 shows the recommended twisted-pair interface network circuit for 10/100 Mbps. Variations with PCB and component characteristics require that the application be tested to verify that the circuit meets the requirements of the intended application.

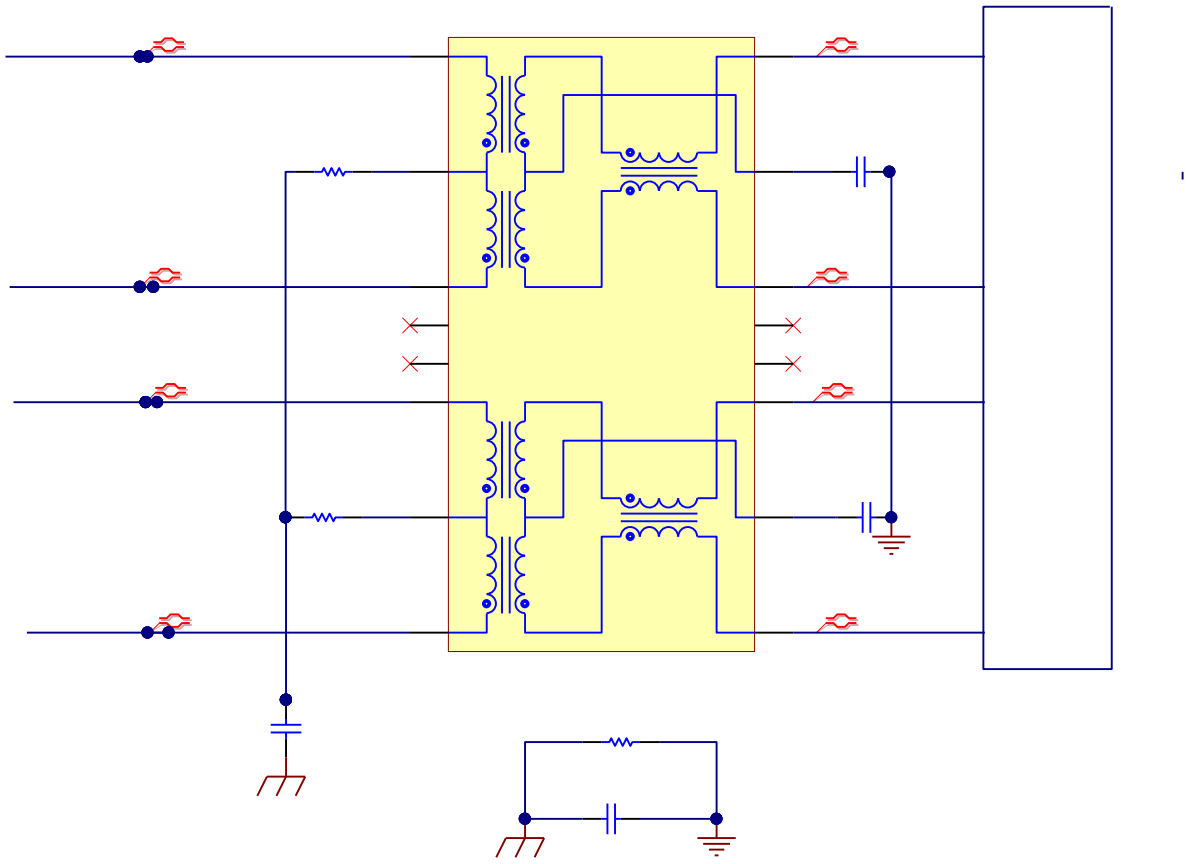

Figure 45. TPI Network Circuit

9.2.2 Design Requirements

The design requirements for the DP83825I in TPI operation (100BASE-TX or 10BASE-Te) are:

1. AVD Supply = 3.3 V
2. VDDIO Supply = 3.3V or 1.8 V
3. Reference Clock Input = 25-MHz or 50-MHz (RMII Slave)

9.2.2.1 Clock Requirements

The DP83825I supports an external CMOS-level oscillator source or an internal oscillator with an external crystal.

9.2.2.1.1 Oscillator

If an external clock source is used, XI should be tied to the clock source and XO should be left floating. The amplitude of the oscillator should be a nominal voltage of VDDIO.

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Typical Applications (continued)

9.2.2.1.2 Crystal

The use of a 25-MHz, parallel resonant, 20-pF load crystal is recommended if operating with a crystal. A typical connection diagram is shown below for a crystal resonator circuit. The load capacitor values will vary with the crystal vendors; check with the vendor for the recommended loads.

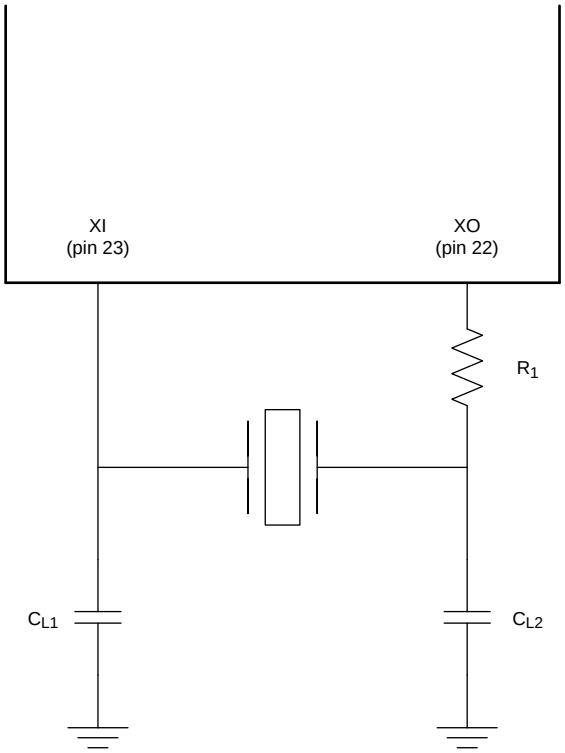

Figure 46. Crystal Oscillator Circuit

ADVANCE INFORMATION

Typical Applications (continued)

Table 39. 25-MHz Oscillator Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature	-50		50	ppm
Frequency Stability	1 year aging	-50		50	ppm
Rise / Fall Time	10% - 90%			8	nsec
Jitter (Short Term)	Cycle-to-cycle			TBD	psec
Jitter (Long Term)	Accumulative over 10 ms			1.75	nsec
Symmetry	Duty Cycle	40		60	%
Load Capacitance			15	30	pF

Table 40. 50-MHz Oscillator Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			50		MHz
Frequency Tolerance	Operational Temperature	-50		50	ppm
Frequency Stability	1 year aging	-50		50	ppm
Rise / Fall Time	10% - 90%			8	nsec
Jitter (Short Term)	Cycle-to-cycle			TBD	psec
Jitter (Long Term)	Accumulative over 10 ms			TBD	nsec
Symmetry	Duty Cycle	40		60	%
Load Capacitance			15	30	pF

Table 41. 25-MHz Crystal Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature	-50		50	ppm
	At 25°C	-50		50	ppm
Frequency Stability	1 year aging	-5		5	ppm
Load Capacitance			15	40	pF
ESR				50	Ohm

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9.2.3 Detailed Design Procedure

The Media Independent Interface RMII connects the DP83825I to the Media Access Controller (MAC). The MAC may in-fact be a discrete device or integrated into a microprocessor, CPU, FPGA, or ASIC. The Media Dependent Interface (MDI) connects the DP83825I to the transformer of the Ethernet network or to AC isolation capacitors when interfacing with a fiber transceiver.

9.2.3.1 RMII Layout Guidelines

1. RMII signals are single-ended signals
2. Traces should be routed with 50-Ω impedance to ground
3. Keep trace lengths as short as possible, less than two inches is recommended and less than six inches maximum

9.2.3.2 MDI Layout Guidelines

1. MDI signals are differential
2. Traces should be routed with 50-Ω impedance to ground and 100-Ω differential controlled impedance
3. Route MDI traces to the transformer on the same layer
4. Use a metal shielded RJ-45 connector and electrically connect the shield to chassis ground

5. Avoid supplies and ground beneath the magnetics
6. Do not overlap the circuit ground and chassis ground planes. Keep chassis ground and circuit ground isolated by turning chassis ground into an isolated island by leaving a gap between the planes. Connecting a 1206 (size) capacitor between chassis ground and circuit ground is recommended to avoid floating metal. Capacitors less than 805 (size) can create an arching path for ESD due to a small air-gap.

10 Power Supply Recommendations

The DP83825I is capable of operating with a 3.3 V or 1.8 V of I/O supply voltages along with analog supply of 3.3 V. The recommended power supply de-coupling network is shown below:

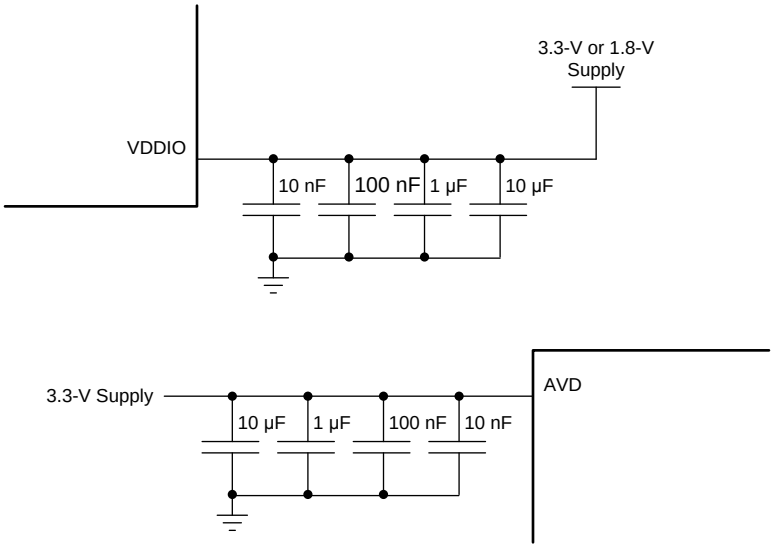

Figure 47. DP83825I Power Supply Decoupling Recommendation

11 Layout

11.1 Layout Guidelines

11.1.1 Signal Traces

PCB traces are lossy and long traces can degrade signal quality. Traces should be kept short as possible. Unless mentioned otherwise, all signal traces should be 50-Ω single-ended impedance. Differential traces should 100-Ω differential. Take care to ensure impedance is controlled throughout. Impedance discontinuities will cause reflections leading to emissions and signal integrity issues. Stubs should be avoided on all signal traces, especially differential signal pairs.

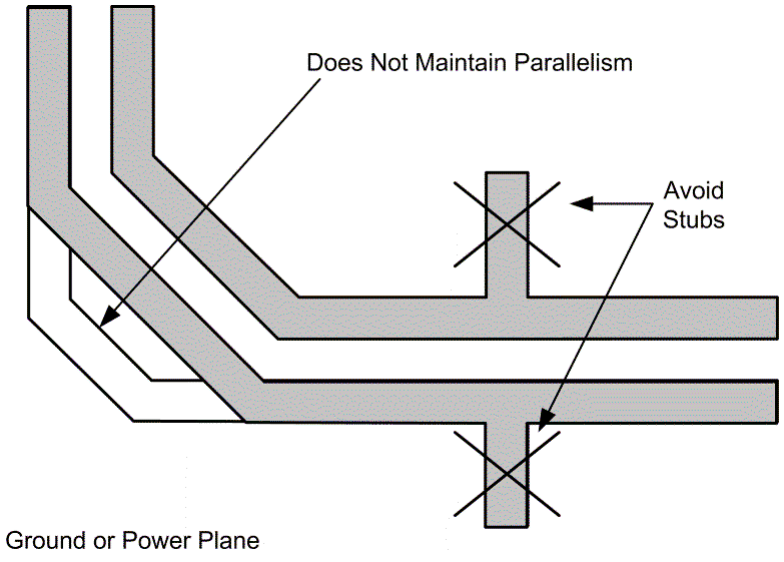

Figure 48. Differential Signal Traces

Layout Guidelines (continued)

Within the differential pairs, trace lengths should be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and emissions. Length matching is also important for MAC interface connections. All RMII transmit signal traces should be length matched to each other and all RMII receive signal traces should be length matched to each other.

Ideally, there should be no crossover or vias on signal path traces. Vias present impedance discontinuities and should be minimized when possible. Route trace pairs on the same layer. Signals on different layers should not cross each other without at least one return path plane between them. Differential pairs should always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

Layout Guidelines (continued)

11.1.2 Return Path

A general best practice is to have a solid return path beneath all MDI signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path between the signal traces should be avoided at all cost. A signal crossing a split plane may cause unpredictable return path currents and could impact signal quality and result in emissions issues.

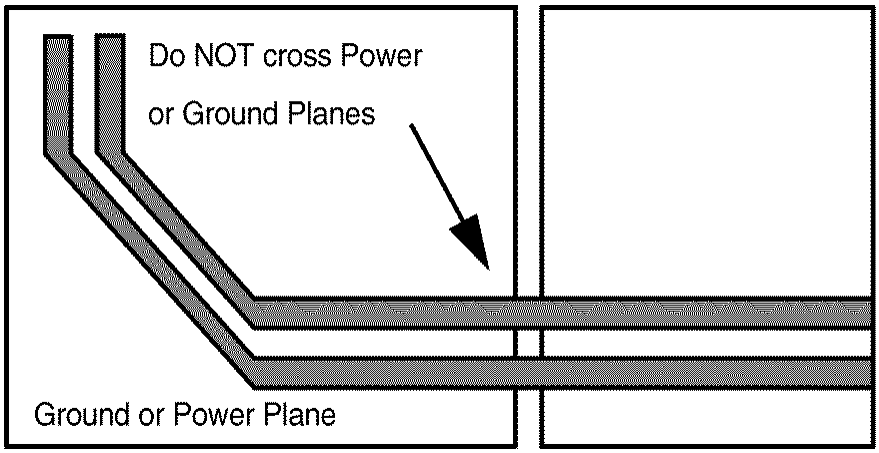

Figure 49. Differential Signal Pair and Plane Crossing

Layout Guidelines (continued)

11.1.3 Transformer Layout

There must be no metal layer running beneath the transformer. Transformers can inject noise into metal beneath them, which can affect the performance of the system. Figure 45.

11.1.3.1 Transformer Recommendations

The following magnetics have been tested with the DP83825I using the DP83825I EVM.

Table 42. Recommended Transformers

MANUFACTURER	PART NUMBER
Pulse Electronics	HX1198FNL
	HX1188NL
	HX1188FNL

Table 43. Transformer Electrical Specifications

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turn Ratio	±2%	1:1	-
Insertion Loss	1 - 100 MHz	–1	dB
Return Loss	1 - 30 MHz	–16	dB
	30 - 60 MHz	–12	dB
	60 - 80 MHz	–10	dB
Differential to Common Rejection Ratio	1 - 50 MHz	–30	dB
	50 - 150 MHz	–20	dB
Crosstalk	30 MHz	–35	dB
	60 MHz	–30	dB
Isolation	HPOT	1500	Vrms

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11.1.4 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

11.1.5 PCB Layer Stacking

To meet signal integrity and performance requirements, a minimum four-layer PCB is recommended. However, a six-layer PCB should be used when possible.

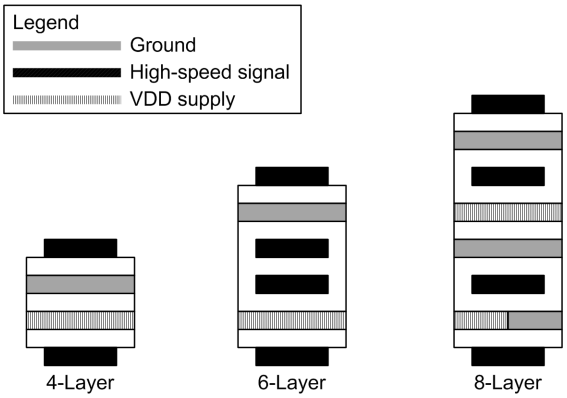


Figure 50. Recommended Layer Stack-Up

11.2 Layout Example

See the DP83825EVM for more information regarding layout.

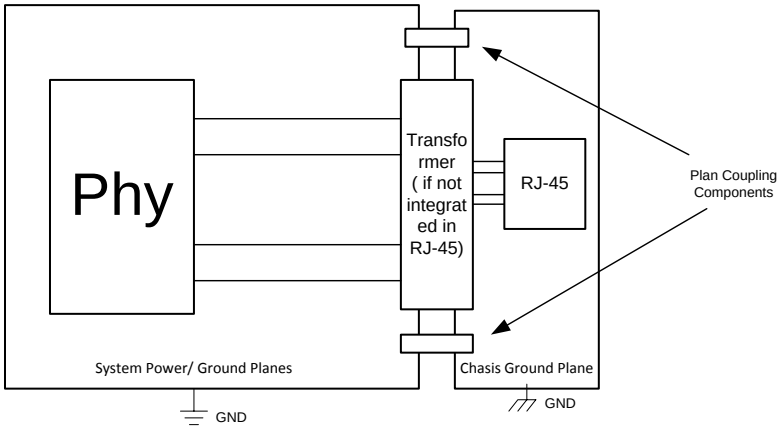


Figure 51. Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

13 Mechanical, Packaging, and Orderable Information

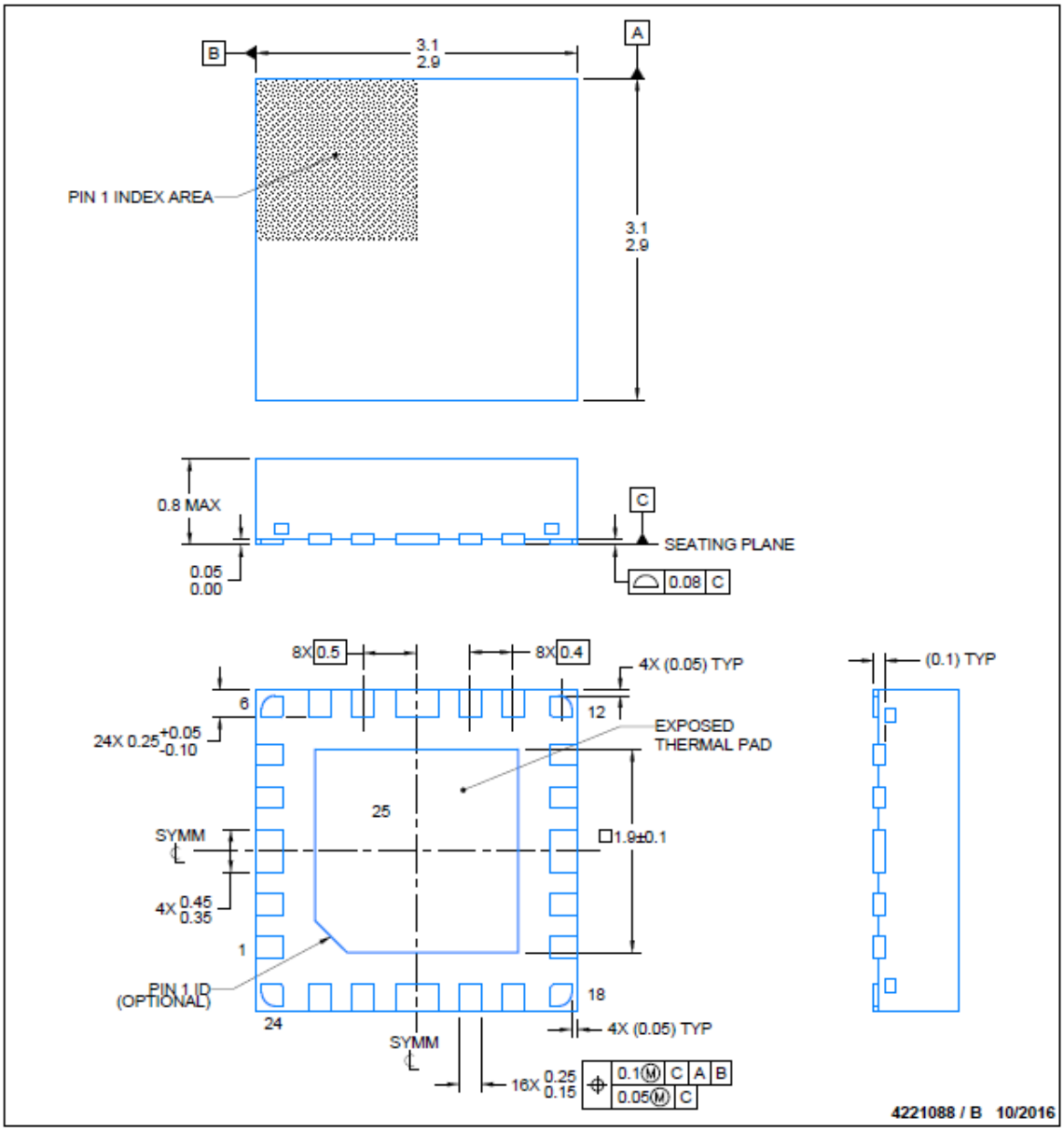
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Figure 52. DP83825I Package Drawing

PACKAGE OUTLINE

RMQ0024A — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

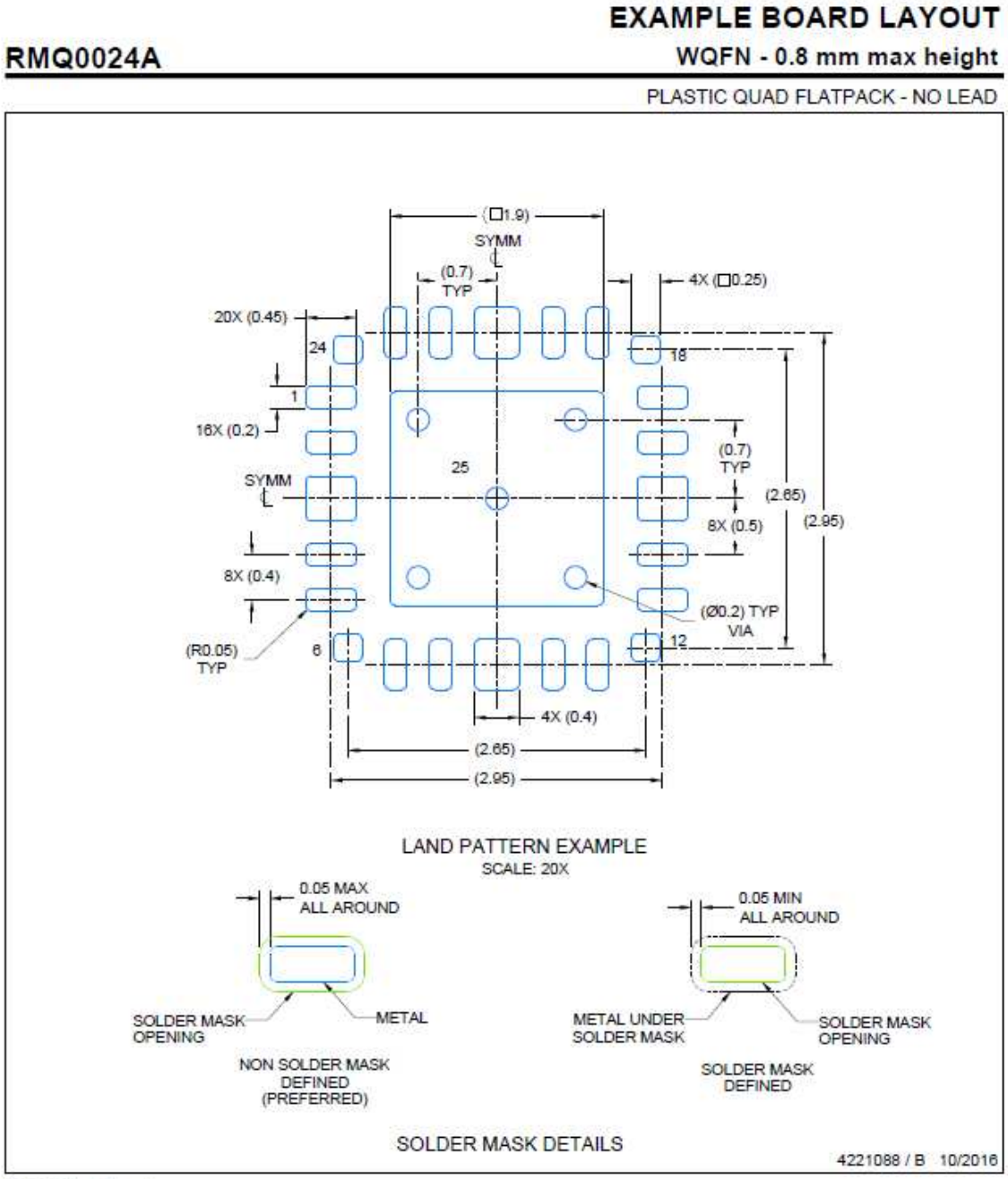


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

Figure 53. DP83825I Package Drawing

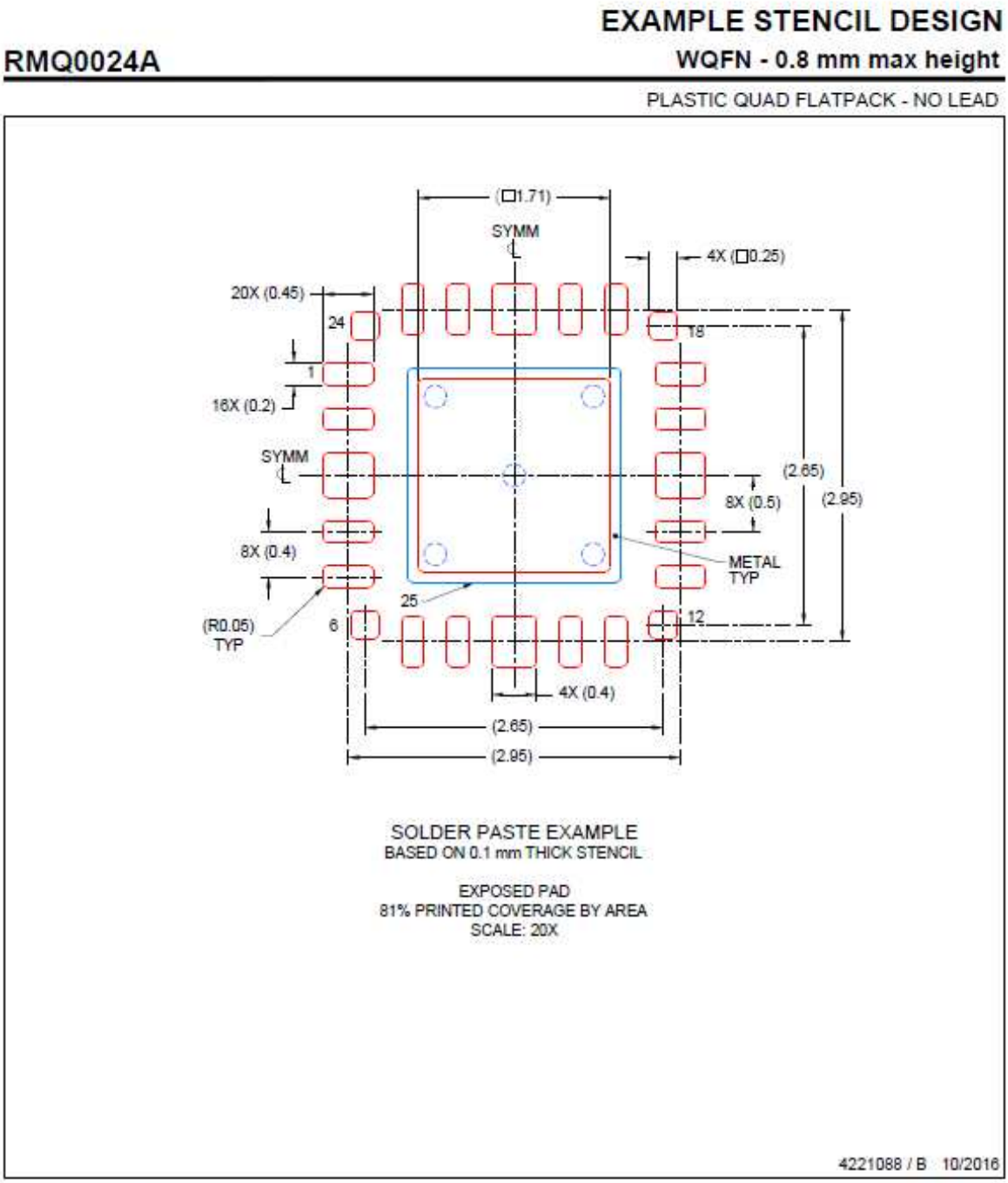


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

Figure 54. DP83825I Package Drawing



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PDP83825IRMQR	ACTIVE	WQFN	RMQ	24	3000	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

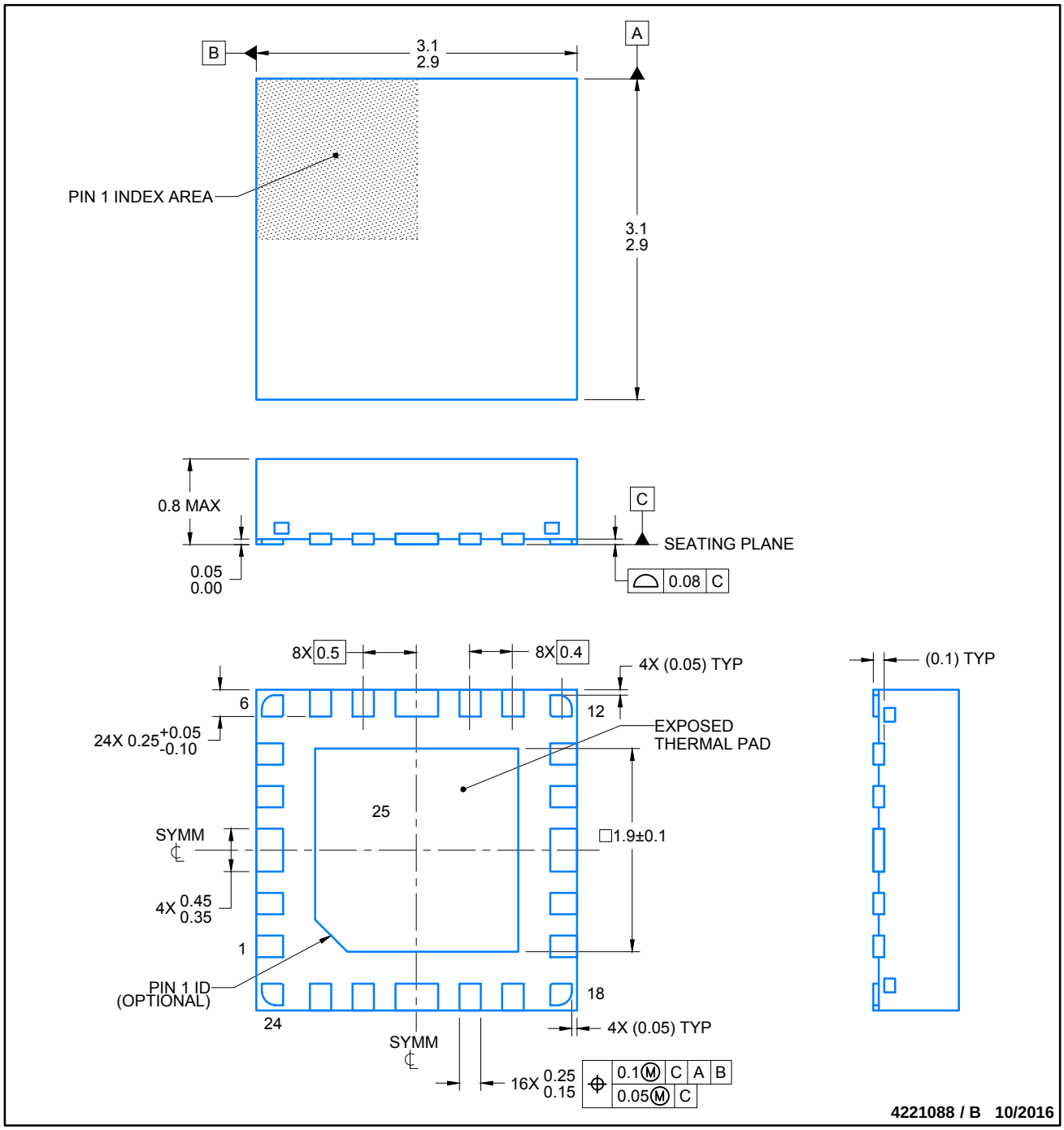
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

RMQ0024A

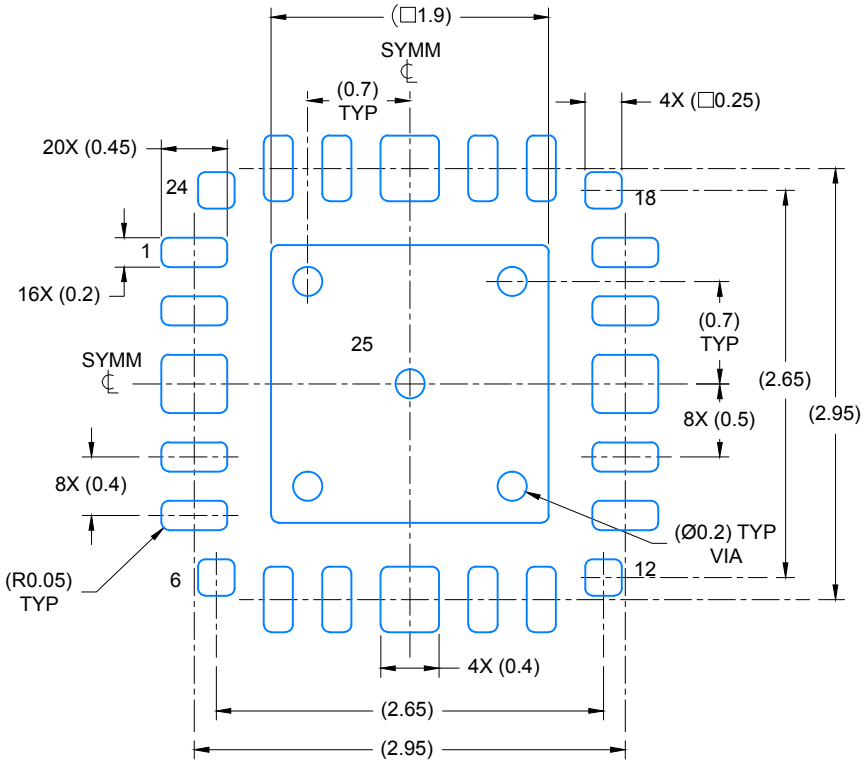
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



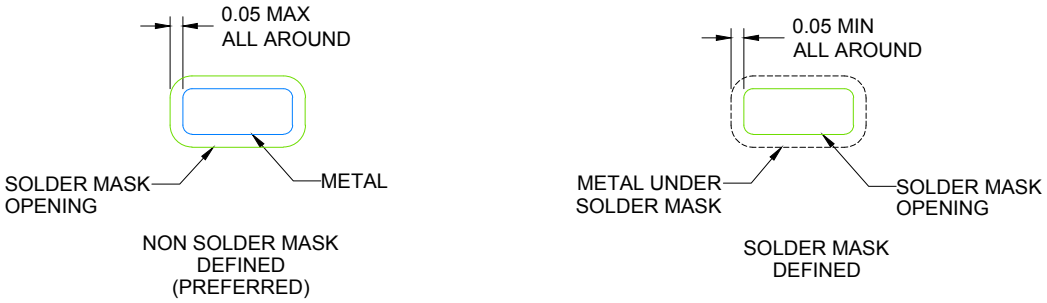
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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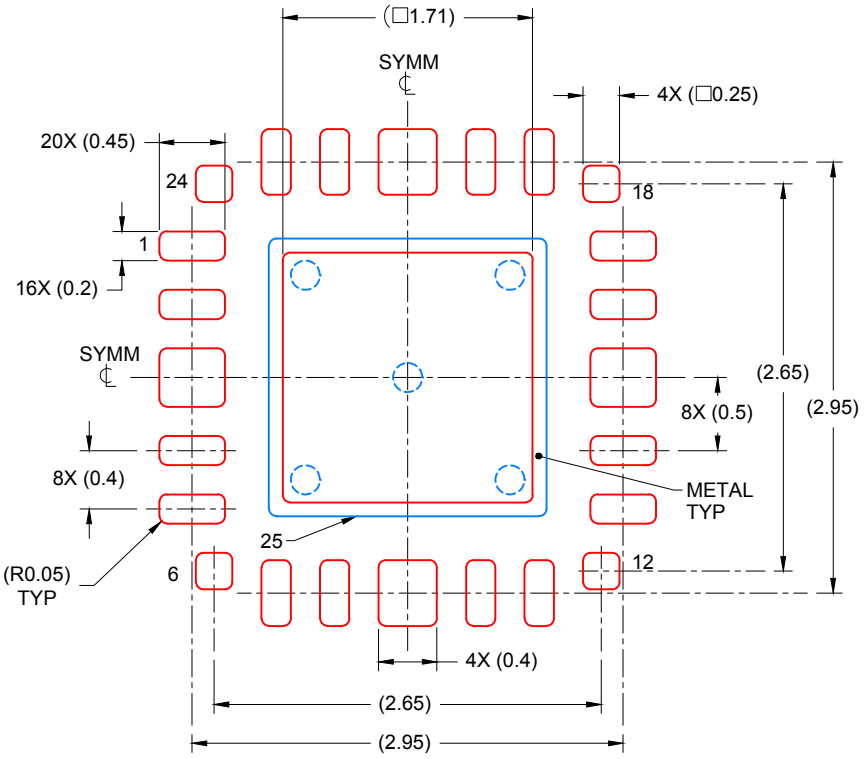
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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