1 Features

- Single H-Bridge PWM Motor Driver
  - Single Brushed-DC Motor Driver
  - 1/2 Bipolar Stepper Motor Driver
- 5-A peak or 3.5-A rms Output Current
- 6.5- to 45-V Operating Supply Voltage Range
- Simple PH/EN Control Interface
- Multiple Decay Modes
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- Low-Current Sleep Mode (10 µA)
- Small Package and Footprint
  - 28 HTSSOP (PowerPAD)

2 Applications

- Automatic Teller and Money Handling Machines
- Video Security Cameras
- Multi-Function Printers and Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation and Robotics
- Stage Lighting Equipment

3 Description

The DRV8829 is a brushed-DC motor or 1/2 bipolar stepper driver for industrial applications. The device output stage consists of an N-channel power MOSFET H-bridge driver. The DRV8829 is capable of driving up to 5-A peak current or 3.5-A rms current (with proper printed-circuit-board ground plane for thermal dissipation and at 24 V and $T_A = 25^\circ C$).

The PH/EN pins provide a simple control interface. An internal sense amplifier allows for adjustable current control. A low-power sleep mode is provided for very low quiescent current standby using a dedicated nSLEEP pin. Current regulation decay mode can be set to slow, fast, or mixed decay.

Protection features are provided for undervoltage, overcurrent, shorts, and overtemperature. Fault conditions are indicated by a nFAULT pin.

### Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV8829</td>
<td>HTSSOP (28)</td>
<td>9.70 mm × 4.40 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
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</tr>
</tbody>
</table>

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision D (June 2015) to Revision E**

- Increased the power supply voltage maximum to 50

**Page**

5

**Changes from Revision C (August 2013) to Revision D**

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section

**Page**

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5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O(1)</th>
<th>DESCRIPTION</th>
<th>EXTERNAL COMPONENTS OR CONNECTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>POWER AND GROUND</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>14, 28</td>
<td>—</td>
<td>Device ground</td>
</tr>
<tr>
<td>VM</td>
<td>4, 11</td>
<td>—</td>
<td>Bridge power supply</td>
</tr>
<tr>
<td>V3P3OUT</td>
<td>15</td>
<td>O</td>
<td>3.3-V regulator output</td>
</tr>
<tr>
<td>CP1</td>
<td>1</td>
<td>IO</td>
<td>Charge pump flying capacitor</td>
</tr>
<tr>
<td>CP2</td>
<td>2</td>
<td>IO</td>
<td>Charge pump flying capacitor</td>
</tr>
<tr>
<td>VCP</td>
<td>3</td>
<td>IO</td>
<td>High-side gate drive voltage</td>
</tr>
<tr>
<td><strong>CONTROL</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ENBL</td>
<td>21</td>
<td>I</td>
<td>Bridge enable</td>
</tr>
<tr>
<td>PHASE</td>
<td>20</td>
<td>I</td>
<td>Bridge phase (direction)</td>
</tr>
<tr>
<td>I0</td>
<td>23</td>
<td>I</td>
<td>Current set inputs</td>
</tr>
<tr>
<td>I1</td>
<td>24</td>
<td>I</td>
<td>Current set inputs</td>
</tr>
<tr>
<td>I2</td>
<td>25</td>
<td>I</td>
<td>Current set inputs</td>
</tr>
<tr>
<td>I3</td>
<td>26</td>
<td>I</td>
<td>Current set inputs</td>
</tr>
<tr>
<td>I4</td>
<td>27</td>
<td>I</td>
<td>Current set inputs</td>
</tr>
<tr>
<td>DECAY</td>
<td>19</td>
<td>I</td>
<td>Decay mode</td>
</tr>
<tr>
<td>nRESET</td>
<td>16</td>
<td>I</td>
<td>Reset input</td>
</tr>
<tr>
<td>nSLEEP</td>
<td>17</td>
<td>I</td>
<td>Sleep mode input</td>
</tr>
<tr>
<td>VREF</td>
<td>12, 13</td>
<td>I</td>
<td>Current set reference input</td>
</tr>
<tr>
<td><strong>STATUS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>nFAULT</td>
<td>18</td>
<td>OD</td>
<td>Fault</td>
</tr>
</tbody>
</table>

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output
### Pin Functions (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O(1)</th>
<th>DESCRIPTION</th>
<th>EXTERNAL COMPONENTS OR CONNECTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISEN</td>
<td>6, 9</td>
<td>IO</td>
<td>Bridge ground / Isense</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Connect to current sense resistor. Both pins must be connected together on the PCB.</td>
</tr>
<tr>
<td>OUT1</td>
<td>5, 10</td>
<td>O</td>
<td>Bridge output 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Connect to motor winding. Both pins must be connected together on the PCB.</td>
</tr>
<tr>
<td>OUT2</td>
<td>7, 8</td>
<td>O</td>
<td>Bridge output 2</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted) (1) (2)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VM</td>
<td>–0.3</td>
<td>50</td>
<td>V</td>
</tr>
<tr>
<td>Digital pin voltage</td>
<td>–0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>VREF</td>
<td>–0.3</td>
<td>4</td>
<td>V</td>
</tr>
<tr>
<td>ISENSE pin voltage</td>
<td>–0.3</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Peak motor drive output current, t &lt; 1 μs</td>
<td>Internally limited</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Continuous motor drive output current(3)</td>
<td>5</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Continuous total power dissipation</td>
<td>See Thermal Information</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TJ</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>TA</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>–60</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th></th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(ESD) Electrostatic discharge</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VM</td>
<td>8.2</td>
<td>45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VREF</td>
<td>1</td>
<td>3.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I3P3</td>
<td>0</td>
<td>1</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>IPWM</td>
<td>0</td>
<td>100</td>
<td>kHz</td>
<td></td>
</tr>
</tbody>
</table>

(1) All VM pins must be connected to the same supply voltage.

(2) Operational at VREF from 0 V to 1 V, but accuracy is degraded.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>DRV8829</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PWP (HTSSOP)</td>
</tr>
<tr>
<td>RθJA</td>
<td>31.6</td>
</tr>
<tr>
<td>RθJC(top)</td>
<td>15.9</td>
</tr>
<tr>
<td>RθJB</td>
<td>5.6</td>
</tr>
<tr>
<td>ψJT</td>
<td>0.2</td>
</tr>
<tr>
<td>ψJB</td>
<td>5.5</td>
</tr>
<tr>
<td>RθJC(bot)</td>
<td>1.4</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
### 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{\text{VM}} )</td>
<td>VM operating supply current ( V_{\text{M}} = 24 , \text{V}, f_{\text{PWM}} &lt; 50 , \text{kHz} )</td>
<td>5</td>
<td>8</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{VMQ}} )</td>
<td>VM sleep mode supply current ( V_{\text{M}} = 24 , \text{V} )</td>
<td>10</td>
<td>20</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{UVLO}} )</td>
<td>VM undervoltage lockout voltage ( V_{\text{M}} ) rising</td>
<td>7.8</td>
<td>8.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{SP3}} )</td>
<td>V3P3OUT voltage ( I_{\text{OUT}} = 0 ) to 1 mA</td>
<td>3.2</td>
<td>3.3</td>
<td>3.4</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{IL}} )</td>
<td>Input low voltage</td>
<td>0.6</td>
<td>0.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{IH}} )</td>
<td>Input high voltage</td>
<td>2.2</td>
<td>5.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{HYS}} )</td>
<td>Input hysteresis</td>
<td>0.3</td>
<td>0.45</td>
<td>0.6</td>
<td>V</td>
</tr>
<tr>
<td>( I_{\text{IL}} )</td>
<td>Input low current ( \text{VIN} = 0 )</td>
<td>–20</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{IH}} )</td>
<td>Input high current ( \text{VIN} = 3.3 , \text{V} )</td>
<td>100</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{PD}} )</td>
<td>Internal pulldown resistance</td>
<td>100</td>
<td></td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{OL}} )</td>
<td>Output low voltage ( I_{O} = 5 , \text{mA} )</td>
<td>0.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{OH}} )</td>
<td>Output high leakage current ( V_{O} = 3.3 , \text{V} )</td>
<td>1</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{IL}} )</td>
<td>Input low threshold voltage ( \text{For slow decay mode} )</td>
<td>0.8</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{IH}} )</td>
<td>Input high threshold voltage ( \text{For fast decay mode} )</td>
<td>2</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{IN}} )</td>
<td>Input current</td>
<td>±40</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{PU}} )</td>
<td>Internal pullup resistance</td>
<td>130</td>
<td></td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{PD}} )</td>
<td>Internal pulldown resistance</td>
<td>80</td>
<td></td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{HS(on)}} )</td>
<td>HS FET on resistance ( V_{\text{M}} = 24 , \text{V}, I_{O} = 1 , \text{A}, T_{J} = 25^\circ \text{C} )</td>
<td>0.1</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{LS(on)}} )</td>
<td>LS FET on resistance ( V_{\text{M}} = 24 , \text{V}, I_{O} = 1 , \text{A}, T_{J} = 85^\circ \text{C} )</td>
<td>0.13</td>
<td>0.16</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{OFF}} )</td>
<td>Off-state leakage current</td>
<td>–40</td>
<td>40</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{PWM}} )</td>
<td>Internal current control PWM frequency</td>
<td>50</td>
<td></td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{BLANK}} )</td>
<td>Current sense blanking time</td>
<td>3.75</td>
<td></td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{R}} )</td>
<td>Rise time</td>
<td>30</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{F}} )</td>
<td>Fall time</td>
<td>30</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{OPC}} )</td>
<td>Overcurrent protection trip level</td>
<td>6</td>
<td>6</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>( T_{\text{SD}} )</td>
<td>Thermal shutdown temperature Die temperature</td>
<td>150</td>
<td>160</td>
<td>180</td>
<td>°C</td>
</tr>
<tr>
<td>( I_{\text{REF}} )</td>
<td>VREF input current ( \text{VREF} = 3.3 , \text{V} )</td>
<td>–3</td>
<td>3</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{TRIP}} )</td>
<td>ISENSE trip voltage ( \text{VREF} = 3.3 , \text{V}, 100% \text{ current setting} )</td>
<td>635</td>
<td>660</td>
<td>685</td>
<td>mV</td>
</tr>
<tr>
<td>( \Delta I_{\text{TRIP}} )</td>
<td>Current trip accuracy (relative to programmed value) ( \text{VREF} = 3.3 , \text{V}, 5% - 34% \text{ current setting} )</td>
<td>–15%</td>
<td>15%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( A_{\text{ISENSE}} )</td>
<td>Current sense amplifier gain Reference only</td>
<td>5</td>
<td></td>
<td>V/V</td>
<td></td>
</tr>
</tbody>
</table>
6.6 Typical Characteristics

Figure 1. Active Supply Current Over Supply Voltage and Temperature

Figure 2. Sleep Current Over Supply Voltage and Temperature
7 Detailed Description

7.1 Overview

The DRV8829 is an integrated motor driver solution for bipolar stepper motors or single/dual brushed-DC motors. The device integrates an NMOS H-bridge and current regulation circuitry. The DRV8829 can be powered with a supply voltage from 8.2 to 45 V, and is capable of providing an output current up to 5-A peak or 3.5-A rms. Actual operable rms current will depend on ambient temperature, supply voltage, and PCP ground plane size.

A simple PH/EN interface allows easy interfacing to the controller circuit.

The current regulation is highly configurable, with several decay modes of operation. The decay mode can be selected as a fixed slow, mixed, or fast decay.

A current scalar feature allows the controller to scale the output current without needing to scale the analog reference voltage input VREF. The DAC is accessed using digital input pins. This allows the controller to save power by decreasing the current consumption when not required.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 PWM Motor Drivers

The DRV8829 contains one H-bridge motor driver with current-control PWM circuitry. Figure 3 shows a block diagram of the motor control circuitry. A bipolar stepper motor is shown, but the driver can also drive a DC motor.

![Figure 3. Motor Control Circuitry](image)

There are multiple VM, ISEN, OUT, and VREF pins. All like-named pins must be connected together on the PCB.

7.3.2 Blanking Time

After the current is enabled in the H-bridge, the voltage on the ISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 μs. The blanking time also sets the minimum on time of the PWM.

7.3.3 nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge drivers. All inputs are ignored while nRESET is active.

Driving nSLEEP low will put the device into a low-power sleep state. In this state, the H-bridge is disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational. The nRESET and nSLEEP have internal pulldown resistors of approximately 100 kΩ. These signals need to be driven to logic high for device operation.

7.3.4 Protection Circuits

The DRV8829 is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.4.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The device will remain disabled until either nRESET pin is applied, or VM is removed and re-applied.

Overcurrent conditions on both high and low side devices; that is, a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. The overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the $I_{SENSE}$ resistor value or VREF voltage.
Feature Description (continued)

7.3.4.2 Thermal Shutdown (TSD)
If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

7.3.4.3 Undervoltage Lockout (UVLO)
If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

7.3.5 Current Regulation
The current through the motor winding is regulated by a fixed-frequency PWM current regulation, or current chopping. When the H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

For stepping motors, current regulation is normally used at all times, and changing the current can be used to microstep the motor. For DC motors, current regulation is used to limit the start-up and stall current of the motor.

If the current regulation feature is not needed, it can be disabled by connecting the ISENSE pins directly to ground and the VREF pins to V3P3.

The PWM chopping current in each bridge is set by a comparator which compares the voltage across a current sense resistor connected to the ISEN pin, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF pins, and is scaled by a 5-bit DAC that allows current settings of zero to 100% in an approximately sinusoidal sequence.

The full-scale (100%) chopping current is calculated in Equation 1.

\[ I_{CHOP} = \frac{V_{REFX}}{5 \cdot R_{SENSE}} \]  

Example:
If a 0.25-Ω sense resistor is used and the VREFx pin is 2.5 V, the full-scale (100%) chopping current will be 2.5 V / (5 × 0.25 Ω) = 2 A.

Five input pins (I0 - I4) are used to scale the current in the bridge as a percentage of the full-scale current set by the VREF input pin and sense resistance. The I0 - I4 pins have internal pulldown resistors of approximately 100 kΩ. The function of the pins is shown in Table 1.

<table>
<thead>
<tr>
<th>I[4..0]</th>
<th>RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00h</td>
<td>0% (Bridge disabled)</td>
</tr>
<tr>
<td>0x01h</td>
<td>5%</td>
</tr>
<tr>
<td>0x02h</td>
<td>10%</td>
</tr>
<tr>
<td>0x03h</td>
<td>15%</td>
</tr>
<tr>
<td>0x04h</td>
<td>20%</td>
</tr>
<tr>
<td>0x05h</td>
<td>24%</td>
</tr>
<tr>
<td>0x06h</td>
<td>29%</td>
</tr>
<tr>
<td>0x07h</td>
<td>34%</td>
</tr>
<tr>
<td>0x08h</td>
<td>38%</td>
</tr>
<tr>
<td>0x09h</td>
<td>43%</td>
</tr>
<tr>
<td>0x0Ah</td>
<td>47%</td>
</tr>
<tr>
<td>0x0Bh</td>
<td>51%</td>
</tr>
<tr>
<td>0x0Ch</td>
<td>56%</td>
</tr>
</tbody>
</table>
Table 1. Current Scalar Logic (continued)

<table>
<thead>
<tr>
<th>I[4..0]</th>
<th>RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0Dh</td>
<td>60%</td>
</tr>
<tr>
<td>0x0Eh</td>
<td>63%</td>
</tr>
<tr>
<td>0x0Fh</td>
<td>67%</td>
</tr>
<tr>
<td>0x10h</td>
<td>71%</td>
</tr>
<tr>
<td>0x11h</td>
<td>74%</td>
</tr>
<tr>
<td>0x12h</td>
<td>77%</td>
</tr>
<tr>
<td>0x13h</td>
<td>80%</td>
</tr>
<tr>
<td>0x14h</td>
<td>83%</td>
</tr>
<tr>
<td>0x15h</td>
<td>86%</td>
</tr>
<tr>
<td>0x16h</td>
<td>88%</td>
</tr>
<tr>
<td>0x17h</td>
<td>90%</td>
</tr>
<tr>
<td>0x18h</td>
<td>92%</td>
</tr>
<tr>
<td>0x19h</td>
<td>94%</td>
</tr>
<tr>
<td>0x1Ah</td>
<td>96%</td>
</tr>
<tr>
<td>0x1Bh</td>
<td>97%</td>
</tr>
<tr>
<td>0x1Ch</td>
<td>98%</td>
</tr>
<tr>
<td>0x1Dh</td>
<td>99%</td>
</tr>
<tr>
<td>0x1 Eh</td>
<td>100%</td>
</tr>
<tr>
<td>0x1Fh</td>
<td>100%</td>
</tr>
</tbody>
</table>

7.4 Device Functional Modes

7.4.1 Bridge Control

The PHASE input pin controls the direction of current flow through the H-bridge. The ENBL input pin enables the H-bridge outputs when active high. Table 2 shows the logic.

Table 2. H-Bridge Logic

<table>
<thead>
<tr>
<th>ENBL</th>
<th>PHASE</th>
<th>OUT1</th>
<th>OUT2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>Z</td>
<td>Z</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>L</td>
<td>H</td>
</tr>
</tbody>
</table>

The control inputs have internal pulldown resistors of approximately 100 kΩ.

7.4.2 Decay Mode

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 4 as case 1. The current flow direction shown indicates the state when the PHASE pin is high.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 4 as case 2.

In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge. This is shown in Figure 4 as case 3.
The DRV8829 supports fast decay, slow decay and a mixed decay mode. Slow, fast, or mixed decay mode is selected by the state of the DECAY pin - logic low selects slow decay, open selects mixed decay operation, and logic high sets fast decay mode. The DECAY pin has both an internal pullup resistor of approximately 130 kΩ and an internal pulldown resistor of approximately 80 kΩ. This sets the mixed decay mode if the pin is left open or undriven.

Mixed decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The DRV8829 is used in brushed motor or stepper control.

8.2 Typical Application
In this application, the DRV8829 will be used to drive a brushed-DC motor. The following design procedure can be used to configure the DRV8829.

![Typical Application Schematic](image)

Figure 5. Typical Application Schematic

8.2.1 Design Requirements
Table 3 gives design input parameters for system design.

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>REFERENCE</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>VM</td>
<td>24 V</td>
</tr>
<tr>
<td>Motor winding resistance</td>
<td>R_L</td>
<td>0.83 Ω</td>
</tr>
<tr>
<td>Motor winding inductance</td>
<td>L_L</td>
<td>232.5 µH</td>
</tr>
<tr>
<td>Target chopping current</td>
<td>I_TRIP</td>
<td>3.5 A</td>
</tr>
</tbody>
</table>
8.2.2 Detailed Design Procedure

The maximum current \(I_{\text{TRIP}}\) is set by the Ix pins, the VREF analog voltage, and the sense resistor value \(R_{\text{SENSE}}\). When starting a brushed-DC motor, a large inrush current may occur because there is no back-EMF. Current regulation will act to limit this inrush current and prevent high current on start-up.

\[
I_{\text{CHOP}} = \frac{V_{\text{REFX}}}{5 \cdot R_{\text{SENSE}}}
\]  

(2)

**Example:** If the desired chopping current is 3.5 A

- Set \(R_{\text{SENSE}} = 100 \text{ m\Omega}\)
- VREF would have to be 1.75 V.
- Create a resistor divider from V3P3OUT (3.3 V) to set VREF ≈ 1.75 V.
- Set \(R2 = 18 \text{ k\Omega}\), set \(R1 = 16 \text{ k\Omega}\)

8.2.2.1 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals \(I_{\text{rms}}^2 \times R\). For example, if the rms motor current is 2-A and a 100-m\(\Omega\) sense resistor is used, the resistor will dissipate \(2 \text{ A}^2 \times 0.1 \text{ \Omega} = 0.4 \text{ W}\). The power quickly increases with greater current levels.

Resistors typically have a rated power within some ambient temperature range, along with a de-rated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.
8.2.3 Application Curves

Figure 6. Motor Start-up without Current Regulation, Overcurrent Trips

Figure 7. Motor Start-up With Current Regulation

Figure 8. Motor Start-up With Current Regulation, Motor Reaches Steady State
9 Power Supply Recommendations

The DRV8829 is designed to operate from an input voltage supply (VM) range from 8.2 V to 45 V. The device has an absolute maximum rating of 47 V. A 0.1-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the DRV8829 as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply’s capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The motor braking method.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be greater than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

![Figure 9. Setup of Motor Drive System With External Power Supply](image-url)
10 Layout

10.1 Layout Guidelines

Each VM terminal must be bypassed to GND using a low-ESR ceramic bypass capacitors with recommended values of 0.1 μF rated for VM. These capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component may be an electrolytic.

A low-ESR ceramic capacitor must be placed in between the CP1 and CP2 pins. TI recommends a value of 0.1 μF rated for VM. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 0.47 μF rated for 16 V. Place this component as close to the pins as possible. In addition, place a 1 MΩ between VM and VCP.

Bypass V3P3OUT to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

The current sense resistor should be placed as close as possible to the device pins to minimize trace inductance between the pin and resistor.

10.2 Layout Example

Figure 10. Example Layout
10.3 Thermal Considerations
The DRV8829 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.4 Power Dissipation
Power dissipation in the DRV8829 is dominated by the power dissipated in the output FET resistance, or \( R_{DS(ON)} \). Average power dissipation when running a stepper motor can be roughly estimated by Equation 3.

\[
P_{TOT} (W) = \left[ R_{DS(ON),HS} (\Omega) + R_{DS(ON),LS} (\Omega) \right] \times [I_{OUT(RMS)} (A)]^2
\]

where
- \( P_{TOT} \) is the total power dissipation
- \( R_{DS(ON)} \) is the resistance of each FET (high-side and low-side)
- \( I_{OUT(RMS)} \) is the RMS output current being applied to each winding

\( I_{OUT(RMS)} \) is equal to the approximately 0.7x the full-scale output current setting.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

\( R_{DS(ON)} \) increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

10.4.1 Heatsinking
The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.


In general, the more copper area that can be provided, the more power can be dissipated.
11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

**SLYZ022 — TI Glossary.**
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV8829PWP</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>28</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>DRV8829</td>
<td>Samples</td>
</tr>
<tr>
<td>DRV8829PWPR</td>
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<td>HTSSOP</td>
<td>PWP</td>
<td>28</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>DRV8829</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "]~[“ will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV8829PWPR</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>28</td>
<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>6.9</td>
<td>10.2</td>
<td>1.8</td>
<td>12.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
## TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV8829PWPR</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>28</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
5. Features may differ or may not be present.

PowerPAD is a trademark of Texas Instruments.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12. Board assembly site may have different recommendations for stencil design.
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