FEATURES

- Single +3.3 V Supply
- LVDS Receiver Inputs Accept LVPECL Signals
- TRI-STATE Outputs
- Receiver Input Threshold < ±100 mV
- Fast Propagation Delay of 1.4 ns (Typ)
- Low Jitter 800 Mbps Fully Differential Data Path
- 100 ps (Typ) of pk-pk Jitter with PRBS = 2^{23−1}
  Data Pattern at 800 Mbps
- Compatible with ANSI/TIA/EIA-644-A LVDS Standard
- 8 pin SOIC and Space Saving (70%) WSON Package
- Industrial Temperature Range

DESCRIPTION

The DS90LV001 LVDS-LVDS Buffer takes an LVDS input signal and provides an LVDS output signal. In many large systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the "stub length" or the distance between the transmission line and the unterminated receivers on individual cards. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns often make it difficult to make the stubs as short as the designer would like.

The DS90LV001, available in the WSON package, will allow the receiver to be placed very close to the main transmission line, thus improving system performance.

A wide input dynamic range will allow the DS90LV001 to receive differential signals from LVPECL as well as LVDS sources. This will allow the device to also fill the role of an LVPECL-LVDS translator.

An output enable pin is provided, which allows the user to place the LVDS output in TRI-STATE.

The DS90LV001 is offered in two package options, an 8 pin WSON and SOIC.
Absolute Maximum Ratings\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V_{CC})</td>
<td>(-0.3)V</td>
<td>+4V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>LVCMOS/LVTTL Input Voltage (EN)</td>
<td>(-0.3)V to (+0.3)V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVDS Receiver Input Voltage (IN+, IN−)</td>
<td>(-0.3)V to +4V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVDS Driver Output Voltage (OUT+, OUT−)</td>
<td>(-0.3)V to +4V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVDS Output Short Circuit Current</td>
<td>Continuous</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>(-65°C) to +150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature Range Soldering (4 sec.)</td>
<td>+260°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Package Power Dissipation at 25°C</td>
<td>726 mW</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Derate D Package</td>
<td>5.8 mW/°C</td>
<td></td>
<td>+25°C</td>
<td></td>
</tr>
<tr>
<td>NGK Package</td>
<td>2.44 W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Derate NGK Package</td>
<td>19.49 mW/°C</td>
<td></td>
<td>+25°C</td>
<td></td>
</tr>
<tr>
<td>ESD Ratings ((HBM, 1.5,\text{kΩ}, 100pF))</td>
<td>(\geq2.5)kV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>((\text{EIAJ}, 0,\text{kΩ}, 200pF))</td>
<td>(\geq250)V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V_{CC})</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Receiver Input Voltage</td>
<td>0</td>
<td>(V_{CC})</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Operating Free Air Temperature</td>
<td>(-40)</td>
<td>+25</td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>
## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVCMOS/LVTTL DC SPECIFICATIONS (EN)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage</td>
<td>$V_{IN} = 3.6,\text{V or } 2.0,\text{V, } V_{CC} = 3.6,\text{V}$</td>
<td>2.0</td>
<td>$V_{CC}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage</td>
<td>GND</td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High Level Input Current</td>
<td>$V_{IN} = 3.6,\text{V or } 2.0,\text{V, } V_{CC} = 3.6,\text{V}$</td>
<td>+7</td>
<td>+20</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low Level Input Current</td>
<td>$V_{IN} = \text{GND or } 0.8,\text{V, } V_{CC} = 3.6,\text{V}$</td>
<td>±1</td>
<td>±10</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$I_{CL}$</td>
<td>Input Clamp Voltage</td>
<td>$I_{CL} = -18,\text{mA}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| LVDS OUTPUT DC SPECIFICATIONS (OUT) | | | | | | |
| $V_{OD}$ | Differential Output Voltage | $R_{L} = 100\,\Omega$ | 250 | 325 | 450 | mV |
| $\Delta V_{OD}$ | Change in Magnitude of $V_{OD}$ for Complimentary Output States | | 20 | mV | | |
| $V_{OS}$ | Offset Voltage | $R_{L} = 100\,\Omega$ | 1.080 | 1.19 | 1.375 | V |
| $\Delta V_{OS}$ | Change in Magnitude of $V_{OS}$ for Complimentary Output States | | 20 | mV | | |
| $I_{OZ}$ | Output TRI-STATE Current | EN = $0\,\text{V, } V_{OUT} = V_{CC}$ or GND | ±1 | ±10 | μA | |
| $I_{OFF}$ | Power-Off Leakage Current | $V_{CC} = 0\,\text{V, } V_{OUT} = 3.6\,\text{V or } GND$ | ±1 | ±10 | μA | |
| $I_{OS}$ | Output Short Circuit Current(3) | EN = $V_{CC}, V_{OUT+}$ and $V_{OUT-} = 0\,\text{V}$ | -16 | -24 | mA | |
| $I_{OSD}$ | Differential Output Short Circuit Current(3) | EN = $V_{CC}, V_{OD} = 0\,\text{V}$ | -7 | -12 | mA | |

| LVDS RECEIVER DC SPECIFICATIONS (IN) | | | | | | |
| $V_{TH}$ | Differential Input High Threshold | $V_{CM} = +0.05\,\text{V, } +1.2\,\text{V or } +3.25\,\text{V}$ | 0 | +100 | mV | |
| $V_{TL}$ | Differential Input Low Threshold | | -100 | 0 | mV | |
| $V_{DMR}$ | Common Mode Voltage Range | $V_{ID} = 100\,\text{mV, } V_{CC} = 3.3\,\text{V}$ | 0.05 | 3.25 | V | |
| $I_{IN}$ | Input Current | $V_{IN} = +3.0\,\text{V}$ | $V_{CC} = 3.6\,\text{V or } 0\,\text{V}$ | ±1 | ±10 | μA | |
| | | $V_{IN} = 0\,\text{V}$ | $V_{CC} = 3.6\,\text{V or } 0\,\text{V}$ | ±1 | ±10 | μA | |
| $\Delta I_{IN}$ | Change in Magnitude of $I_{IN}$ | $V_{IN} = +3.0\,\text{V}$ | $V_{CC} = 3.6\,\text{V or } 0\,\text{V}$ | 1 | 6 | μA | |
| | | $V_{IN} = 0\,\text{V}$ | | 1 | 6 | μA | |

| SUPPLY CURRENT | | | | | | |
| $I_{CCD}$ | Total Supply Current | $EN = V_{CC}, R_{L} = 100\,\Omega, C_{L} = 5\,\text{pF}$ | 47 | 70 | mA | |
| $I_{CCZ}$ | TRI-STATE Supply Current | EN = $0\,\text{V}$ | 22 | 35 | mA | |

1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except $V_{OD}$ and $\Delta V_{OD}$.
2. All typical are given for $V_{CC} = +3.3\,\text{V}$ and $T_{A} = +25\,^\circ\text{C}$, unless otherwise stated.
3. Output short circuit current ($I_{OS}$) is specified as magnitude only, minus sign indicates direction only.
## AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPHLD</td>
<td>Differential Propagation Delay High to Low</td>
<td>$R_L = 100\Omega, \ C_L = 5\ pF$ Figure 4 and Figure 5</td>
<td>1.0</td>
<td>1.4</td>
<td>2.0</td>
<td>ns</td>
</tr>
<tr>
<td>TPLHD</td>
<td>Differential Propagation Delay Low to High</td>
<td>$R_L = 100\Omega, \ C_L = 5\ pF$ Figure 4 and Figure 5</td>
<td>1.0</td>
<td>1.4</td>
<td>2.0</td>
<td>ns</td>
</tr>
<tr>
<td>TSKD1</td>
<td>Pulse Skew $</td>
<td>T_{PLHD} - T_{PHLD}</td>
<td>$</td>
<td>0</td>
<td>20</td>
<td>60</td>
</tr>
<tr>
<td>TSKD2</td>
<td>Part to Part Skew</td>
<td>200</td>
<td>400</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSKD3</td>
<td>Part to Part Skew</td>
<td>200</td>
<td>400</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSKD4</td>
<td>Part to Part Skew</td>
<td>200</td>
<td>400</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TLH</td>
<td>Rise Time</td>
<td>$R_L = 100\Omega, \ C_L = 5\ pF$ Figure 4 and Figure 6</td>
<td>200</td>
<td>320</td>
<td>450</td>
<td>ps</td>
</tr>
<tr>
<td>TIL</td>
<td>Fall Time</td>
<td>Figure 4 and Figure 6</td>
<td>200</td>
<td>310</td>
<td>450</td>
<td>ps</td>
</tr>
<tr>
<td>TPHZ</td>
<td>Disable Time (Active High to Z)</td>
<td>$R_L = 100\Omega, \ C_L = 5\ pF$ Figure 7 and Figure 8</td>
<td>3</td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TPLZ</td>
<td>Disable Time (Active Low to Z)</td>
<td>3</td>
<td>25</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPZH</td>
<td>Enable Time (Z to Active High)</td>
<td>25</td>
<td>45</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPZL</td>
<td>Enable Time (Z to Active Low)</td>
<td>25</td>
<td>45</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TDJ</td>
<td>LVDS Data Jitter, Deterministic (Peak-to-Peak)</td>
<td>$V_{ID} = 300\text{mV}; \ PRBS = 2^{23} - 1 \text{ data}; \ V_{CM} = 1.2\text{V at } 800\text{Mbps (NRZ)}$</td>
<td>100</td>
<td>135</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>TRJ</td>
<td>LVDS Clock Jitter, Random</td>
<td>$V_{ID} = 300\text{mV}; \ V_{CM} = 1.2\text{V at } 400\text{MHz clock}$</td>
<td>2.2</td>
<td>3.5</td>
<td>ps</td>
<td></td>
</tr>
</tbody>
</table>

(1) All typical are given for $V_{CC} = +3.3\text{V}$ and $T_A = +25^\circ\text{C}$, unless otherwise stated.

(2) The parameters are ensured by design. The limits are based on statistical analysis of the device performance over the PVT (process, voltage and temperature) range.

(3) $t_{SKD1}$, $t_{PLHD} - t_{PHLD}$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

(4) $t_{SKD2}$, Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same $V_{CC}$ and within 5°C of each other within the operating temperature range.

(5) $t_{SKD4}$, Part to Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. $t_{SKD4}$ is defined as $|Max - Min|$ differential propagation delay.

(6) The parameters are ensured by design. The limits are based on statistical analysis of the device performance over the PVT range with the following test equipment setup: HP8133A (pattern pulse generator), 5 feet of RG142B cable with DUT test board and HP83480A (digital scope mainframe) with HP83484A (50GHz scope module). The HP8133A with RG142B cable exhibit a $t_{DJ} = 21\text{ps}$ and $t_{RJ} = 1.8\text{ps}$.
DC Test Circuits

Figure 2. Differential Driver DC Test Circuit

Figure 3. Differential Driver Full Load DC Test Circuit

AC Test Circuits and Timing Diagrams

Figure 4. LVDS Output Load

Figure 5. Propagation Delay Low-to-High and High-to-Low
Figure 6. LVDS Output Transition Time

Figure 7. TRI-STATE Delay Test Circuit

Figure 8. Output active to TRI-STATE and TRI-STATE to active output time
DS90LV001 Pin Descriptions (SOIC and WSON)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin #</th>
<th>Input/Output</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>1</td>
<td>P</td>
<td>Ground</td>
</tr>
<tr>
<td>IN –</td>
<td>2</td>
<td>I</td>
<td>Inverting receiver LVDS input pin</td>
</tr>
<tr>
<td>IN+</td>
<td>3</td>
<td>I</td>
<td>Non-inverting receiver LVDS input pin</td>
</tr>
<tr>
<td>NC</td>
<td>4</td>
<td></td>
<td>No Connect</td>
</tr>
<tr>
<td>VCC</td>
<td>5</td>
<td>P</td>
<td>Power Supply, 3.3V ± 0.3V.</td>
</tr>
<tr>
<td>OUT+</td>
<td>6</td>
<td>O</td>
<td>Non-inverting driver LVDS output pin</td>
</tr>
<tr>
<td>OUT -</td>
<td>7</td>
<td>O</td>
<td>Inverting driver LVDS output pin</td>
</tr>
<tr>
<td>EN</td>
<td>8</td>
<td>I</td>
<td>Enable pin. When EN is LOW, the driver is disabled and the LVDS outputs are in TRI-STATE. When EN is HIGH, the driver is enabled. LVCMOS/LVTTL levels.</td>
</tr>
<tr>
<td>DAP</td>
<td>NA</td>
<td>NA</td>
<td>Die Attach Pad or DAP (WSON Package only). The DAP is NOT connected to the device GND nor any other pin. It is still recommended to connect the DAP to a GND plane of a PCB for enhanced heat dissipation.</td>
</tr>
</tbody>
</table>

Typical Applications

Backplane Stub-Hider Application

Cable Repeater Application
APPLICATION INFORMATION

MODE OF OPERATION

The DS90LV001 can be used as a "stub-hider." In many systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the "stub length" or the distance between the transmission line and the unterminated receivers on the individual cards. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns and PCB designs often make it difficult to make the stubs as short as the designer would like. The DS90LV001, available in the WSON package, can improve system performance by allowing the receiver to be placed very close to the main transmission line either on the backplane itself or very close to the connector on the card. Longer traces to the LVDS receiver may be placed after the DS90LV001. This very small WSON package is a 75% space savings over the SOIC package.

INPUT FAILSAFE

The receiver inputs of the DS90LV001 do not have internal failsafe biasing. For point-to-point and multidrop applications with a single source, failsafe biasing may not be required. When the driver is off, the link is inactive. If failsafe biasing is required, this can be accomplished with external high value resistors. Using the equations in the LVDS Owner’s Manual Chapter 4, the IN+ should be pull to V_{CC} (3.3V) with 20kΩ and the IN− should be pull to GND with 12kΩ. This provides a slight positive differential bias, and sets a known HIGH state on the link with a minimum amount of distortion.

PCB LAYOUT AND POWER SYSTEM BYPASS

Circuit board layout and stack-up for the DS90LV001 should be designed to provide noise-free power to the device. Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range 0.01 µF to 0.1 µF. Tantalum capacitors may be in the range 2.2 µF to 10 µF. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. It is recommended practice to use two vias at each power pin of the DS90LV001 as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components.
The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity on signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line or the thickness of the dielectric separating the transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

There are more common practices which should be followed when designing PCBs for LVDS signaling. Please see application note AN-1108 for guidelines. In addition, application note AN-1187 has additional information specifically related to WSON recommendations.
Typical Performance Curves

Output High Voltage vs Power Supply Voltage

\[ V_{OH} \text{ - Output High Voltage (V)} \]
\[ V_{CC} \text{ - Power Supply Voltage (V)} \]

\[ T_A = 25^\circ C \]
\[ \text{Load} = 100\Omega \]

Figure 9.

Output Low Voltage vs Power Supply Voltage

\[ V_{OL} \text{ - Output Low Voltage (V)} \]
\[ V_{CC} \text{ - Power Supply Voltage (V)} \]

\[ T_A = 25^\circ C \]
\[ \text{Load} = 100\Omega \]

Figure 10.

Output Short Circuit Current vs Power Supply Voltage

\[ I_{OS} \text{ - Output Short Circuit Current (mA)} \]
\[ V_{CC} \text{ - Power Supply Voltage (V)} \]

\[ T_A = 25^\circ C \]
\[ V_{IN} = V_{CC} \text{ or GND} \]

Figure 11.

Differential Output Short Circuit Current vs Power Supply Voltage

\[ I_{OSD} \text{ - Differential Output Short Circuit Current (mA)} \]
\[ V_{CC} \text{ - Power Supply Voltage (V)} \]

\[ T_A = 25^\circ C \]
\[ V_{IN} = V_{CC} \text{ or GND} \]

Figure 12.

Output TRI-STATE Current vs Power Supply Voltage

\[ I_{O} \text{ - Output TRI-STATE Current (mA)} \]
\[ V_{CC} \text{ - Power Supply Voltage (V)} \]

\[ T_A = 25^\circ C \]
\[ V_{IN} = V_{CC} \text{ or GND} \]

Figure 13.

Offset Voltage vs Power Supply Voltage

\[ V_{OS} \text{ - Offset Voltage (V)} \]
\[ V_{CC} \text{ - Power Supply Voltage (V)} \]

\[ T_A = 25^\circ C \]
\[ R_L = 100\Omega \]

Figure 14.
Typical Performance Curves (continued)

Figure 15. Differential Output Voltage vs Power Supply Voltage

Figure 16. Differential Output Voltage vs Load Resistor

Figure 17. Power Supply Current vs Frequency

Figure 18. Power Supply Current vs Power Supply Voltage

Figure 19. TRI-STATE Power Supply Current vs Power Supply Voltage

Figure 20. Differential Transition Voltage vs Power Supply Voltage
Typical Performance Curves (continued)

Differential Propagation Delay vs Power Supply Voltage

![Graph](Figure 21)

$V_{CC}$ - Power Supply Voltage (V)

$\tau_{PLH0}$, $\tau_{PHL0}$ - Differential Propagation Delay (ns)

- $T_A = 25^\circ C$
- $Freq = 100$ MHz
- $V_{ID} = 200$ mV
- $C_L = 5$ pF
- $R_L = 100$ $\Omega$

Differential Propagation Delay vs Ambient Temperature

![Graph](Figure 22)

$V_{CC}$ - Power Supply Voltage (V)

$\tau_{PHL0}$, $\tau_{PLH0}$ - Differential Propagation Delay (ns)

- $V_{CC} = 3.3$ V
- $Freq = 100$ MHz
- $V_{ID} = 200$ mV
- $C_L = 5$ pF
- $R_L = 100$ $\Omega$

Differential Skew vs Power Supply Voltage

![Graph](Figure 23)

$V_{CC}$ - Power Supply Voltage (V)

$\delta_{SK01}$ - Differential Skew (ps)

- $T_A = 25^\circ C$
- $Freq = 100$ MHz
- $V_{ID} = 200$ mV
- $C_L = 5$ pF
- $R_L = 100$ $\Omega$

Differential Skew vs Ambient Temperature

![Graph](Figure 24)

$V_{CC}$ - Power Supply Voltage (V)

$\delta_{SK01}$ - Differential Skew (ps)

- $V_{CC} = 3.3$ V
- $Freq = 100$ MHz
- $V_{ID} = 200$ mV
- $C_L = 5$ pF
- $R_L = 100$ $\Omega$

Transition Time vs Power Supply Voltage

![Graph](Figure 25)

$V_{CC}$ - Power Supply Voltage (V)

$\tau_{TLH}$, $\tau_{THL}$, $\tau_{TLH}^{-\tau_{THL}}$ - Transition Time (ps)

- $T_A = 25^\circ C$
- $Freq = 100$ MHz
- $V_{ID} = 200$ mV
- $C_L = 5$ pF
- $R_L = 100$ $\Omega$

Transition Time vs Ambient Temperature

![Graph](Figure 26)

$T_A$ - Ambient Temperature (°C)

$\tau_{TLH}$, $\tau_{THL}$, $\tau_{TLH}^{-\tau_{THL}}$ - Transition Time (ps)

- $V_{CC} = 3.3$ V
- $Freq = 100$ MHz
- $V_{ID} = 200$ mV
- $C_L = 5$ pF
- $R_L = 100$ $\Omega$
Typical Performance Curves (continued)

**Differential Propagation Delay vs Differential Input Voltage**

![Figure 27.](image1)

**Differential Propagation Delay vs Common-Mode Voltage**

![Figure 28.](image2)

**Peak-to-Peak Output Jitter at \(V_{CM} = 0.4V\) vs Differential Input Voltage**

![Figure 29.](image3)

**Peak-to-Peak Output Jitter at \(V_{CM} = 2.9V\) vs Differential Input Voltage**

![Figure 30.](image4)

**Peak-to-Peak Output Jitter at \(V_{CM} = 1.2V\) vs Differential Input Voltage**

![Figure 31.](image5)

**Peak-to-Peak Output Jitter at \(V_{CM} = 1.2V\) vs Ambient Temperature**

![Figure 32.](image6)
## REVISION HISTORY

Changes from Revision D (April 2013) to Revision E  

- Changed layout of National Data Sheet to TI format  

<table>
<thead>
<tr>
<th>Changes from Revision D (April 2013) to Revision E</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changed layout of National Data Sheet to TI format</td>
<td>13</td>
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</tbody>
</table>
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<tr>
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<td>Call TI</td>
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<td>001</td>
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<td>CU SN</td>
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<td>-40 to 85</td>
<td>LV001 TM</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# TAPE AND REEL INFORMATION

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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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*All dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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<th>Width (mm)</th>
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D (R-PDSO-G8)  PLASTIC SMALL OUTLINE

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
   ▶️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
   ▶️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AA.

4040047-3/M 06/11

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