 FEATURES

- >600 Mbps (300 MHz) Switching Rates
- 0.3 ns Typical Differential Skew
- 0.7 ns Maximum Differential Skew
- 1.5 ns Maximum Propagation Delay
- 3.3V Power Supply Design
- ±355 mV Differential Signaling
- Low Power Dissipation (23 mW @ 3.3V Static)
- Flow-Through Design Simplifies PCB Layout
- Interoperable with Existing 5V LVDS Devices
- Power Off Protection (Outputs in High Impedance)
- Conforms to TIA/EIA-644 Standard
- 8-Lead SOIC Package Saves Space
- Industrial Temperature Operating Range
  – (−40°C to +85°C)

DESCRIPTION

The DS90LV017A is a single LVDS driver device optimized for high data rate and low power applications. The DS90LV017A is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized. The device is designed to support data rates in excess of 600Mbps (300MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The device is in a 8-lead SOIC package. The DS90LV017A has a flow-through design for easy PCB layout. The differential driver outputs provides low EMI with its typical low output swing of 355 mV. The DS90LV017A can be paired with its companion single line receiver, the DS90LV018A, or with any of TI's LVDS receivers, to provide a high-speed point-to-point LVDS interface.

Connection Diagram

![Connection Diagram](image)

**Figure 1. Dual-In-Line**

See Package Number D (R-PDSO-G8)

Functional Diagram

![Functional Diagram](image)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.
## Absolute Maximum Ratings\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V(_{CC}))</td>
<td>−0.3V</td>
<td>+3V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage (DI)</td>
<td>−0.3V</td>
<td>+3.6V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage (DO±)</td>
<td>−0.3V</td>
<td>+3.9V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Package Power Dissipation @ +25°C</td>
<td>1190 mW</td>
<td>Derate D Package</td>
<td>9.5 mW/°C above +25°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C</td>
<td>+150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature Range Soldering (4 sec.)</td>
<td>+260°C</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### ESD Ratings

- HBM 1.5 k\(\Omega\), 100 pF: \(\geq 8\) kV
- EIAJ 0 \(\Omega\), 200 pF: \(\geq 1000\) V
- CDM: \(\geq 1000\) V
- IEC direct 330 \(\Omega\), 150 pF: \(\geq 4\) kV

\(^{(1)}\) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. **Electrical Characteristics** specifies conditions of device operation.

## Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V(_{CC}))</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Temperature (T(_A))</td>
<td>−40</td>
<td>25</td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>

## Electrical Characteristics

**Over Supply Voltage and Operating Temperature ranges, unless otherwise specified\(^{(1)}\)\(^{(2)}\)\(^{(3)}\)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Pin</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OD})</td>
<td>Output Differential Voltage (R_L = 100) (\Omega)</td>
<td>(V_{OD}) (Figure 2)</td>
<td>DO+, DO−</td>
<td>(V_{OUT} = V_{CC}) or GND, (V_{CC}) = 0V</td>
<td>250</td>
<td>355</td>
<td>450</td>
<td>mV</td>
</tr>
<tr>
<td>(\Delta V_{OD})</td>
<td>(V_{OD}) Magnitude Change</td>
<td>(V_{OD})</td>
<td>1</td>
<td>35</td>
<td>mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{OH})</td>
<td>Output High Voltage</td>
<td></td>
<td>1.4</td>
<td>1.6</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{OL})</td>
<td>Output Low Voltage</td>
<td></td>
<td>0.9</td>
<td>1.1</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{OS})</td>
<td>Offset Voltage</td>
<td></td>
<td>1.25</td>
<td>1.2</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\Delta V_{OS})</td>
<td>Offset Magnitude Change</td>
<td></td>
<td>3</td>
<td>25</td>
<td>mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{OXD})</td>
<td>Power-off Leakage</td>
<td>(V_{OUT} = V_{CC}) or GND, (V_{CC}) = 0V</td>
<td>0</td>
<td>±1</td>
<td>μA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{OSD})</td>
<td>Output Short Circuit Current</td>
<td></td>
<td>−5.7</td>
<td>−8</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>Input High Voltage</td>
<td></td>
<td>2.0</td>
<td>(V_{CC})</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Input Low Voltage</td>
<td></td>
<td>GND</td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{IH})</td>
<td>Input High Current</td>
<td>(V_{IN} = 3.3) or 2.4(V)</td>
<td>≥2</td>
<td>±10</td>
<td>μA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{IL})</td>
<td>Input Low Current</td>
<td>(V_{IN} = \text{GND}) or 0.5(V)</td>
<td>≥1</td>
<td>±10</td>
<td>μA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{CL})</td>
<td>Input Clamp Voltage</td>
<td>(I_{CL} = −18) (\mu)A</td>
<td>−1.5</td>
<td>−0.6</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{CC})</td>
<td>Power Supply Current</td>
<td>(V_{CC})</td>
<td>5</td>
<td>8</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except \(V_{OD}\).

\(^{(2)}\) All typicals are given for: \(V_{CC} = +3.3\) V and \(T_A = +25\) °C.

\(^{(3)}\) The DS90LV017A is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.
Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified(1)(2)(3)(4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{\text{PHLD}})</td>
<td>Differential Propagation Delay High to Low</td>
<td>(R_L = 100\Omega, C_L = 15\ pF) ((\text{Figure 3 and Figure 4}))</td>
<td>0.3</td>
<td>0.8</td>
<td>1.5</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{\text{PLHD}})</td>
<td>Differential Propagation Delay Low to High</td>
<td></td>
<td>0.3</td>
<td>1.1</td>
<td>1.5</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{\text{SKD1}})</td>
<td>Differential Pulse Skew (</td>
<td>t_{\text{PHLD}} - t_{\text{PLHD}}</td>
<td>) ((5))</td>
<td></td>
<td>0</td>
<td>0.3</td>
</tr>
<tr>
<td>(t_{\text{SKD3}})</td>
<td>Differential Part to Part Skew ((6))</td>
<td></td>
<td>0</td>
<td></td>
<td>1.0</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{\text{SKD4}})</td>
<td>Differential Part to Part Skew ((7))</td>
<td></td>
<td>0</td>
<td></td>
<td>1.2</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{\text{TLH}})</td>
<td>Transition Low to High Time</td>
<td></td>
<td>0.2</td>
<td>0.5</td>
<td>1.0</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{\text{THL}})</td>
<td>Transition High to Low Time</td>
<td></td>
<td>0.2</td>
<td>0.5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>(f_{\text{MAX}})</td>
<td>Maximum Operating Frequency ((8))</td>
<td></td>
<td>350</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
</tbody>
</table>

(1) All typicals are given for: \(V_{\text{CC}} = +3.3\) V and \(T_A = +25\) °C.
(2) These parameters are ensured by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage, temperature) ranges.
(3) \(C_L\) includes probe and fixture capacitance.
(4) Generator waveform for all tests unless otherwise specified: \(f = 1\) MHz, \(Z_O = 50\Omega, t_r \leq 1\) ns, \(t_f \leq 1\) ns (10%-90%).
(5) \(t_{\text{SKD1}}, |t_{\text{PHLD}} - t_{\text{PLHD}}|\), is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(6) \(t_{\text{SKD3}}, \text{ Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same \(V_{\text{CC}}\) and within 5°C of each other within the operating temperature range.}
(7) \(t_{\text{SKD4}}, \text{ part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. \(t_{\text{SKD4}}\) is defined as |Max − Min| differential propagation delay.}
(8) \(f_{\text{MAX}}\) generator input conditions: \(t_r = t_f < 1\) ns (0% to 100%), 50% duty cycle, 0V to 3V. Output criteria: duty cycle = 45%/55%, \(V_{\text{OD}} > 250\) mV.

Parameter Measurement Information

Figure 2. Differential Driver DC Test Circuit

Figure 3. Differential Driver Propagation Delay and Transition Time Test Circuit
Parameter Measurement Information (continued)

Figure 4. Differential Driver Propagation Delay and Transition Time Waveforms

APPLICATION INFORMATION

Table 1. Device Pin Descriptions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>DI1</td>
<td>TTL/CMOS driver input pins</td>
</tr>
<tr>
<td>7</td>
<td>DO1+</td>
<td>Non-inverting driver output pin</td>
</tr>
<tr>
<td>8</td>
<td>DO1−</td>
<td>Inverting driver output pin</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Ground pin</td>
</tr>
<tr>
<td>1</td>
<td>VCC</td>
<td>Positive power supply pin, +3.3V ± 0.3V</td>
</tr>
<tr>
<td>3, 5, 6</td>
<td>NC</td>
<td>No connect</td>
</tr>
</tbody>
</table>
Typical Performance Curves

Output High Voltage vs Power Supply Voltage

\[ V_{\text{OH}} - \text{Output High Voltage (V)} \]
\[ V_{\text{CC}} - \text{Power Supply Voltage (V)} \]
\[ T_A = 25^\circ \text{C} \]
\[ R_L = 100\Omega \]

Figure 5.

Output Low Voltage vs Power Supply Voltage

\[ V_{\text{OL}} - \text{Output Low Voltage (V)} \]
\[ V_{\text{CC}} - \text{Power Supply Voltage (V)} \]
\[ T_A = 25^\circ \text{C} \]
\[ R_L = 100\Omega \]

Figure 6.

Output Short Circuit Current vs Power Supply Voltage

\[ I_{\text{OS}} - \text{Output Short Circuit Current (mA)} \]
\[ V_{\text{IN}} = V_{\text{CC}} \text{ or } \text{GND} \]
\[ V_{\text{OUT}} = 0\text{V} \]
\[ V_{\text{CC}} - \text{Power Supply Voltage (V)} \]

Figure 7.

Differential Output Voltage vs Power Supply Voltage

\[ V_{\text{OD}} - \text{Differential Output Voltage (mV)} \]
\[ V_{\text{CC}} - \text{Power Supply Voltage (V)} \]
\[ T_A = 25^\circ \text{C} \]
\[ R_L = 100\Omega \]

Figure 8.

Differential Output Voltage vs Load Resistor

\[ V_{\text{OD}} - \text{Differential Output Voltage (mV)} \]
\[ R_L - \text{Load Resistor (\Omega)} \]
\[ V_{\text{CC}} = 3.3\text{V} \]
\[ T_A = 25^\circ \text{C} \]

Figure 9.

Offset Voltage vs Power Supply Voltage

\[ V_{\text{OS}} - \text{Offset Voltage (V)} \]
\[ V_{\text{CC}} - \text{Power Supply Voltage (V)} \]
\[ T_A = 25^\circ \text{C} \]
\[ R_L = 100\Omega \]

Figure 10.
Typical Performance Curves (continued)

**Figure 11.**
Power Supply Current vs Frequency

- $I_{CC} = 25^\circ C$
- $V_{IN} = 0V$ to $3V$
- $R_L = 100\Omega$
- $C_L = 15\ pF$
- $V_{CC} = 3.3V$

**Figure 12.**
Power Supply Current vs Power Supply Voltage

- $I_{CC} = 25^\circ C$
- $V_{IN} = 0V$ to $3V$
- $R_L = 100\Omega$
- $C_L = 15\ pF$

**Figure 13.**
Power Supply Current vs Ambient Temperature

- $I_{CC} = 3.3V$
- Frequency = 1 MHz
- $V_{IN} = 0V$ to $3V$
- $R_L = 100\Omega$
- $C_L = 15\ pF$

**Figure 14.**
Differential Propagation Delay vs Power Supply Voltage

- $I_{PLHD}$
- $T_A = 25^\circ C$
- Frequency = 1 MHz
- $C_L = 15\ pF$
- $R_L = 100\Omega$

**Figure 15.**
Differential Propagation Delay vs Ambient Temperature

- $I_{PLHD}$
- $V_{CC} = 3.3V$
- Frequency = 1 MHz
- $C_L = 15\ pF$
- $R_L = 100\Omega$

**Figure 16.**
Differential Skew vs Power Supply Voltage

- $I_{SKD}$
- $T_A = 25^\circ C$
- Frequency = 1 MHz
- $C_L = 15\ pF$
- $R_L = 100\Omega$
Typical Performance Curves (continued)

**Figure 17.** Differential Skew vs Ambient Temperature

- $t_{sk}$ - Differential Skew (ps)
- $T_A$ = Ambient Temperature (°C)
- $V_{CC} = 3.3V$
- Freq = 1 MHz
- $C_L = 15 \text{ pF}$
- $R_L = 100 \Omega$

**Figure 18.** Transition Time vs Power Supply Voltage

- $t_{THL}$, $t_{TLH}$ - Transition Time (ps)
- $T_A = 25\degree C$
- Freq = 1 MHz
- $C_L = 15 \text{ pF}$
- $R_L = 100 \Omega$
- $V_{CC} = 3.3V$

**Figure 19.** Transition Time vs Ambient Temperature

- $t_{THL}$, $t_{TLH}$ - Transition Time (ps)
- $T_A$ = Ambient Temperature (°C)
- Freq = 1 MHz
- $C_L = 15 \text{ pF}$
- $R_L = 100 \Omega$
## REVISION HISTORY

### Changes from Revision B (April 2013) to Revision C

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changed layout of National Data Sheet to TI format</td>
<td>7</td>
</tr>
</tbody>
</table>

Submit Documentation Feedback
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type Package Drawing</th>
<th>Pins Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS90LV017ATM</td>
<td>NRND</td>
<td>SOIC D 8 95</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 85</td>
<td>LV17A TM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DS90LV017ATM/NOPB</td>
<td>ACTIVE</td>
<td>SOIC D 8 95</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LV17A TM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DS90LV017ATMX/NOPB</td>
<td>ACTIVE</td>
<td>SOIC D 8 2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LV17A TM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- ** OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

*All dimensions are nominal.

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS90LV017ATMX/NOPB</td>
<td>SOIC</td>
<td>D 8</td>
<td>2500</td>
<td></td>
<td>330.0</td>
<td>12.4</td>
<td>6.5</td>
<td>5.4</td>
<td>2.0</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

**Dimensions:**
- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS90LV017ATMX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.