**Low Noise, Low Distortion**
**INSTRUMENTATION AMPLIFIER**

**FEATURES**
- LOW NOISE: $1\text{nV}/\sqrt{\text{Hz}}$
- LOW THD+N: 0.0009% at 1kHz, $G = 100$
- HIGH GBW: 100MHz at $G = 1000$
- WIDE SUPPLY RANGE: ±9V to ±25V
- HIGH CMRR: >100dB
- BUILT-IN GAIN SETTING RESISTORS: $G = 1, 100$
- UPGRADES AD625

**APPLICATIONS**
- HIGH QUALITY MICROPHONE PREAMPS (REPLACES TRANSFORMERS)
- MOVING-COIL PREAMPLIFIERS
- DIFFERENTIAL RECEIVERS
- AMPLIFICATION OF SIGNALS FROM:
  - Strain Gages (Weigh Scale Applications)
  - Thermocouples
  - Bridge Transducers

**DESCRIPTION**

The INA103 is a very low noise, low distortion monolithic instrumentation amplifier. Its current-feedback circuitry achieves very wide bandwidth and excellent dynamic response. It is ideal for low-level audio signals such as balanced low-impedance microphones. The INA103 provides near-theoretical limit noise performance for 200Ω source impedances. Many industrial applications also benefit from its low noise and wide bandwidth.

Unique distortion cancellation circuitry reduces distortion to extremely low levels, even in high gain. Its balanced input, low noise and low distortion provide superior performance compared to transformer-coupled microphone amplifiers used in professional audio equipment.

The INA103’s wide supply voltage (±9 to ±25V) and high output current drive allow its use in high-level audio stages as well. A copper lead frame in the plastic DIP assures excellent thermal performance.

The INA103 is available in 16-pin plastic DIP and SOL-16 surface-mount packages. Commercial and Industrial temperature range models are available.
## SPECIFICATIONS

All specifications at \( T_A = +25°C, V_S = ±15V \) and \( R_L = 2kΩ \), unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>INA103KP, KU</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>GAIN</strong></td>
<td></td>
<td>MIN</td>
</tr>
<tr>
<td>Range of Gain</td>
<td>1</td>
<td></td>
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<tr>
<td>Gain Equation (1)</td>
<td>( G = 1 + 6kΩ/R_G )</td>
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<td>Gain Error, DC G = 1</td>
<td>±10V Output</td>
<td>0.005</td>
</tr>
<tr>
<td>G = 100</td>
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<tr>
<td>Gain Temp. Co. G = 1</td>
<td>±10V Output</td>
<td>0.05</td>
</tr>
<tr>
<td>G = 100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nonlinearity, DC G = 1</td>
<td>±10V Output</td>
<td>0.0003</td>
</tr>
<tr>
<td>G = 100</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| **OUTPUT** | | | | |
| Voltage, \( R_L = 600Ω \) | \( T_A = T_{MIN} \) to \( T_{MAX} \) | ±11.5 | ±12 | | V |
| \( R_L = 600Ω \) | \( V_S = ±25, T_A = 25°C \) | ±20 | ±21 | | V |
| Current | | | | | |
| Short Circuit Current | | | | | |
| Capacitive Load Stability | 10 | | | | nF |

| **INPUT OFFSET VOLTAGE** | | | | |
| Initial Offset RTI (3) (KU Grade) | \( (30 + 1200/G) \mu V \) | | | | µV |
| vs Temp G = 1 to 1000 | \( (250 + 5000/G) \mu V \) | | | | µV |
| G = 1000 | | | | | µV/V |
| vs Supply | \( ±9V \) to \( ±25V \) | 0.2 + 8/G | 4 + 60/G | | µV/V |

| **INPUT BIAS CURRENT** | | | | |
| Initial Bias Current | | | | | |
| vs Temp G = 1 to 1000 | \( T_A = T_{MIN} \) to \( T_{MAX} \) | 1 + 20/G | | | µA |
| G = 1000 | | | | | µA/C |
| Initial Offset Current | | | | | µA/
| vs Temp G = 1 to 1000 | \( T_A = T_{MIN} \) to \( T_{MAX} \) | 0.04 | 1 | | µA/C |
| G = 1000 | | | | | µA/C |

| **INPUT IMPEDANCE** | | | | |
| Differential Mode | 60 || 2 | | MΩ || pF |
| Common-Mode | 60 || 5 | | MΩ || pF |

| **INPUT VOLTAGE RANGE** | | | | |
| Common-Mode Range (4) | ±11 | ±12 | | V |
| CMR G = 1 | DC to 60Hz | 72 | 86 | | dB |
| G = 100 | DC to 60Hz | 100 | 125 | | dB |

| **INPUT NOISE** | | | | |
| Voltage (5) \( R_S = 0Ω \) | | | | |
| 10Hz | 2 | | | nV/√Hz |
| 100Hz | 1.2 | | | nV/√Hz |
| 1kHz | 1 | | | nV/√Hz |
| Current | 2 | | | pA/√Hz |

| **OUTPUT NOISE** | | | | |
| Voltage 1kHz | 65 | | | nV/√Hz |
| A Weighted, 20Hz-20kHz | 20Hz-20kHz | –100 | | dBu |

| **DYNAMIC RESPONSE** | | | | |
| –3dB Bandwidth: G = 1 | Small Signal | 6 | | MHz |
| G = 100 | Small Signal | 800 | | kHz |
| Full Power Bandwidth | \( V_{OUT} = ±10V, R_L = 600Ω \) | 240 | | kHz |
| Slew Rate G = 1 | 15 | | | V/µs |
| G = 1 to 500 | | | | |
| THD + Noise G = 100, \( f = 1kHz \) | 0.0009 | | | % |
| Settling Time 0.1% G = 1 | \( V_O = 20V \) Step | 1.7 | | µs |
| G = 100 | | | | |
| Settling Time 0.01% G = 1 | \( V_O = 20V \) Step | 3.5 | | µs |
| G = 100 | | | | |
| Overload Recovery (6) | 50% Overdrive | 1 | | µs |

**NOTES:**
1. Gains other than 1 and 100 can be set by adding an external resistor, \( R_G \) between pins 2 and 15. Gain accuracy is a function of \( R_G \).
2. FS = Full Scale.
3. Adjustable to zero.
4. \( V_O = 0V \), see Typical Curves for \( V_{CL} \) vs \( V_O \).
5. \( V_{NOISE RTI} = \sqrt{V^2_{INPUT} + (V_{VOUT}/Gain)^2 + 4KTR_G} \), see Typical Curves.
6. Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.
SPECIFICATIONS (CONT)

All specifications at TA = +25°C, VS = ±15V and RL = 2kΩ, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>INA103KP, KU</th>
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</thead>
<tbody>
<tr>
<td>POWER SUPPLY</td>
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<td></td>
</tr>
<tr>
<td>Rated Voltage</td>
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<td>±15</td>
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<tr>
<td>Voltage Range</td>
<td>±9</td>
<td>±25</td>
</tr>
<tr>
<td>Quiescent Current</td>
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<td>TEMPERATURE RANGE</td>
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<td>Specification</td>
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<tr>
<td>Operation</td>
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<td>+85</td>
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<tr>
<td>Storage</td>
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<td>+100</td>
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<tr>
<td>Thermal Resistance, θJA</td>
<td>100</td>
<td></td>
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</tbody>
</table>

PIN CONFIGURATION

- Input
+ Gain Sense
+ Offset Null
– Offset Null
– Gain Drive
+ Gain Drive
–R\textsubscript{0}
G = 100
R\textsubscript{0}
Ref
V–
V+

NOTE: (1) Pin 1 Marking—SOL-16 Package

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ABSOLUTE MAXIMUM RATINGS\(^{(1)}\)

- Power Supply Voltage: ±25V
- Input Voltage Range, Continuous: ±3V\textsubscript{S}
- Operating Temperature Range: –40°C to +85°C
- Storage Temperature Range: –40°C to +85°C
- Junction Temperature: P, U Package: +125°C
- Lead Temperature (soldering, 10s): +300°C
- Output Short Circuit to Common: Continuous

NOTE: (1) Stresses above these ratings may cause permanent damage.

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TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ C$, $V_S = \pm 15V$, unless otherwise noted.

**INPUT VOLTAGE RANGE vs SUPPLY**

**OUTPUT SWING vs SUPPLY**

**MAX COMMON-MODE VOLTAGE vs OUTPUT VOLTAGE**

**OUTPUT SWING vs LOAD RESISTANCE**

**OFFSET VOLTAGE vs TIME FROM POWER UP (G = 100)**

**INPUT BIAS CURRENT vs SUPPLY**
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ C$, $V_S = \pm 15V$, unless otherwise noted.

INPUT BIAS CURRENT vs TEMPERATURE

SMALL SIGNAL TRANSIENT RESPONSE
(G = 1)

LARGE SIGNAL TRANSIENT RESPONSE
(G = 1)

SMALL SIGNAL TRANSIENT RESPONSE
(G = 100)

LARGE SIGNAL TRANSIENT RESPONSE
(G = 100)

SETTLING TIME vs GAIN
(0.1%, 20V STEP)
TYPICAL PERFORMANCE CURVES (CONT)

At $T_{a} = +25^\circ C$, $V_{s} = \pm 15V$, unless otherwise noted.

**SETTLING TIME vs GAIN**

(0.01%, 20V STEP)

**SMALL-SIGNAL FREQUENCY RESPONSE**

**NOISE VOLTAGE (RTI) vs FREQUENCY**

**CMR vs FREQUENCY**

**THD + N vs FREQUENCY**

**V+ POWER SUPPLY REJECTION vs FREQUENCY**
TYPICAL PERFORMANCE CURVES (CONT)

At \( T_A = +25^\circ \text{C}, \ V_S = \pm 15 \text{V}, \) unless otherwise noted.

### Power Supply Rejection (dB)

- **Frequency (Hz):** 1, 10, 100, 1k, 10k, 100k
- **Gain:** G = 1, G = 10, G = 100, G = 1000

### THD + N vs Level (dBu)

- **Output Amplitude (dBu):** -60, -45, -30, -15, 0, 15
- **Gain:** G = 1, G = 10, G = 100, G = 1000
- **f = 1kHz**

### THD + N vs Load (Ω)

- **Gain:** G = 1, G = 10, G = 100, G = 1000
- **V\text{OUT} = 20Vp-p, f = 1kHz**

### CCIF IMD vs Frequency (Hz)

- **Gain:** G = 1, G = 10, G = 100, G = 1000
- **Output Amplitude (dBu):** -60, -50, -40, -30, -20, -10, 0, 10, 20

### SMPTE IMD vs Amplitude (dBu)

- **Gain:** G = 1, G = 10, G = 100, G = 1000
- **Output Amplitude (dBu):** -60, -50, -40, -30, -20, -10, 0, 10, 20
APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation. Power supplies should be bypassed with 1µF tantalum capacitors near the device pins. The output Sense (pin 11) and output Reference (pin 7) should be low impedance connections. Resistance of a few ohms in series with these connections will degrade the common-mode rejection of the amplifier.
To avoid oscillations, make short, direct connection to the gain set resistor and gain sense connections. Avoid running output signals near these sensitive input nodes.

INPUT CONSIDERATIONS

Certain source impedances can cause the INA103 to oscillate. This depends on circuit layout and source or cable characteristics connected to the input. An input network consisting of a small inductor and resistor (Figure 2) can greatly reduce the tendency to oscillate. This is especially useful if various input sources are connected to the INA103. Although not shown in other figures, this network can be used, if needed, with all applications shown.

GAIN SELECTION

Gains of 1 or 100V/V can be set without external resistors. For G = 1V/V (unity gain) leave pin 14 open (no connection)—see Figure 4. For G = 100V/V, connect pin 14 to pin 6—see Figure 5.
Gain can also be accurately set with a single external resistor as shown in Figure 1. The two internal feedback resistors are laser-trimmed to 3kΩ within approximately ±0.1%. The temperature coefficient of these resistors is approximately 50ppm/°C. Gain using an external Rg resistor is—

\[ G = 1 + \frac{6k\Omega}{R_g} \]
Accuracy and TCR of the external $R_G$ will also contribute to gain error and temperature drift. These effects can be directly inferred from the gain equation.

Connections available on $A_1$ and $A_2$ allow external resistors to be substituted for the internal $3k\Omega$ feedback resistors. A precision resistor network can be used for very accurate and stable gains. To preserve the low noise of the INA103, the value of external feedback resistors should be kept low. Increasing the feedback resistors to $20k\Omega$ would increase noise of the INA103 to approximately $1.5nV/\sqrt{Hz}$. Due to the current-feedback input circuitry, bandwidth would also be reduced.

### NOISE PERFORMANCE

The INA103 provides very low noise with low source impedance. Its $1nV/\sqrt{Hz}$ voltage noise delivers near theoretical noise performance with a source impedance of $200\Omega$.

Relatively high input stage current is used to achieve this low noise. This results in relatively high input bias current and input current noise. As a result, the INA103 may not provide best noise performance with source impedances greater than $10k\Omega$. For source impedance greater than $10k\Omega$, consider the INA114 (excellent for precise DC applications), or the INA111 FET-input IA for high speed applications.

### OFFSET ADJUSTMENT

Offset voltage of the INA103 has two components: input stage offset voltage is produced by $A_1$ and $A_2$; and, output stage offset is produced by $A_3$. Both input and output stage offset are laser trimmed and may not need adjustment in many applications.

Offset voltage can be trimmed with the optional circuit shown in Figure 3. This offset trim circuit primarily adjusts the output stage offset, but also has a small effect on input stage offset. For a $1mV$ adjustment of the output voltage, the input stage offset is adjusted approximately $1\mu V$. Use this adjustment to null the INA103’s offset voltage with zero differential input voltage. Do not use this adjustment to null offset produced by a sensor, or offset produced by subsequent stages, since this will increase temperature drift.

To offset the output voltage without affecting drift, use the circuit shown in Figure 4. The voltage applied to pin 7 is summed at the output. The op amp connected as a buffer provides a low impedance at pin 7 to assure good common-mode rejection.

Figure 5 shows a method to trim offset voltage in AC-coupled applications. A nearly constant and equal input bias current of approximately $2.5\mu A$ flows into both input terminals. A variable input trim voltage is created by adjusting the balance of the two input bias return resistances through which the input bias currents must flow.
Figure 6 shows an active control loop that adjusts the output offset voltage to zero. \( A_2, R, \) and \( C \) form an integrator that produces an offsetting voltage applied to one input of the INA103. This produces a \(-6\text{dB/octave}\) low frequency roll-off like the capacitor input coupling in Figure 5.

**COMMON-MODE INPUT RANGE**

For proper operation, the combined differential input signal and common-mode input voltage must not cause the input amplifiers to exceed their output swing limits. The linear input range is shown in the typical performance curve "Maximum Common-Mode Voltage vs Output Voltage." For a given total gain, the input common-mode range can be increased by reducing the input stage gain and increasing the output stage gain with the circuit shown in Figure 7.

**OUTPUT SENSE**

An output sense terminal allows greater gain accuracy in driving the load. By connecting the sense connection at the load, \( I R \) voltage loss to the load is included inside the feedback loop. Current drive can be increased by connecting a current booster inside the feedback loop as shown in Figure 11.

**FIGURE 4. Output Offsetting.**

**FIGURE 5. Input Offset Adjustment for AC-Coupled Inputs.**

**FIGURE 6. Automatic DC Restoration.**
A common problem with many IC op amps and instrumentation amplifiers is shown in (a). Here, the amplifier’s input is driven beyond its linear common-mode range, forcing the output of the amplifier into the supply rails. The output then “folds back”, i.e., a more positive input voltage now causes the output of the amplifier to go negative. The INA103 has protection circuitry to prevent fold-back, and as shown in (b), limits cleanly.

FIGURE 9. INA103 Overload Condition Performance.

FIGURE 13. Instrumentation Amplifier with Shield Driver.

FIGURE 14. Gain-of-100 INA103 with FET Buffers.
## PACKAGE INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
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<td>25</td>
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<td>CU NIPDAU</td>
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<td>DW</td>
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<td>INA103KU</td>
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</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
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### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal.*

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<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width (W1) (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
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<th>Pin1 Quadrant</th>
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### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

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This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
**MECHANICAL DATA**

**N (R-PDIP-T**)**

16 PINS SHOWN

**PLASTIC DUAL-IN-LINE PACKAGE**

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<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
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<tbody>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
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**MS-001 VARIATION**

| AA | BB | AC | AD |

**NOTES:**

A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

1. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

2. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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