

# INA333-Q1 Automotive, Zero-Drift, micro-Power, Instrumentation Amplifier

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1:  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
- Low offset voltage: 25  $\mu\text{V}$  (maximum),  $G \geq 100$
- Low drift: 0.1  $\mu\text{V}/^{\circ}\text{C}$ ,  $G \geq 100$
- Low noise: 50  $\text{nV}/\sqrt{\text{Hz}}$ ,  $G \geq 100$
- High CMRR: 100 dB (minimum),  $G \geq 10$
- Low input bias current: 200 pA (maximum)
- Supply range: 1.8 V to 5.5 V
- Input voltage:  $(V-) + 0.1\text{ V}$  to  $(V+) - 0.1\text{ V}$
- Output range:  $(V-) + 0.05\text{ V}$  to  $(V+) - 0.05\text{ V}$
- Low quiescent current: 50  $\mu\text{A}$
- Operating temperature:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- RFI filtered inputs
- Package: 8-Pin VSSOP

## 2 Applications

- [Powertrain torque sensor](#)
- [Powertrain pressure sensor](#)
- [Powertrain temperature sensor](#)
- [Powertrain knock sensor](#)
- [Vehicle occupant detection sensor](#)
- [Driver vital sign monitoring](#)

## 3 Description

The INA333-Q1 is a low-power, precision instrumentation amplifier offering excellent accuracy. The versatile three-operational-amplifier design, small size, and low power make this device an excellent choice for a wide range of automotive applications that use resistive bridge sensors.

A single external resistor sets any gain from 1 to 1000. The INA333-Q1 is designed to use an industry-standard gain equation:  $G = 1 + (100\text{ k}\Omega / R_G)$ .

The INA333-Q1 provides very low offset voltage (25  $\mu\text{V}$ ,  $G \geq 100$ ), excellent offset voltage drift (0.1  $\mu\text{V}/^{\circ}\text{C}$ ,  $G \geq 100$ ), and high common-mode rejection (100 dB at  $G \geq 10$ ). The device operates with power supplies as low as 1.8 V ( $\pm 0.9\text{ V}$ ) and quiescent current is only 50  $\mu\text{A}$ , making this device an excellent choice for battery-operated systems. Autocalibration techniques maintain excellent precision over the industrial temperature range. The INA333-Q1 also offers exceptionally low noise density (50  $\text{nV}/\sqrt{\text{Hz}}$ ) that extends down to dc.

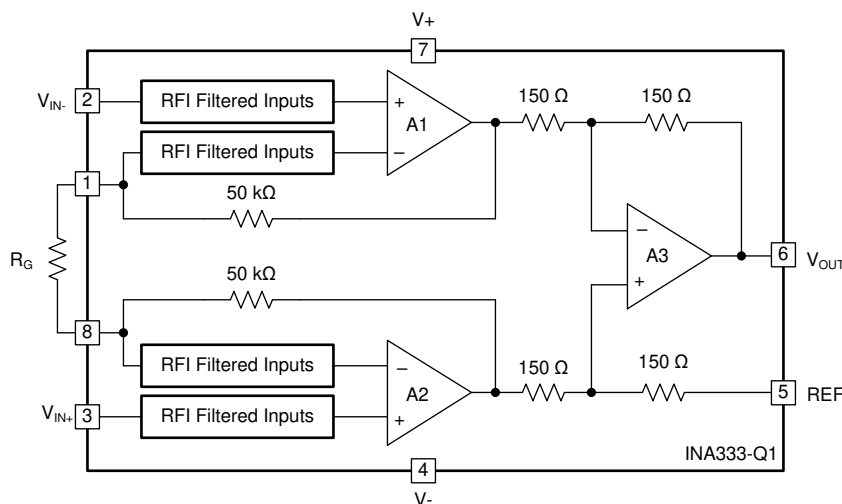
The INA333-Q1 device is available in an 8-pin VSSOP package and is specified over the  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA333-Q1	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

### Simplified Schematic



$$G = 1 + \left( \frac{100\text{ k}\Omega}{R_G} \right)$$



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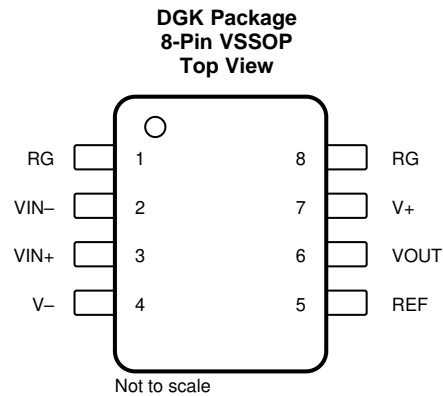
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## 4 Revision History

DATE	REVISION	NOTES
October 2019	*	Initial release.

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## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
REF	5	I	Reference input. This pin must be driven by low impedance or connected to ground.
RG	1, 8	—	Gain setting pins. For gains greater than 1, place a gain resistor between pins 1 and 8.
V+	7	—	Positive supply
V-	4	—	Negative supply
VIN+	3	I	Positive input
VIN-	2	I	Negative input
VOUT	6	O	Output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
	Supply voltage		7	V
	Analog input voltage <sup>(2)</sup>	(V <sub>-</sub> ) - 0.3	(V <sub>+</sub> ) + 0.3	V
	Output short-circuit <sup>(3)</sup>	Continuous		
T <sub>A</sub>	Operating temperature	-40	150	°C
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
- Short-circuit to ground.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD classification level 3A	±4000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1000	

- AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage	1.8	5.5	V
T <sub>A</sub>	Specified temperature	-40	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		INA333-Q1	UNIT
		DGK (VSSOP)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	169.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	62.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	90.3	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	7.6	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	88.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 Electrical Characteristics

at  $V_S = 1.8\text{ V to }5.5\text{ V}$  at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = V_S / 2$ , and  $G = 1$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>INPUT<sup>(1)</sup></b>							
$V_{OSI}$	Offset voltage, RTI <sup>(2)</sup>			$\pm 10 \pm 25/G$	$\pm 25 \pm 75/G$		$\mu\text{V}$
PSRR	Power-supply rejection ratio			$\pm 1 \pm 5/G$	$\pm 5 \pm 15/G$		$\mu\text{V/V}$
		$T_A = -40^\circ\text{C to }+125^\circ\text{C}$			$\pm 0.1 \pm 0.5/G$		$\mu\text{V}/^\circ\text{C}$
	Long-term stability			See <sup>(3)</sup>			
	Turn on time to specified $V_{OSI}$	$T_A = -40^\circ\text{C to }+125^\circ\text{C}$		See <i>Typical Characteristics</i>			
$Z_{IN}$	Input impedance	Differential		100    3			G $\Omega$    pF
		Common-mode		100    3			
$V_{CM}$	Common-mode voltage	$V_O = 0\text{ V}$		$(V-) + 0.1$	$(V+) - 0.1$		V
CMRR	Common-mode rejection ratio	DC to 60 Hz, $V_{CM} = (V-) + 0.1\text{ V to } (V+) - 0.1\text{ V}$	$G = 1$	80	90		dB
			$G = 10$	100	110		
			$G = 100$	100	115		
			$G = 1000$	100	115		
<b>INPUT BIAS CURRENT</b>							
$I_B$	Input bias current			$\pm 70$	$\pm 200$		pA
		$T_A = -40^\circ\text{C to }+125^\circ\text{C}$		See <a href="#">Figure 26</a>			pA/ $^\circ\text{C}$
$I_{OS}$	Input offset current			$\pm 50$	$\pm 200$		pA
		$T_A = -40^\circ\text{C to }+125^\circ\text{C}$		See <a href="#">Figure 28</a>			pA/ $^\circ\text{C}$
<b>INPUT VOLTAGE NOISE</b>							
$e_{NI}$	Input voltage noise	$G = 100, R_S = 0\ \Omega$	$f = 10\text{ Hz}$	50			nV/ $\sqrt{\text{Hz}}$
			$f = 100\text{ Hz}$	50			
			$f = 1\text{ kHz}$	50			
			$f = 0.1\text{ Hz to }10\text{ Hz}$	1			
$i_N$	Input current noise	$f = 10\text{ Hz}$		100			fA/ $\sqrt{\text{Hz}}$
		$f = 0.1\text{ Hz to }10\text{ Hz}$		2			
<b>GAIN</b>							
	Gain equation			$1 + (100\text{ k}\Omega/R_G)$			V/V
G	Gain			1	1000		V/V
	Gain error	$V_S = 5.5\text{ V},$ $(V-) + 100\text{ mV} \leq V_O \leq (V+) - 100\text{ mV}$	$G = 1$	$\pm 0.01\%$	$\pm 0.1\%$		
			$G = 10$	$\pm 0.05\%$	$\pm 0.25\%$		
			$G = 100$	$\pm 0.07\%$	$\pm 0.25\%$		
			$G = 1000$	$\pm 0.25\%$	$\pm 0.5\%$		
	Gain drift error	$V_S = 5.5\text{ V},$ $(V-) + 100\text{ mV} \leq V_O \leq (V+) - 100\text{ mV},$ $T_A = -40^\circ\text{C to }+125^\circ\text{C}$	$G = 1$	$\pm 1$	$\pm 5$		ppm/ $^\circ\text{C}$
			$G > 1^{(4)}$	$\pm 15$	$\pm 50$		
	Gain nonlinearity	$V_S = 5.5\text{ V},$ $(V-) + 100\text{ mV} \leq V_O \leq (V+) - 100\text{ mV},$ $R_L = 10\text{ k}\Omega$		10			ppm
<b>OUTPUT</b>							
	Output voltage swing from rail	$V_S = 5.5\text{ V}, R_L = 10\text{ k}\Omega$		See <a href="#">Figure 29</a>		50	mV
	Capacitive load drive			500			pF
$I_{SC}$	Short-circuit current	Continuous to common	Source	5			mA
			Sink	-40			

(1) Total  $V_{OS}$ , referred-to-input =  $(V_{OSI}) + (V_{OSO} / G)$ .

(2) RTI = Referred-to-input.

(3) 300-hour life test at  $150^\circ\text{C}$  demonstrated randomly distributed variation of approximately  $1\ \mu\text{V}$ .

(4) Does not include effects of external resistor  $R_G$ .

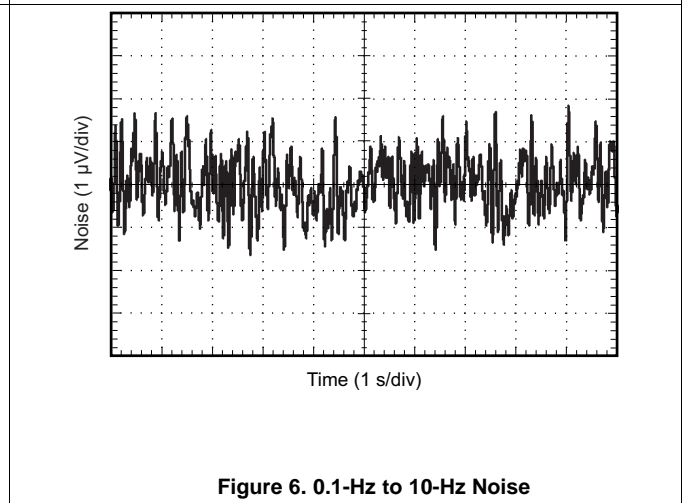
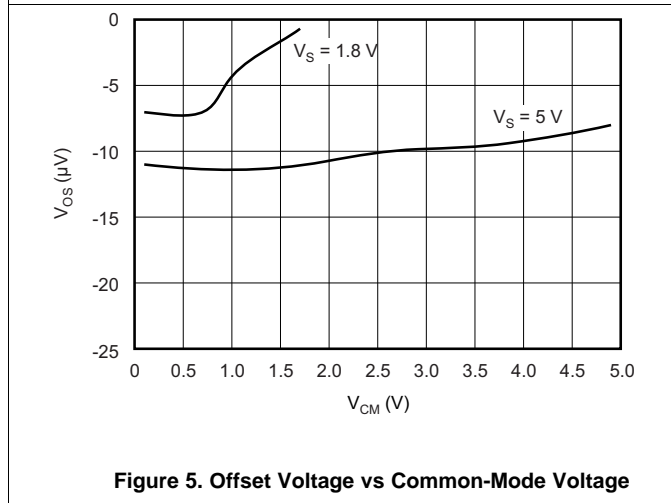
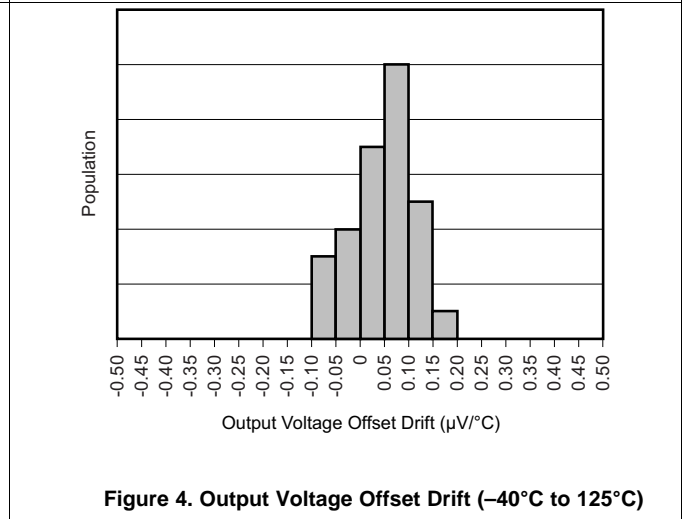
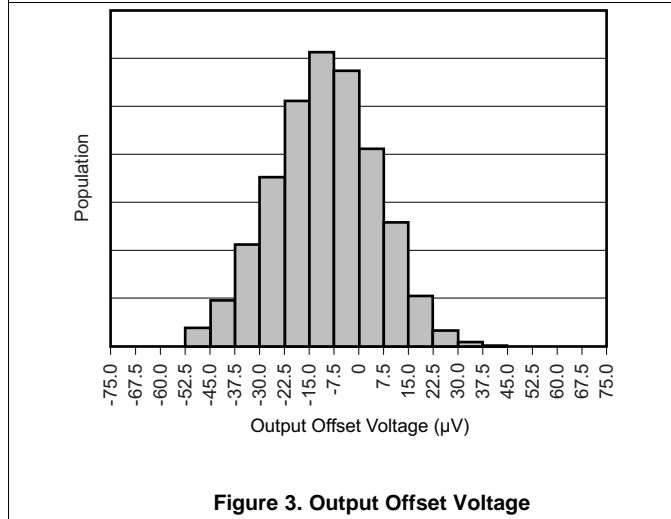
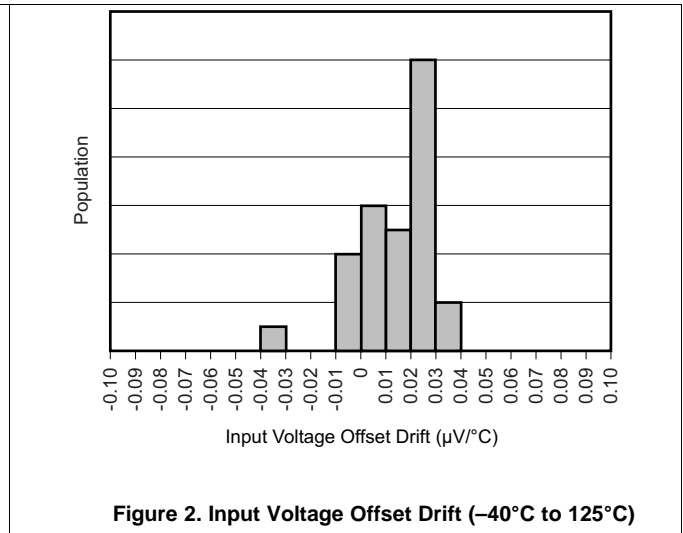
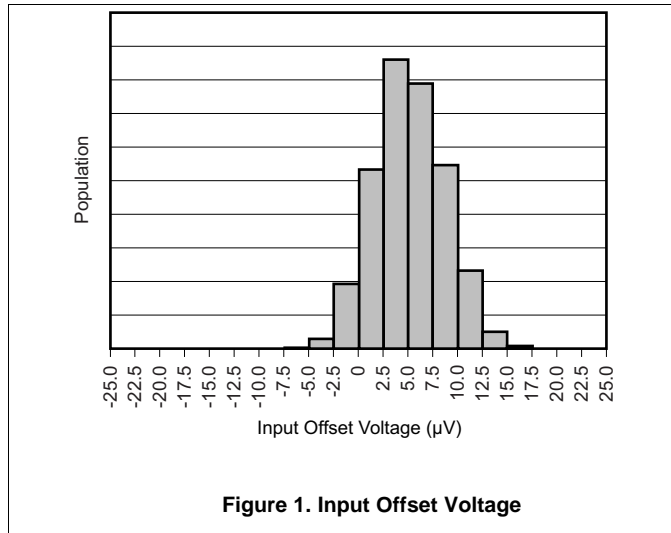
**Electrical Characteristics (continued)**

 at  $V_S = 1.8\text{ V to }5.5\text{ V}$  at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = V_S / 2$ , and  $G = 1$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>FREQUENCY RESPONSE</b>						
	Bandwidth, -3 dB	$G = 1$		150		kHz
		$G = 10$		35		
		$G = 100$		3.5		Hz
		$G = 1000$		350		
SR	Slew rate	$V_S = 5\text{ V}$ , $V_O = 4\text{-V step}$ , $G = 1$		0.16		V/ $\mu\text{s}$
		$V_S = 5\text{ V}$ , $V_O = 4\text{-V step}$ , $G = 100$		0.05		
$t_s$	Settling time to 0.01%	$V_{STEP} = 4\text{ V}$ , $G = 1$		50		$\mu\text{s}$
		$V_{STEP} = 4\text{ V}$ , $G = 100$		400		
	Settling time to 0.001%	$V_{STEP} = 4\text{ V}$ , $G = 1$		60		
		$V_{STEP} = 4\text{ V}$ , $G = 100$		500		
	Overload recovery	50% overdrive		75		$\mu\text{s}$
<b>REFERENCE INPUT</b>						
$R_{IN}$	Input impedance			300		k $\Omega$
	Reference input voltage		V-		V+	V
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent current	$V_{IN} = V_S / 2$		50	75	$\mu\text{A}$
		$V_{IN} = V_S / 2$ , $T_A = -40^\circ\text{C to }+125^\circ\text{C}$			80	

## 6.6 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$  (unless otherwise noted)



Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$  (unless otherwise noted)

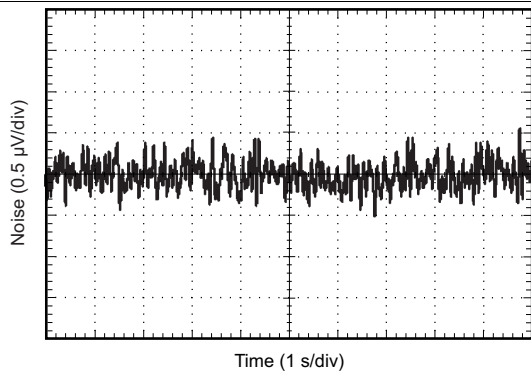


Figure 7. 0.1-Hz to 10-Hz Noise

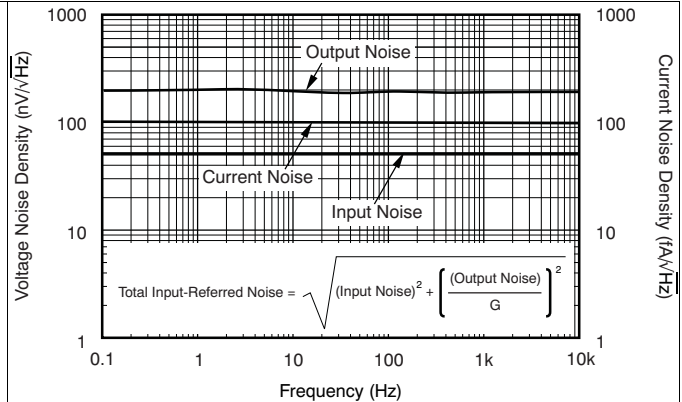


Figure 8. Spectral Noise Density

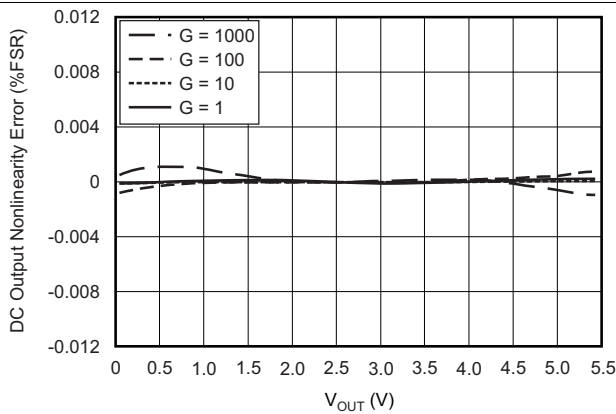


Figure 9. Nonlinearity Error

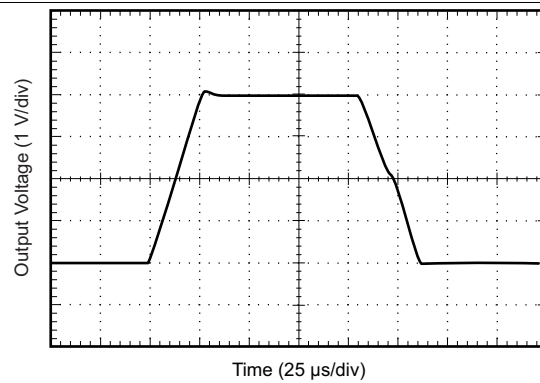


Figure 10. Large Signal Response

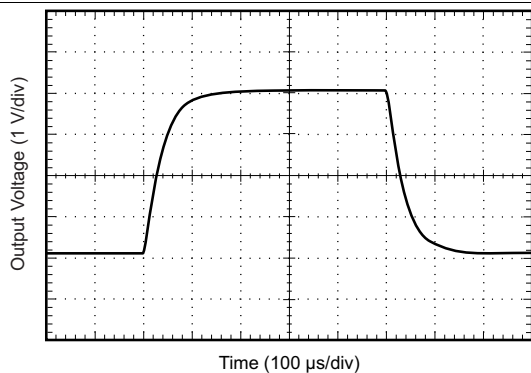


Figure 11. Large-Signal Step Response

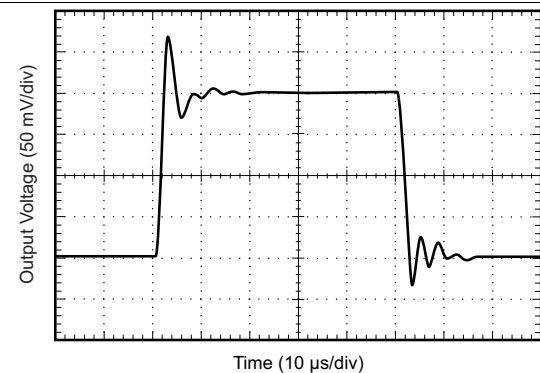


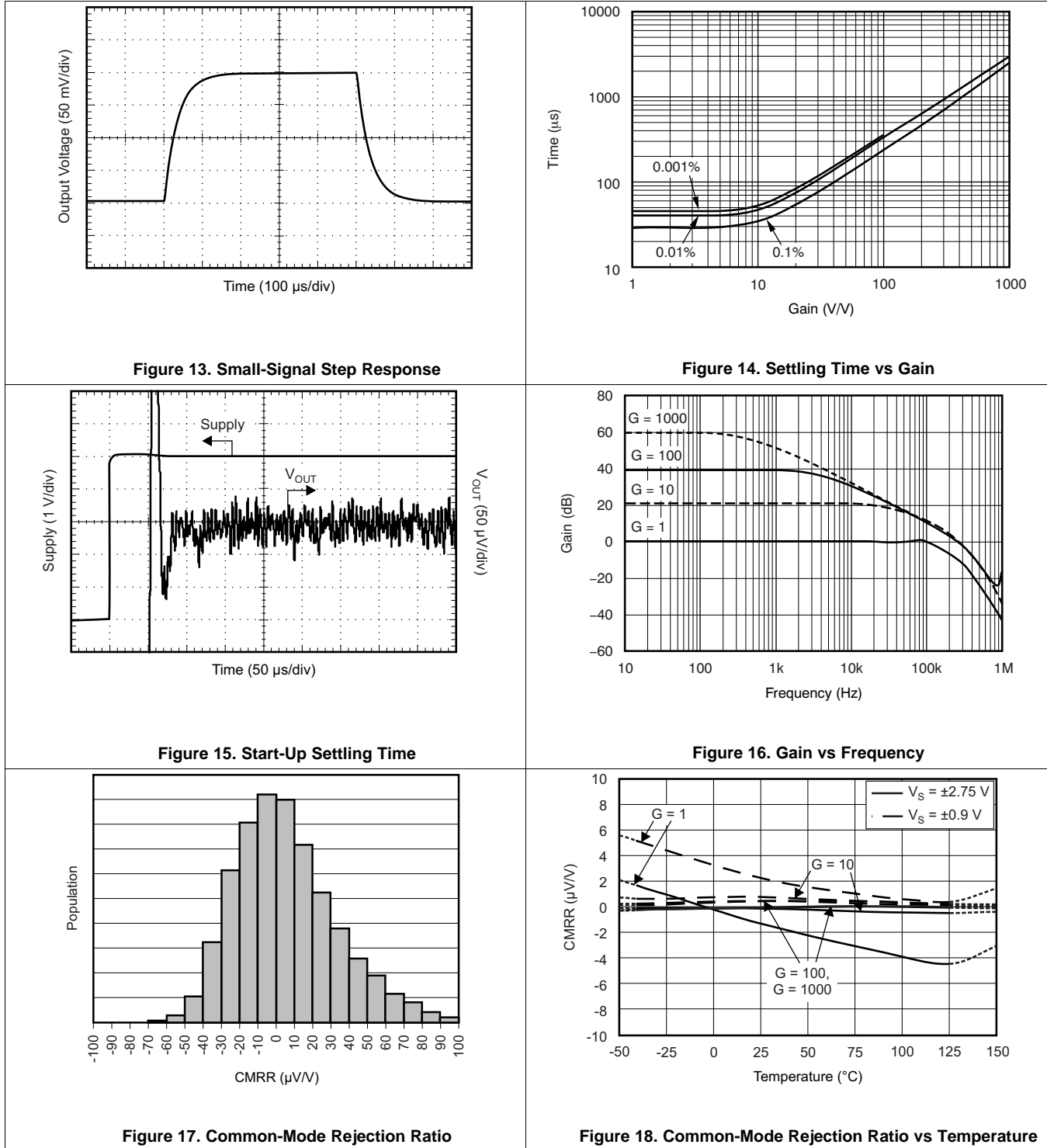
Figure 12. Small-Signal Step Response

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Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = \text{mid supply}$ , and  $G = 1$  (unless otherwise noted)



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Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = \text{mid supply}$ , and  $G = 1$  (unless otherwise noted)

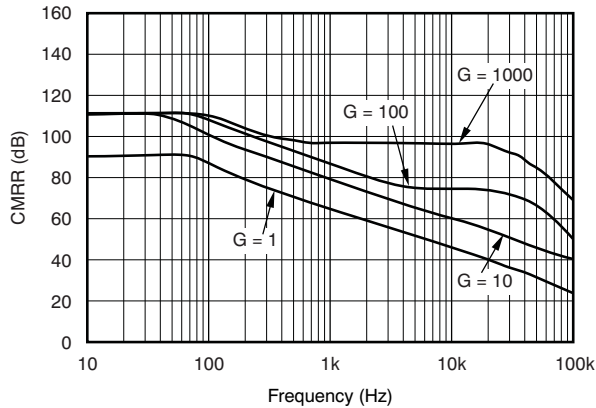


Figure 19. Common-Mode Rejection Ratio vs Frequency

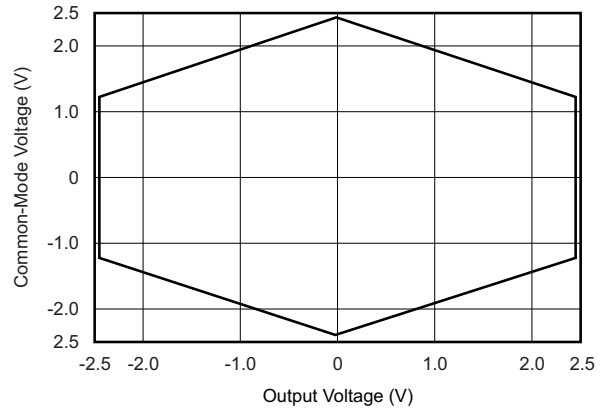


Figure 20. Typical Common-Mode Range vs Output Voltage

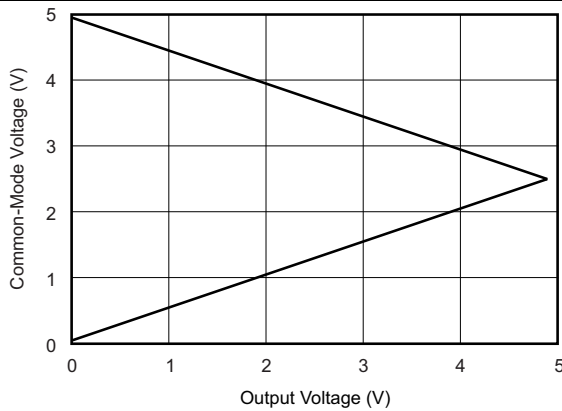


Figure 21. Typical Common-Mode Range vs Output Voltage

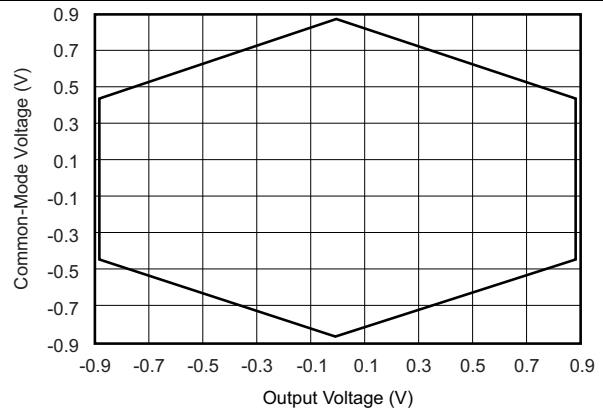


Figure 22. Typical Common-Mode Range vs Output Voltage

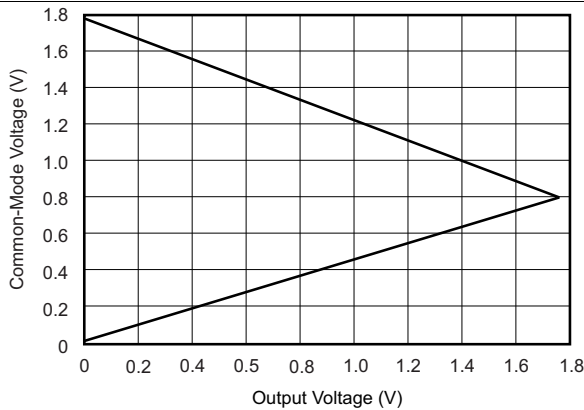


Figure 23. Typical Common-Mode Range vs Output Voltage

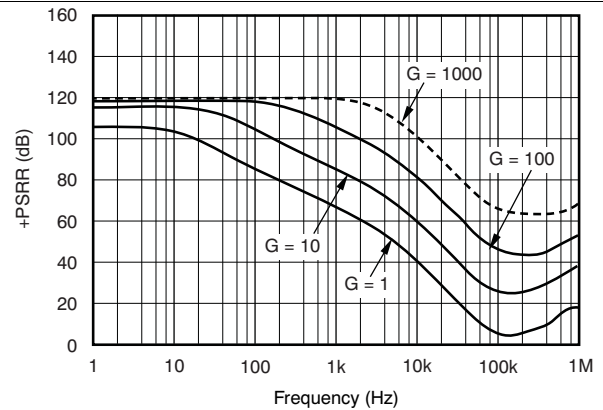


Figure 24. Positive Power-Supply Rejection Ratio

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Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = \text{mid supply}$ , and  $G = 1$  (unless otherwise noted)

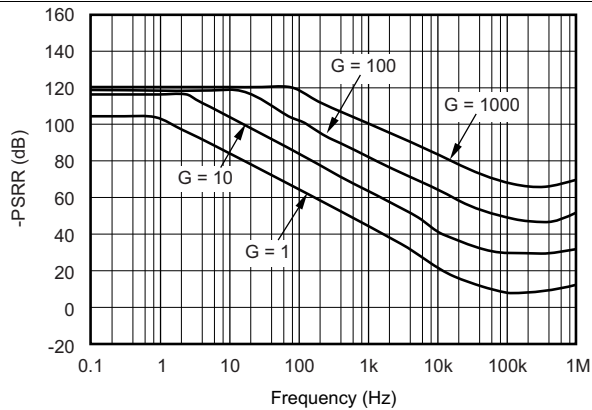


Figure 25. Negative Power-Supply Rejection Ratio

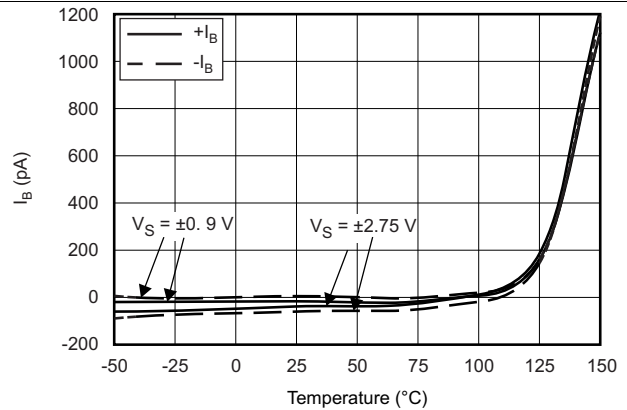


Figure 26. Input Bias Current vs Temperature

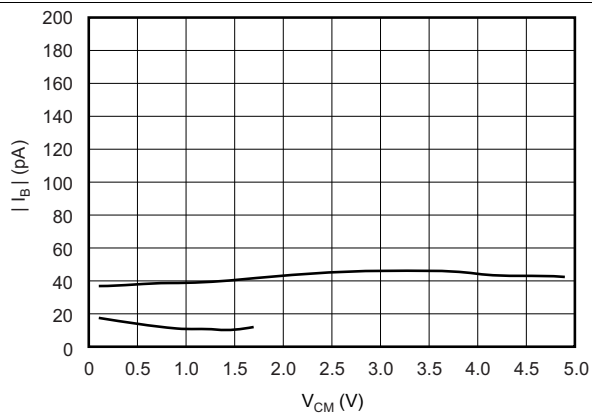


Figure 27. Input Bias Current vs Common-Mode Voltage

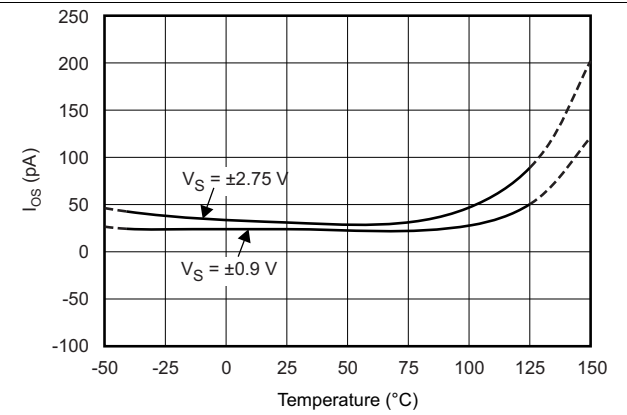


Figure 28. Input Offset Current vs Temperature

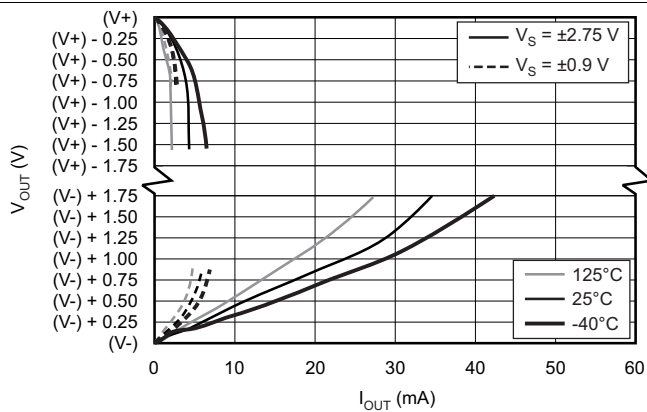


Figure 29. Output Voltage Swing vs Output Current

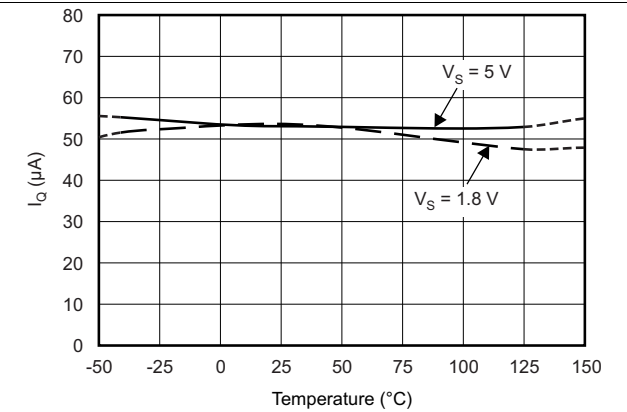
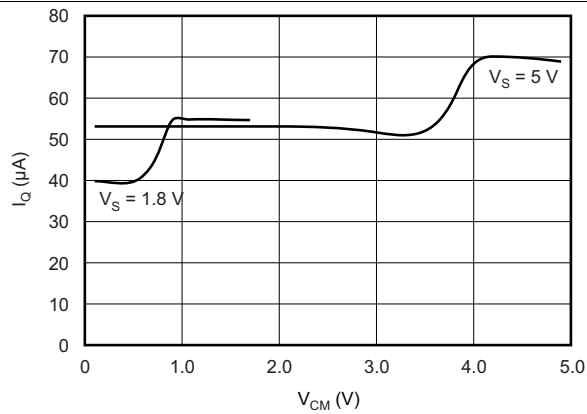


Figure 30. Quiescent Current vs Temperature

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**Typical Characteristics (continued)**

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$  (unless otherwise noted)



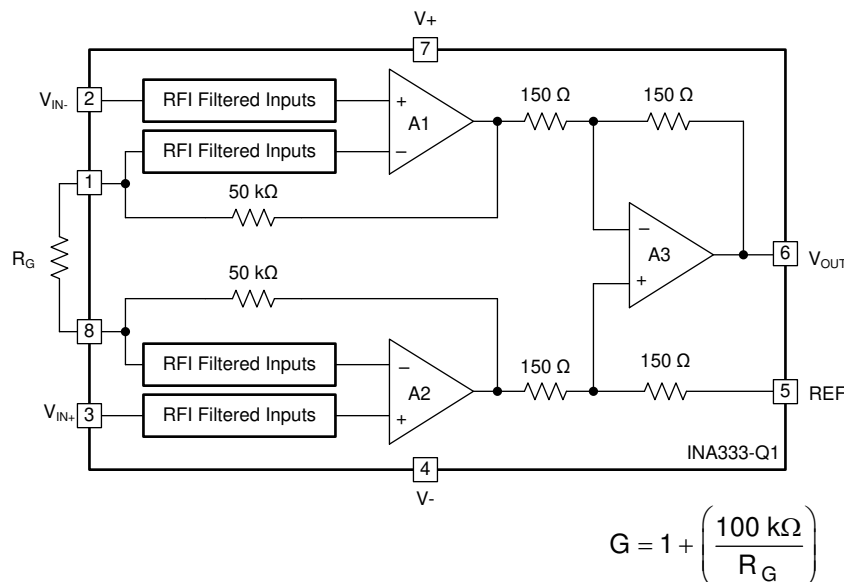
**Figure 31. Quiescent Current vs Common-Mode Voltage**

## 7 Detailed Description

### 7.1 Overview

The INA333-Q1 is a monolithic instrumentation amplifier (INA) based on the precision zero-drift INA333-Q1 (operational amplifier) core. The INA333-Q1 also integrates laser-trimmed resistors to maintain excellent common-mode rejection and low gain error. The combination of the zero-drift amplifier core and the precision resistors allows this device to achieve outstanding dc precision, and makes the INA333-Q1 an excellent choice for many 3.3-V and 5-V automotive applications.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Operating Voltage

The INA333-Q1 operates over a power-supply range of 1.8 V to 5.5 V ( $\pm 0.9$  V to  $\pm 2.75$  V). Supply voltages greater than 7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

#### 7.3.2 Internal Offset Correction

The INA333-Q1 internal operational amplifiers use an auto-calibration technique with a time-continuous, 350-kHz operational amplifier in the signal path. The amplifier is zero-corrected every 8  $\mu$ s using a proprietary technique. At power up, the amplifier requires approximately 100  $\mu$ s to achieve the specified  $V_{OS}$  accuracy. This design has no aliasing or flicker noise.

#### 7.3.3 Input Protection

The input pins of the INA333-Q1 are protected with internal diodes connected to the power-supply rails. These diodes clamp and prevent the applied signal from damaging the input circuitry. If the input signal voltage exceeds the power supplies by greater than 0.3 V, limit the input signal current to less than 10 mA to protect the internal clamp diodes. This current limiting is generally done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

### 7.4 Device Functional Modes

The INA333-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 1.8 V. The recommended maximum specified power-supply voltage for the INA333-Q1 is 5.5 V.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The INA333-Q1 measures small differential voltage with high common-mode voltage developed between the noninverting and inverting input. The high input impedance makes the INA333-Q1 a great choice for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

#### 8.1.1 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA333-Q1 is from approximately 0.1 V below the positive supply voltage to 0.1 V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A1 and A2. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage; see [Figure 20](#) to [Figure 23](#) in the *Typical Characteristics* section.

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA333-Q1 is near 0 V even though both inputs are overloaded.

## 8.2 Typical Application

Figure 32 shows the basic connections required for operation of the INA333-Q1. Good layout practice mandates the use of bypass capacitors placed close to the device pins as shown.

The output of the INA333-Q1 is referred to the output reference (REF) pin, which is normally grounded. This connection must be low-impedance to maintain good common-mode rejection. Although 15 Ω or less of stray resistance can be tolerated while maintaining specified CMRR, small stray resistances of tens of ohms in series with the REF pin can cause noticeable degradation in CMRR.

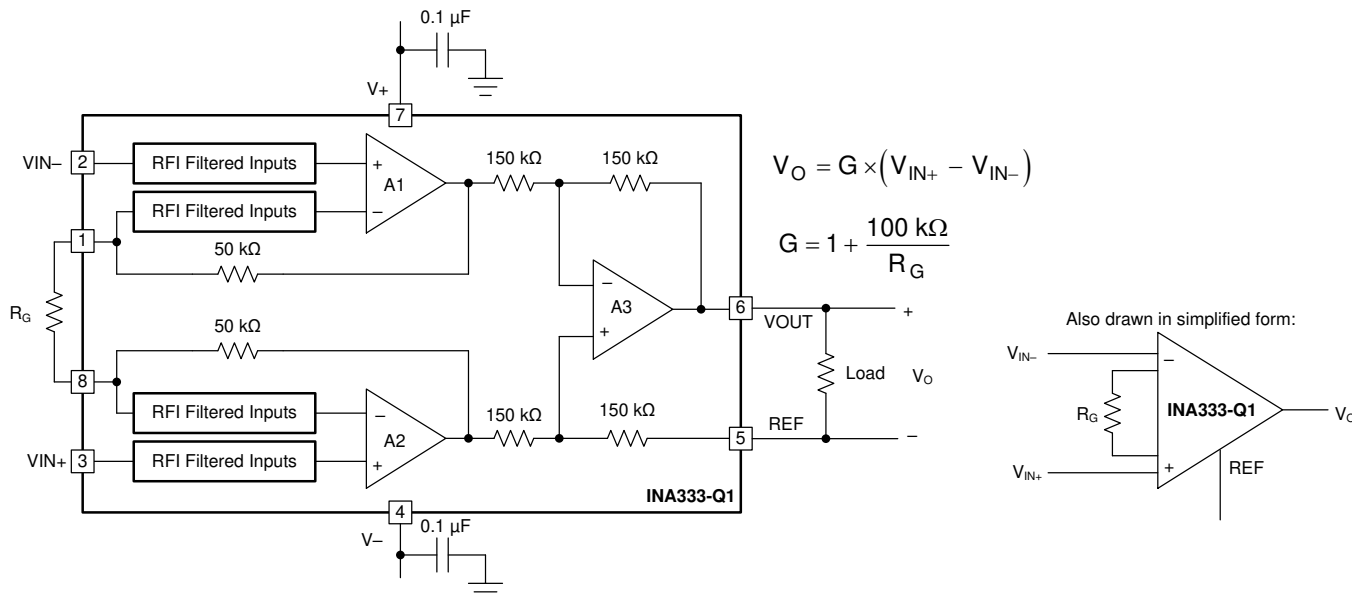


Figure 32. Basic Connections

### 8.2.1 Design Requirements

The device can be configured to monitor the input differential voltage when the gain of the input signal is set by the external resistor  $R_G$ . The output signal references to the Ref pin. The most common application is where the output is referenced to ground when no input signal is present by connecting the Ref pin to ground. When the input signal increases, the output voltage at the OUT pin increases, too.

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Setting the Gain

Gain of the INA333-Q1 is set by a single external resistor,  $R_G$ , connected between pins 1 and 8. The value of  $R_G$  is selected according to Equation 1:

$$G = 1 + (100 \text{ k}\Omega / R_G) \quad (1)$$

Table 1 lists several commonly-used gains and resistor values. The 100 kΩ in Equation 1 comes from the sum of the two internal feedback resistors of  $A_1$  and  $A_2$ . These on-chip resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA333-Q1.

## Typical Application (continued)

The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain. The contribution of  $R_G$  to gain accuracy and drift can be directly inferred from the gain Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. To maintain stability, avoid parasitic capacitance of more than a few picofarads at the  $R_G$  connections. Careful matching of any parasitics on both  $R_G$  pins maintains optimal CMRR over frequency.

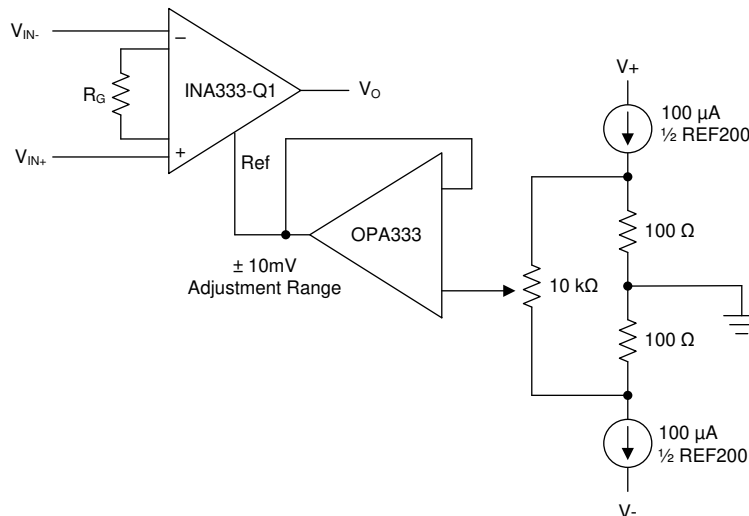
**Table 1. Commonly-Used Gains and Resistor Values**

DESIRED GAIN	$R_G$ ( $\Omega$ )	NEAREST 1% $R_G$ ( $\Omega$ )
1	NC <sup>(1)</sup>	NC
2	100k	100k
5	25k	24.9k
10	11.1k	11k
20	5.26k	5.23k
50	2.04k	2.05
100	1.01k	1k
200	502.5	499
500	200.4	200
1000	100.1	100

(1) NC denotes no connection. When using the SPICE model, the simulation will not converge unless a resistor is connected to the  $R_G$  pins; use a very large resistor value.

### 8.2.2.2 Offset Trimming

Most applications require no external offset adjustment; however, if necessary, adjustments can be made by applying a voltage to the REF pin. Figure 33 shows an optional circuit for trimming the output offset voltage. The voltage applied to REF pin is summed at the output. The operational amplifier buffer provides low impedance at the REF pin to preserve good common-mode rejection.



**Figure 33. Optional Trimming of Output Offset Voltage**



### 8.2.2.3 Noise Performance

The auto-calibration technique used by the INA333-Q1 results in reduced low frequency noise, typically only 50 nV/√Hz (G = 100). The spectral noise density is shown in detail in Figure 8. The low-frequency noise of the INA333-Q1 is approximately 1 μV<sub>PP</sub> measured from 0.1 Hz to 10 Hz (G = 100).

### 8.2.2.4 Input Bias Current Return Path

The input impedance of the INA333-Q1 is extremely high; approximately 100 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically ±70 pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 34 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA333-Q1, and the input amplifiers will saturate. If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 34). With higher source impedance, use two equal resistors to provide a balanced input with the possible advantages of a lower input offset voltage as a result of bias current, and improved high-frequency common-mode rejection.

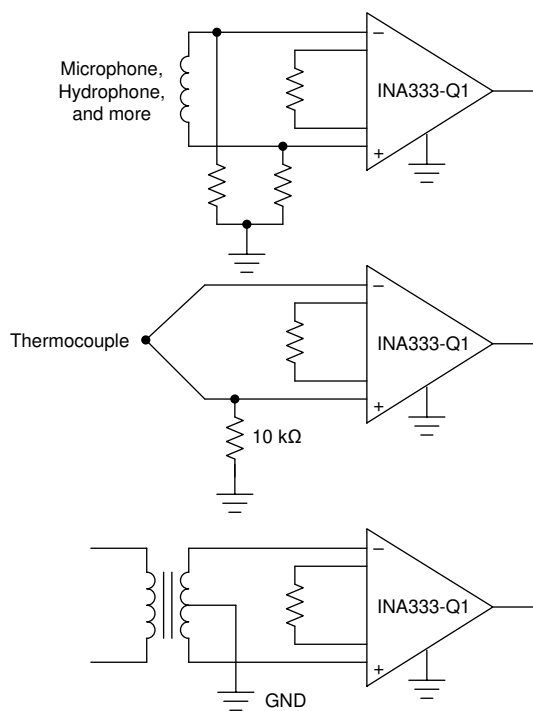


Figure 34. Providing an Input Common-Mode Current Path

### 8.2.2.5 Low Voltage Operation

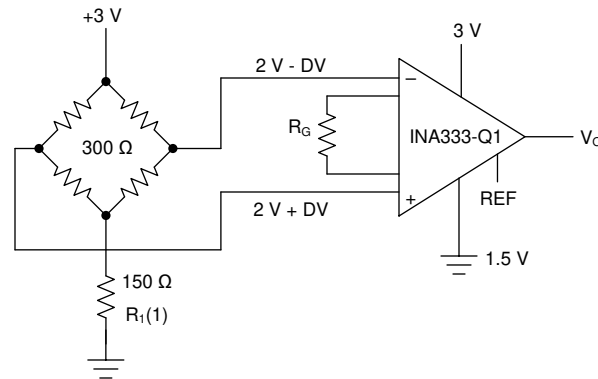
The INA333-Q1 can be operated on power supplies as low as  $\pm 0.9$  V. Most parameters vary only slightly throughout this supply voltage range; see the [Typical Characteristics](#) section. Operation at very-low supply voltage requires careful attention to make sure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. [Figure 20](#) to [Figure 23](#) show the range of linear operation for various supply voltages and gains.

### 8.2.2.6 Single-Supply Operation

The INA333-Q1 can be used on single power supplies of 1.8 V to 5.5 V. [Figure 35](#) shows a basic single-supply circuit. The output REF pin is connected to midsupply. Zero differential input voltage demands an output voltage of midsupply. Actual output voltage swing is limited to approximately 50 mV more than ground, when the load is referred to ground, as shown. [Figure 29](#) shows how the output voltage swing varies with output current.

With single-supply operation,  $V_{IN+}$  and  $V_{IN-}$  must both be 0.1 V greater than ground for linear operation. For instance, the inverting input cannot be connected to ground to measure a voltage connected to the noninverting input.

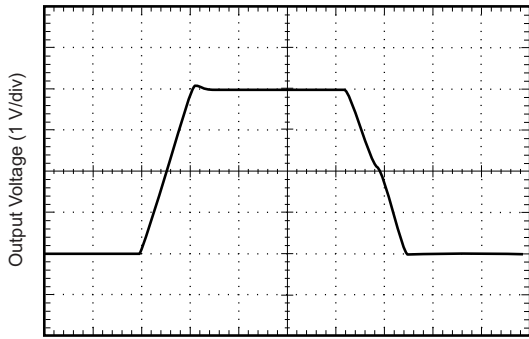
To show the issues affecting low voltage operation, consider the circuit in [Figure 35](#) that shows the INA333-Q1 operating from a single 3-V supply. A resistor in series with the low side of the bridge makes sure that the bridge output voltage is within the common-mode range of the amplifier inputs.



- (1)  $R_1$  creates proper common-mode voltage, only for low-voltage operation; see the [Single-Supply Operation](#) section.

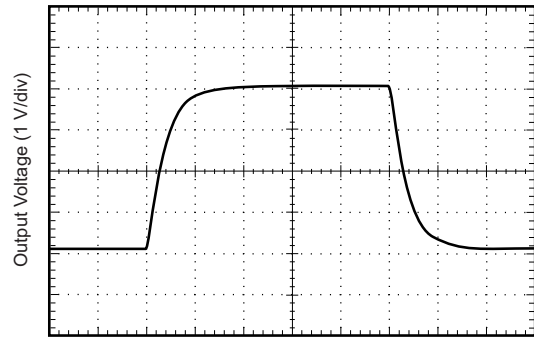
**Figure 35. Single-Supply Bridge Amplifier**

**8.2.3 Application Curves**



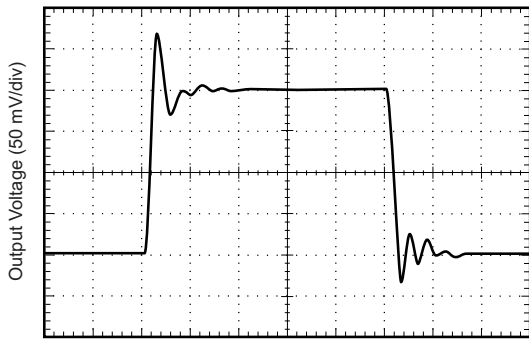
Time (25  $\mu$ s/div)

**Figure 36. Large Signal Response**



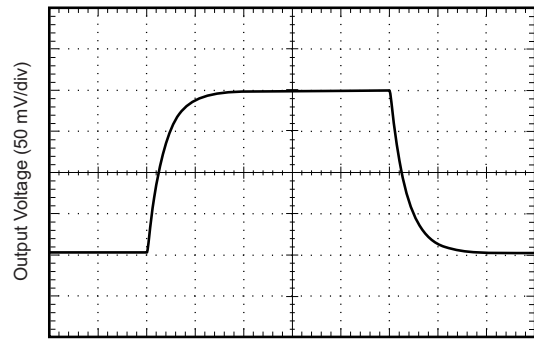
Time (100  $\mu$ s/div)

**Figure 37. Large-Signal Step Response**



Time (10  $\mu$ s/div)

**Figure 38. Small-Signal Step Response**



Time (100  $\mu$ s/div)

**Figure 39. Small-Signal Step Response**

**ADVANCE INFORMATION**

## 9 Power Supply Recommendations

The minimum power supply voltage for INA333-Q1 is 1.8 V, and the maximum power supply voltage is 5.5 V; for specified performance, 3.3 V to 5 V is recommended. Add a bypass capacitor at the input to compensate for the layout and power supply source impedance.

## 10 Layout

### 10.1 Layout Guidelines

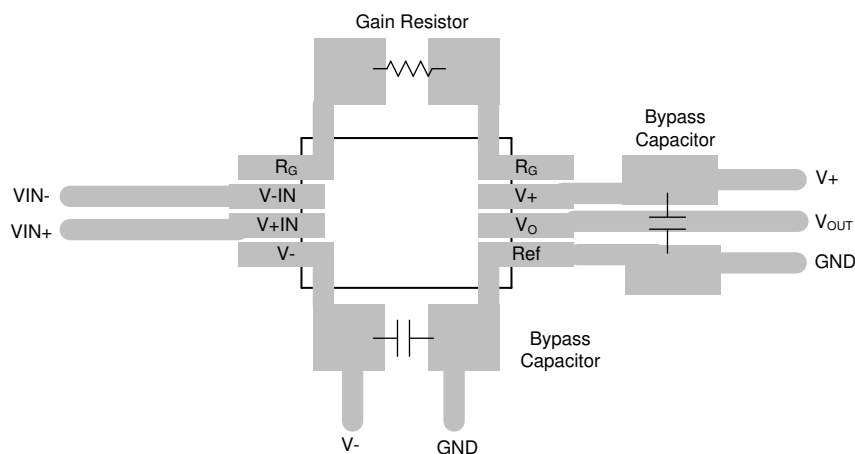
Attention to good layout practices is always recommended.

- Keep traces short.
- When possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible.
- Place a 0.1- $\mu$ F bypass capacitor closely across the supply pins.

These guidelines should be applied throughout the analog circuit to improve performance, and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

Instrumentation amplifiers vary in susceptibility to radio-frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The INA333-Q1 has been specifically designed to minimize susceptibility to RFI by incorporating passive RC filters with an 8-MHz corner frequency at the  $V_{IN+}$  and  $V_{IN-}$  inputs. As a result, the INA333-Q1 demonstrates remarkably low sensitivity compared to previous-generation devices. Strong RF fields may continue to cause varying offset levels, however, and may require additional shielding.

### 10.2 Layout Example



**Figure 40. Layout Example**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

##### 11.1.1.1 TINA-TI (Free Download Software)

#### Using TINA-TI SPICE-Based Analog Simulation Program with the INA333-Q1

TINA is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. It provides all the conventional dc, transient, and frequency domain analysis of SPICE as well as additional design capabilities.

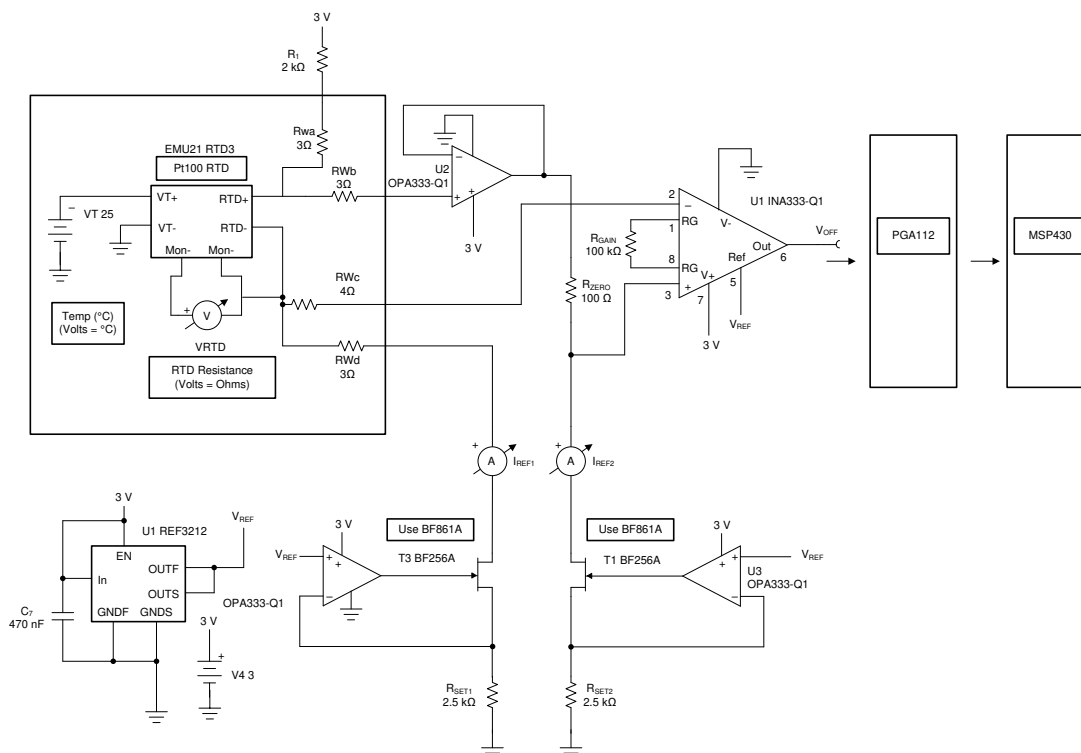
Available as a free download from the [Analog eLab Design Center](#), TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways.

Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Figure 41 shows example TINA-TI circuits for the INA333-Q1 device that can be used to develop, modify, and assess the circuit design for specific applications. Links to download these simulation files are given below.

#### NOTE

These files require that either the TINA software (from DesignSoft) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.



RW<sub>a</sub>, RW<sub>b</sub>, RW<sub>c</sub>, and RW<sub>d</sub> simulate wire resistance. These resistors are included to show the four-wire sense technique immunity to line mismatches. This method assumes the use of a four-wire RTD.

**Figure 41. Four-Wire, 3-V Conditioner for a PT100 RTD With Programmable Gain Acquisition System**

Download the TINA-TI simulation file for this circuit with the following link: [PT100 RTD](#).

## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [OPA188-Q1 Precision, Low-Noise, Rail-to-Rail Output, 36-V, Zero-Drift, Automotive-Grade Operational Amplifier data sheet](#)
- Texas Instruments, [OPA333-Q1 1.8-V microPower CMOS Operational Amplifier Zero-Drift Series data sheet](#)
- Texas Instruments, [Circuit board layout techniques](#)

### 11.3 Trademarks

All trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA333QDGKRQ1	PREVIEW	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		
PINA333QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF INA333-Q1 :**

- Catalog: [INA333](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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