1 Features

- Internally Trimmed Offset Voltage: 0.5 mV (Max)
- Input Offset Voltage Drift: 7 μV/°C (Typ)
- Low Input Bias Current: 50 pA
- Low Input Noise Current: 0.01 pA/√Hz
- Wide Gain Bandwidth: 3 MHz (Min)
- High Slew Rate: 10 V/μs (Min)
- Low Supply Current: 1.8 mA
- High Input Impedance: 10^{12} Ω
- Low Total Harmonic Distortion: ≤0.02%
- Low 1/f Noise Corner: 50 Hz
- Fast Settling Time to 0.01%: 2 μs

2 Applications

- High Speed Integrators
- Fast D/A Converters
- Sample and Hold Circuits

3 Description

These devices are low-cost, high-speed, JFET input operational amplifiers with very low input offset voltage and input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LF411-N</td>
<td>8-Pin PDIP</td>
<td>9.59mm×6.35mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E

- Added Handling Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ............................................................... 1
- Changed Input Offset Voltage Drift Feature from Max to Typ. ................................. 1
- Deleted the word “specified” in first sentence of Description paragraph.......................... 1
- Deleted note. .................................................................................................................. 5
- Deleted $\Delta V_{OS}/\Delta T$ Max specification for LM411A..................................................... 5
- Deleted $\Delta V_{OS}/\Delta T$ Max specification for LM411. .................................................................. 5

Changes from Revision C (March 2013) to Revision D

- Changed layout of National Data Sheet to TI format ..................................................... 12
5 Pin Configuration and Functions

NOTE: See Package Number NEV0008A
NOTE: Pin 4 connected to case.

Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Balance</td>
<td>1</td>
<td>I</td>
</tr>
<tr>
<td>Inverting</td>
<td>2</td>
<td>Input</td>
</tr>
<tr>
<td>Non-Inverting</td>
<td>3</td>
<td>Input</td>
</tr>
<tr>
<td>V-</td>
<td>4</td>
<td>P</td>
</tr>
<tr>
<td>Balance</td>
<td>5</td>
<td>I</td>
</tr>
<tr>
<td>Output</td>
<td>6</td>
<td>O</td>
</tr>
<tr>
<td>V+</td>
<td>7</td>
<td>P</td>
</tr>
<tr>
<td>NC</td>
<td>8</td>
<td>NC</td>
</tr>
</tbody>
</table>

NOTE: See Package Number P0008E
## 6 Specifications

### 6.1 Absolute Maximum Ratings \(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>LF411A</th>
<th>LF411</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>±22</td>
<td>±18</td>
<td>V</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>±38</td>
<td>±30</td>
<td>V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>±19</td>
<td>±15</td>
<td>V</td>
</tr>
<tr>
<td>Output Short Circuit Duration</td>
<td>Continuous</td>
<td>Continuous</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>TO Package</th>
<th>PDIP Package</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td>Power Dissipation (^{(3)}) (^{(4)})</td>
<td>150</td>
<td>115</td>
<td>670</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>See (^{(5)})</td>
<td>See (^{(5)})</td>
<td>°C</td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 s)</td>
<td>260</td>
<td>260</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.

\(^{(2)}\) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

\(^{(3)}\) For operating at elevated temperature, these devices must be derated based on a thermal resistance of θJA.

\(^{(4)}\) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside specified limits.

\(^{(5)}\) These devices are available in both the commercial temperature range \(0°C ≤ T_A ≤ 70°C\) and the military temperature range \(-55°C ≤ T_A ≤ 125°C\). The temperature range is designated by the position just before the package type in the device number. A “C” indicates the commercial temperature range and an “M” indicates the military temperature range. The military temperature range is available in the TO package only.

### 6.2 Handling Ratings

<table>
<thead>
<tr>
<th>Tstg</th>
<th>Storage temperature range</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
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<tbody>
<tr>
<td>Supply Voltage LF411A</td>
<td></td>
<td>±20</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Supply Voltage LF411</td>
<td></td>
<td>±15</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

### 6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (^{(1)})</th>
<th>TO</th>
<th>PDIP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 PINS</td>
<td>8 PINS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>Still Air</td>
<td>162</td>
<td>°C/W</td>
</tr>
<tr>
<td>400 LF/min Air Flow</td>
<td>65</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>120</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_{JC}) Junction-to-case (top) thermal resistance</td>
<td>20</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
### 6.5 DC Electrical Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>LF411A</th>
<th>LF411</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
</tr>
<tr>
<td>V&lt;sub&gt;OS&lt;/sub&gt;</td>
<td>Input Offset Voltage</td>
<td>R&lt;sub&gt;S&lt;/sub&gt;=10 kΩ, TA=25°C</td>
<td>0.3</td>
<td>0.5</td>
</tr>
<tr>
<td>∆V&lt;sub&gt;OS&lt;/sub&gt;/ΔT</td>
<td>Average TC of Input Offset Voltage</td>
<td>R&lt;sub&gt;S&lt;/sub&gt;=10 kΩ</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>I&lt;sub&gt;OS&lt;/sub&gt;</td>
<td>Input Offset Current</td>
<td>V&lt;sub&gt;G&lt;/sub&gt;=±15V (2) (3)</td>
<td>T&lt;sub&gt;j&lt;/sub&gt;=25°C</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T&lt;sub&gt;j&lt;/sub&gt;=70°C</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T&lt;sub&gt;j&lt;/sub&gt;=125°C</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>I&lt;sub&gt;B&lt;/sub&gt;</td>
<td>Input Bias Current</td>
<td>V&lt;sub&gt;G&lt;/sub&gt;=±15V (2) (3)</td>
<td>T&lt;sub&gt;j&lt;/sub&gt;=25°C</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T&lt;sub&gt;j&lt;/sub&gt;=70°C</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T&lt;sub&gt;j&lt;/sub&gt;=125°C</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>R&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Input Resistance</td>
<td>T&lt;sub&gt;j&lt;/sub&gt;=25°C</td>
<td>1012</td>
<td>1012</td>
</tr>
<tr>
<td>A&lt;sub&gt;VOL&lt;/sub&gt;</td>
<td>Large Signal Voltage Gain</td>
<td>V&lt;sub&gt;G&lt;/sub&gt;=±15V, V&lt;sub&gt;Q&lt;/sub&gt;=±10V, R&lt;sub&gt;L&lt;/sub&gt;=2k, TA=25°C</td>
<td>50</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Over Temperature</td>
<td>25</td>
<td>200</td>
</tr>
<tr>
<td>V&lt;sub&gt;O&lt;/sub&gt;</td>
<td>Output Voltage Swing</td>
<td>V&lt;sub&gt;G&lt;/sub&gt;=±15V, R&lt;sub&gt;L&lt;/sub&gt;=10k</td>
<td>±12</td>
<td>±13.5</td>
</tr>
<tr>
<td>V&lt;sub&gt;CM&lt;/sub&gt;</td>
<td>Input Common-Mode Voltage Range</td>
<td></td>
<td>±16</td>
<td>+19.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-16.5</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td>R&lt;sub&gt;S&lt;/sub&gt;≤10kΩ</td>
<td>80</td>
<td>100</td>
</tr>
<tr>
<td>PSRR</td>
<td>Supply Voltage Rejection Ratio</td>
<td></td>
<td>80</td>
<td>100</td>
</tr>
<tr>
<td>I&lt;sub&gt;S&lt;/sub&gt;</td>
<td>Supply Current</td>
<td></td>
<td>1.8</td>
<td>2.8</td>
</tr>
</tbody>
</table>

(1) RETS 411X for LF411MH and LF411MJ military specifications.
(2) Unless otherwise specified, the specifications apply over the full temperature range and for V<sub>G</sub>=±20V for the LF411A and for V<sub>G</sub>=±15V for the LF411. V<sub>OS</sub>, I<sub>B</sub>, and I<sub>OS</sub> are measured at V<sub>CM</sub>=0.
(3) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T<sub>j</sub>. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P<sub>D</sub>. T<sub>j</sub>=T<sub>A</sub>+θ<sub>jA</sub>P<sub>D</sub> where θ<sub>jA</sub> is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
(4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from ±15V to ±5V for the LF411A and from ±20V to ±5V for the LF411.

### 6.6 AC Electrical Characteristics

<table>
<thead>
<tr>
<th>PARAMETER&lt;sup&gt;(1)(2)&lt;/sup&gt;</th>
<th>TEST CONDITIONS</th>
<th>LF411A</th>
<th>LF411</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>V&lt;sub&gt;G&lt;/sub&gt;=±15V, TA=25°C</td>
<td>10</td>
<td>15</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain-Bandwidth Product</td>
<td>V&lt;sub&gt;G&lt;/sub&gt;=±15V, TA=25°C</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>e&lt;sub&gt;n&lt;/sub&gt;</td>
<td>Equivalent Input Noise Voltage</td>
<td>TA=25°C, R&lt;sub&gt;S&lt;/sub&gt;=100Ω, f=1 kHz</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;n&lt;/sub&gt;</td>
<td>Equivalent Input Noise Current</td>
<td>TA=25°C, f=1 kHz</td>
<td>0.01</td>
<td>0.01</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
<td>AV=±10, RL=10kΩ, V&lt;sub&gt;O&lt;/sub&gt;=20 Vp-p, BW=20 Hz−20 kHz</td>
<td>&lt;0.02</td>
<td></td>
</tr>
</tbody>
</table>

(1) Unless otherwise specified, the specifications apply over the full temperature range and for V<sub>G</sub>=±20V for the LF411A and for V<sub>G</sub>=±15V for the LF411. V<sub>OS</sub>, I<sub>B</sub>, and I<sub>OS</sub> are measured at V<sub>CM</sub>=0.
(2) RETS 411X for LF411MH and LF411MJ military specifications.
## 6.7 Typical Performance Characteristics

<table>
<thead>
<tr>
<th>Figure 1. Input Bias Current</th>
<th>Figure 2. Input Bias Current</th>
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<tr>
<td><img src="image1.png" alt="Input Bias Current" /></td>
<td><img src="image2.png" alt="Input Bias Current" /></td>
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</table>

<table>
<thead>
<tr>
<th>Figure 3. Supply Current</th>
<th>Figure 4. Positive Common-Mode Input Voltage Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image3.png" alt="Supply Current" /></td>
<td><img src="image4.png" alt="Positive Common-Mode Input Voltage Limit" /></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Figure 5. Negative Common-Mode Input Voltage Limit</th>
<th>Figure 6. Positive Current Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image5.png" alt="Negative Common-Mode Input Voltage Limit" /></td>
<td><img src="image6.png" alt="Positive Current Limit" /></td>
</tr>
</tbody>
</table>
Typical Performance Characteristics (continued)

Figure 7. Negative Current Limit

Figure 8. Output Voltage Swing

Figure 9. Output Voltage Swing

Figure 10. Gain Bandwidth

Figure 11. Bode Plot

Figure 12. Slew Rate

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Submit Documentation Feedback
Typical Performance Characteristics (continued)

Figure 13. Distortion vs Frequency

Figure 14. Undistorted Output Voltage Swing

Figure 15. Open Loop Frequency Response

Figure 16. Common-Mode Rejection Ratio

Figure 17. Power Supply Rejection Ratio

Figure 18. Equivalent Input Noise Voltage
Typical Performance Characteristics (continued)

Figure 19. Open Loop Voltage Gain

Figure 20. Output Impedance

Figure 21. Inverter Settling Time
6.8 Pulse Response ($R_L=2 \, k\Omega$, $C_L=10 \, pF$)

Figure 22. Small Signal Inverting

Figure 23. Small Signal Non-Inverting

Figure 24. Large Signal Inverting

Figure 25. Large Signal Non-Inverting

Figure 26. Current Limit ($R_L = 100 \, \Omega$)
7 Detailed Description

7.1 Overview

These devices are low-cost, high-speed, JFET input operational amplifiers with very low input offset voltage and input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

7.2 Functional Block Diagram

7.3 Feature Description

The amplifier’s differential inputs consist of a non-inverting input (+IN) and an inverting input (-IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp \( V_{OUT} \) is given by the equation \( V_{OUT} = A_{OL}(IN+ - IN-) \).

7.4 Device Functional Modes

7.4.1 Simplified Schematic

![Figure 27. Simplified Schematic](image)
Device Functional Modes (continued)

7.4.2 Detailed Schematic

Figure 28. Detailed Schematic
8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LF411 series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

8.2 Typical Applications

1. High Speed Current Booster
2. 10-Bit Linear DAC with No $V_{OS}$ Adjust
3. Single Supply Analog Switch with Buffered Output

8.2.1 High-Speed Current Booster

[Image of circuit diagram]

Figure 29. High-Speed Current Booster
Typical Applications (continued)

8.2.1.1 Design Requirements

PNP = 2N2905
NPN = 2N2219
TO-5 heat sinks for Q6-Q7
±15V supplies.

8.2.1.2 Detailed Design Procedure

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.
Typical Applications (continued)

8.2.2 10-Bit Linear DAC with No V_{OS} Adjust

![Diagram of 10-Bit Linear DAC with No V_{OS} Adjust]

\[ V_{OUT} = -V_{REF} \left( \frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \ldots + \frac{A_{10}}{1024} \right) \]

\[-10V \leq V_{REF} \leq 10V\]

\[0 \leq V_{OUT} \leq \frac{1023}{1024} V_{REF}\]

where \(A_{N}=1\) if the \(A_N\) digital input is high

\(A_{N}=0\) if the \(A_N\) digital input is low

Figure 30. 10-Bit Linear DAC with No V_{OS} Adjust

8.2.2.1 Design Requirements

\(\pm 15V\) supplies.

8.2.2.2 Detailed Design Procedure

See Section 9.2.1.2.

8.2.3 Single Supply Analog Switch With Buffered Output

![Diagram of Single Supply Analog Switch With Buffered Output]

Figure 31. Single Supply Analog Switch With Buffered Output

8.2.3.1 Design Requirements

Single 12V supply.

8.2.3.2 Detailed Design Procedure

See Section 9.2.1.2.
9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 0.1µF capacitors be placed as close as possible to the op amp power supply pins. The minimum power supply voltage is ±5V.

10 Layout

10.1 Layout Guidelines

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

10.2 Layout Example

![LF411-N Layout Diagram](image-url)

Figure 32. LF411-N Layout
11 Device and Documentation Support

11.1 Trademarks
All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LF411ACN/NOPB</td>
<td>LIFEBUY</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>Call TI</td>
<td>Level-1-NA-UNLIM</td>
<td>0 to 70</td>
<td>LF 411ACN</td>
<td></td>
</tr>
<tr>
<td>LF411CN/NOPB</td>
<td>LIFEBUY</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-NA-UNLIM</td>
<td>0 to 70</td>
<td>LF 411CN</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
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