FEATURES

- High Efficiency Sleep Mode
- 40 µA Typical Iq in Sleep Mode
- 10 µA Typical Iq in Shutdown Mode
- 3.0V Minimum Input Voltage
- 4.0V to 18V Continuous Input Range
- 2.0% Reference Accuracy
- Cycle-by-Cycle Current Limit
- Adjustable Frequency (150 kHz to 500 kHz)
- Synchronizable to an External Clock
- Power Good Flag
- Forced PWM Function
- Adjustable Soft-Start
- HTSSOP-16 Exposed Pad Package
- Thermal Shut Down

APPLICATIONS

- Automotive Telematics
- Navigation Systems
- In-Dash Instrumentation
- Battery Powered Applications
- Stand-by Power for Home Gateways/Set-Top Boxes

DESCRIPTION

The LM26001B is a switching regulator designed for the high efficiency requirements of applications with stand-by modes. The device features a low-current sleep mode to maintain efficiency under light-load conditions and current-mode control for accurate regulation over a wide input voltage range. Quiescent current is reduced to 10 µA typically in shutdown mode and less than 40 µA in sleep mode. Forced PWM mode is also available to disable sleep mode.

The LM26001B can deliver up to 1.5A of continuous load current with a fixed current limit, through the internal N-channel switch. The part has a wide input voltage range of 4.0V to 18V and can operate with input voltages as low as 3V during line transients.

Operating frequency is adjustable from 150 kHz to 500 kHz with a single resistor and can be synchronized to an external clock.

Other features include Power good, adjustable soft-start, enable pin, input under-voltage protection, and an internal bootstrap diode for reduced component count.
Pin Descriptions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VIN</td>
<td>Power supply input</td>
</tr>
<tr>
<td>2</td>
<td>VIN</td>
<td>Power supply input</td>
</tr>
<tr>
<td>3</td>
<td>PGOOD</td>
<td>Power Good pin. An open drain output which goes high when the output voltage is greater than 92% of nominal.</td>
</tr>
<tr>
<td>4</td>
<td>EN</td>
<td>Enable is an analog level input pin. When pulled below 0.8V, the device enters shutdown mode.</td>
</tr>
<tr>
<td>5</td>
<td>SS</td>
<td>Soft-start pin. Connect a capacitor from this pin to GND to set the soft-start time.</td>
</tr>
<tr>
<td>6</td>
<td>COMP</td>
<td>Compensation pin. Connect to a resistor capacitor pair to compensate the control loop.</td>
</tr>
<tr>
<td>7</td>
<td>FB</td>
<td>Feedback pin. Connect to a resistor divider between Vout and GND to set output voltage.</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>9</td>
<td>FREQ</td>
<td>Frequency adjust pin. Connect a resistor from this pin to GND to set the operating frequency.</td>
</tr>
<tr>
<td>10</td>
<td>FPWM</td>
<td>FPWM is a logic level input pin. For normal operation, connect to GND. When pulled high, sleep mode operation is disabled.</td>
</tr>
<tr>
<td>11</td>
<td>SYNC</td>
<td>Frequency synchronization pin. Connect to an external clock signal for synchronized operation. SYNC must be pulled low for non-synchronized operation.</td>
</tr>
<tr>
<td>12</td>
<td>VBIAS</td>
<td>Connect to an external 3V or greater supply to bypass the internal regulator for improved efficiency. If not used, VBIAS should be tied to GND.</td>
</tr>
<tr>
<td>13</td>
<td>VDD</td>
<td>The output of the internal regulator. Bypass with a minimum 1.0 μF capacitor.</td>
</tr>
<tr>
<td>14</td>
<td>BOOT</td>
<td>Bootstrap capacitor pin. Connect a 0.1μF minimum ceramic capacitor from this pin to SW to generate the gate drive bootstrap voltage.</td>
</tr>
<tr>
<td>15</td>
<td>SW</td>
<td>Switch pin. The source of the internal N-channel switch.</td>
</tr>
<tr>
<td>16</td>
<td>SW</td>
<td>Switch pin. The source of the internal N-channel switch.</td>
</tr>
<tr>
<td>EP</td>
<td>EP</td>
<td>Exposed Pad thermal connection. Connect to GND.</td>
</tr>
</tbody>
</table>

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.
### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>-0.3V to 20V</td>
</tr>
<tr>
<td>SW</td>
<td>-0.5V to 20V</td>
</tr>
<tr>
<td>VDD</td>
<td>-0.3V to 7V</td>
</tr>
<tr>
<td>VBIAS</td>
<td>-0.3V to 10V</td>
</tr>
<tr>
<td>FB</td>
<td>-0.3V to 6V</td>
</tr>
<tr>
<td>BOOT</td>
<td>SW-0.3V to SW+7V</td>
</tr>
<tr>
<td>PGOOD</td>
<td>-0.3V to 7V</td>
</tr>
<tr>
<td>FREQ</td>
<td>-0.3V to 7V</td>
</tr>
<tr>
<td>SYNC</td>
<td>-0.3V to 7V</td>
</tr>
<tr>
<td>EN</td>
<td>-0.3V to 20V</td>
</tr>
<tr>
<td>FPWM</td>
<td>-0.3V to 7V</td>
</tr>
<tr>
<td>SS</td>
<td>-0.3V to 7V</td>
</tr>
</tbody>
</table>

#### Storage Temperature
-65°C to +150°C

### Power Dissipation
2.6 W

### Recommended Lead Temperature
- Vapor Phase (70s): 215°C
- Infrared (15s): 220°C

### ESD Susceptibility
- Machine Model: 200V
- Human Body Model: 2KV
- Charged Device Model: 1kV

---

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.

2. The absolute maximum specification applies to DC voltage. An extended negative voltage limit of -2V applies for a pulse of up to 1µs, and -1V for a pulse of up to 20µs.

3. The maximum allowable power dissipation is a function of the maximum junction temperature, \( T_{J_{\text{MAX}}} \), the junction-to-ambient thermal resistance, \( \theta_{JA} \), and the ambient temperature, \( T_A \). The maximum allowable power dissipation at any ambient temperature is calculated using:

   \[
   P_{D_{\text{MAX}}} = \frac{(T_{J_{\text{MAX}}} - T_A)}{\theta_{JA}}
   \]

   The maximum power dissipation of 2.6W is determined using \( T_A = 25°C \), \( \theta_{JA} = 38°C/W \), and \( T_{J_{\text{MAX}}} = 125°C \).

4. The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. The charged device model is per JESD22-C101-C.

---

### Operating Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Junction Temp.</td>
<td>-40°C to 125°C</td>
</tr>
<tr>
<td>Supply Voltage (2)</td>
<td>3.0V to 18V</td>
</tr>
</tbody>
</table>

---

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.

2. Below 4.0V input, power dissipation may increase due to increased \( R_{D\text{SON}} \). Therefore, a minimum input voltage of 4.0V is required to operate continuously within specification. A minimum of 3.9V (typical) is also required for startup.
Electrical Characteristics

Specifications in standard type are for $T_J = 25^\circ C$ only, and limits in boldface type apply over the junction temperature ($T_J$) range of -40°C to +125°C. Unless otherwise stated, $V_{IN} = 12V$. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ C$, and are provided for reference purposes only\(^{(1)}\).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{SD}$ (^{(2)})</td>
<td>Shutdown Current</td>
<td>$EN = 0V$</td>
<td>10.8</td>
<td>20</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{q_Sleep_VB}$ (^{(2)})</td>
<td>Quiescent Current</td>
<td>Sleep mode, $V_{BIAS} = 5V$</td>
<td>38</td>
<td>70</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{q_Sleep_VDD}$</td>
<td>Quiescent Current</td>
<td>Sleep mode, $V_{BIAS} = GND$</td>
<td>75</td>
<td>125</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{q_PWM_VB}$</td>
<td>Quiescent Current</td>
<td>PWM mode, $V_{BIAS} = 5V$</td>
<td>150</td>
<td>230</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{q_PWM_VDD}$</td>
<td>Quiescent Current</td>
<td>PWM mode, $V_{BIAS} = GND$</td>
<td>0.65</td>
<td>0.85</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{BIAS_Sleep}$ (^{(2)})</td>
<td>Bias Current</td>
<td>Sleep mode, $V_{BIAS} = 5V$</td>
<td>33</td>
<td>85</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{BIAS_PWM}$</td>
<td>Bias Current</td>
<td>PWM mode, $V_{BIAS} = 5V$</td>
<td>0.5</td>
<td>0.70</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_{FB}$</td>
<td>Feedback Voltage</td>
<td>$5V &lt; V_{IN} &lt; 18V$</td>
<td>1.2093</td>
<td>1.234</td>
<td>1.2589</td>
<td>V</td>
</tr>
<tr>
<td>$I_{FB}$</td>
<td>FB Bias Current</td>
<td></td>
<td>±200</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{OUT}/\Delta V_{IN}$</td>
<td>Vout Line Regulation</td>
<td>$5V &lt; V_{IN} &lt; 18V$</td>
<td>0.001</td>
<td>%/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{OUT}/\Delta I_{OUT}$</td>
<td>Vout Load Regulation</td>
<td>$0.8V &lt; V_{COMP} &lt; 1.15V$</td>
<td>0.07</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>VDD Output Voltage</td>
<td>$7V &lt; V_{IN} &lt; 18V$, $I_{VDD} = 0$ mA to 5 mA</td>
<td>5.50</td>
<td>5.95</td>
<td>6.50</td>
<td>V</td>
</tr>
<tr>
<td>$I_{SS_Source}$</td>
<td>Soft-Start Source Current</td>
<td></td>
<td>1.5</td>
<td>2.2</td>
<td>4.6</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{bias_in}$</td>
<td>VBIAS On Voltage</td>
<td>Specified at $I_{BIAS} = 92.5%$ of full value</td>
<td>2.64</td>
<td>2.9</td>
<td>3.07</td>
<td>V</td>
</tr>
</tbody>
</table>

**Switching**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DS(ON)}$</td>
<td>Switch On Resistance</td>
<td>$I_{SW} = 1A$</td>
<td>0.12</td>
</tr>
<tr>
<td>$I_{Fsw_off}$</td>
<td>Switch Off State Leakage Current</td>
<td>$V_{IN} = 18V$, $V_{SW} = 0V$</td>
<td>0.002</td>
</tr>
<tr>
<td>$f_{SW}$</td>
<td>Switching Frequency</td>
<td>$RFREQ = 62k$, 124k, 240k</td>
<td>$\pm 10%$</td>
</tr>
<tr>
<td>$V_{FREQ}$</td>
<td>FREQ Voltage</td>
<td></td>
<td>1.0</td>
</tr>
<tr>
<td>$f_{SW_range}$</td>
<td>Switching Frequency Range</td>
<td></td>
<td>150</td>
</tr>
<tr>
<td>$V_{SYNC}$</td>
<td>Sync Pin Threshold</td>
<td>SYNC rising</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SYNC falling</td>
<td>0.8</td>
</tr>
<tr>
<td>$I_{SYNC}$</td>
<td>SYNC Leakage Current</td>
<td></td>
<td>114</td>
</tr>
<tr>
<td>$F_{SYNC_UP}$</td>
<td>Upper frequency synchronization range</td>
<td>As compared to nominal $f_{SW}$</td>
<td>+30</td>
</tr>
<tr>
<td>$F_{SYNC_DN}$</td>
<td>Lower frequency synchronization range</td>
<td>As compared to nominal $f_{SW}$</td>
<td>-20</td>
</tr>
<tr>
<td>$T_{OFMIN}$</td>
<td>Minimum Off-time</td>
<td></td>
<td>365</td>
</tr>
<tr>
<td>$T_{ONMIN}$</td>
<td>Minimum On-time</td>
<td></td>
<td>155</td>
</tr>
<tr>
<td>$TH_{SLEEP_HYS}$</td>
<td>Sleep Mode Threshold Hysteresis</td>
<td>$V_{FB}$ rising, % of $TH_{WAKE}$</td>
<td>101.2</td>
</tr>
<tr>
<td>$TH_{WAKE}$</td>
<td>Wake Up Threshold</td>
<td>Measured at falling $FB$, $COMP = 0.6V$</td>
<td>1.234</td>
</tr>
<tr>
<td>$I_{BOOT}$</td>
<td>BOOT Pin Leakage Current</td>
<td>$BOOT = 16V$, $SW = 10V$</td>
<td>0.0006</td>
</tr>
</tbody>
</table>

\(^{(1)}\) All room temperature limits are 100% production tested. All limits at temperature extremes are specified through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

\(^{(2)}\) $Iq$ and $ISD$ specify the current into the $VIN$ pin. $IBIAS$ is the current into the $VBIAS$ pin when the $VBIAS$ voltage is greater than 3V. All quiescent current specifications apply to non-switching operation.
### Electrical Characteristics (continued)

Specifications in standard type are for $T_J = 25^\circ C$ only, and limits in boldface type apply over the junction temperature ($T_J$) range of -40°C to +125°C. Unless otherwise stated, $V_{in}=12V$. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ C$, and are provided for reference purposes only(1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{LIMPK}$</td>
<td>Peak Current Limit</td>
<td></td>
<td>1.80</td>
<td>2.5</td>
<td>3.25</td>
<td>A</td>
</tr>
<tr>
<td>$V_{FB_SC}$</td>
<td>Short Circuit Frequency Foldback Threshold</td>
<td>Measured at FB falling</td>
<td>0.87</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$F_{\text{min}_sc}$</td>
<td>Min Frequency in Foldback</td>
<td>$V_{FB} &lt; 0.3V$</td>
<td>71</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>$V_{TH_PGOOD}$</td>
<td>Power Good Threshold</td>
<td>$V_{PGOOD}$ rising</td>
<td>89</td>
<td>92</td>
<td>95</td>
<td>%</td>
</tr>
<tr>
<td>$I_{PGOOD_HI}$</td>
<td>PGOOD Leakage Current</td>
<td>$V_{PGOOD} = 5V$</td>
<td>0.2</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$R_{DS_PGOOD}$</td>
<td>PGOOD On Resistance</td>
<td>$V_{PGOOD}$ sink current = 500 µA</td>
<td>64</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{UVLO}$</td>
<td>Under-Voltage Lock-Out Threshold</td>
<td>$V_{in}$ falling, shutdown, $V_{DD} = V_{IN}$</td>
<td>2.60</td>
<td>2.9</td>
<td>3.20</td>
<td>V</td>
</tr>
<tr>
<td>$V_{UVLO}$</td>
<td>Under-Voltage Lock-Out Threshold</td>
<td>$V_{in}$ rising, soft-start, $V_{DD} = V_{IN}$</td>
<td>3.60</td>
<td>3.9</td>
<td>4.20</td>
<td>V</td>
</tr>
<tr>
<td>$TSD$</td>
<td>Thermal Shutdown Threshold</td>
<td>Power dissipation = 1W, 0 lpfm air flow</td>
<td>160</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$\theta_{JA}$</td>
<td>Thermal Resistance</td>
<td>$P_{dissipation} = 1W$, 0 lpfm air flow</td>
<td>38</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>$V_{TH_EN}$</td>
<td>Enable Threshold voltage</td>
<td>Enable Hysteresis</td>
<td>0.8</td>
<td>1.2</td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>$I_{EN_Source}$</td>
<td>EN Source Current</td>
<td>EN = 0V</td>
<td>4.5</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$V_{TH_FPWM}$</td>
<td>FPWM Threshold</td>
<td>FPWM = 5V</td>
<td>0.8</td>
<td>1.2</td>
<td>1.6</td>
<td>V</td>
</tr>
<tr>
<td>$I_{FPWM}$</td>
<td>FPWM Leakage Current</td>
<td>FPWM = 5V</td>
<td>35</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$g_{m}$</td>
<td>Error Amp Trans-Conductance</td>
<td></td>
<td>400</td>
<td>670</td>
<td>1000</td>
<td>µmho</td>
</tr>
<tr>
<td>$I_{COMP}$</td>
<td>COMP Source Current</td>
<td>$V_{COMP} = 0.9V$</td>
<td>56</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$V_{COMP}$</td>
<td>COMP Pin Voltage Range</td>
<td></td>
<td>0.64</td>
<td>1.27</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

Copyright © 2007–2013, Texas Instruments Incorporated
Typical Performance Characteristics

Unless otherwise specified the following conditions apply: \( V_{\text{in}} = 12\, \text{V}, T_J = 25^\circ\text{C} \).

**Figure 2.**

VFB vs Temperature

**Figure 3.**

VFB vs \( V_{\text{in}} \)

**Figure 4.**

IQ and IVBIAS vs Temperature (Sleep Mode)

**Figure 5.**

IQ and IVBIAS vs Temperature (PWM Mode)

**Figure 6.**

Normalized Switching Frequency vs Temperature (300kHz)

**Figure 7.**

UVLO Threshold vs Temperature (\( V_{\text{DD}} = V_{\text{in}} \))
Typical Performance Characteristics (continued)

Unless otherwise specified the following conditions apply: Vin = 12V, TJ = 25°C.

**Peak Current Limit vs Temperature**

![Graph showing peak current limit vs temperature](image)

**Short Circuit Foldback Frequency vs V\_FB (325 kHz nominal)**

![Graph showing short circuit foldback frequency vs V\_FB](image)

**Efficiency vs Load Current (330kHz)**

![Graph showing efficiency vs load current (330kHz)](image)

**Efficiency vs Load Current (500kHz)**

![Graph showing efficiency vs load current (500kHz)](image)

**Startup Waveforms**

![Graph showing startup waveforms](image)
Typical Performance Characteristics (continued)

Unless otherwise specified the following conditions apply: Vin = 12V, T_j = 25°C.

**Load Transient Response**

![Load Transient Response](image)

**Low Input Voltage Dropout**

Nominal VOUT = 5V

![Low Input Voltage Dropout](image)
GENERAL

The LM26001B is a current mode PWM buck regulator. At the beginning of each clock cycle, the internal high-side switch turns on, allowing current to ramp up in the inductor. The inductor current is internally monitored during each switching cycle. A control signal derived from the inductor current is compared to the voltage control signal at the COMP pin, derived from the feedback voltage. When the inductor current reaches the threshold, the high-side switch is turned off and inductor current ramps down. While the switch is off, inductor current is supplied through the catch diode. This cycle repeats at the next clock cycle. In this way, duty cycle and output voltage are controlled by regulating inductor current. Current mode control provides superior line and load regulation. Other benefits include cycle by cycle current limiting and a simplified compensation scheme. Typical PWM waveforms are shown in Figure 15.
SLEEP MODE

In light load conditions, the LM26001B automatically switches into sleep mode for improved efficiency. As loading decreases, the voltage at FB increases and the COMP voltage decreases. When the COMP voltage reaches the 0.6V (typical) clamp threshold, and the FB voltage rises 1% above nominal, sleep mode is enabled and switching stops. The regulator remains in sleep mode until the FB voltage falls to the reset threshold, at which point switching resumes. This 1% FB window limits the corresponding output ripple to approximately 1% of nominal output voltage. The sleep cycle will repeat until load current is increased. Figure 16 shows typical switching and output voltage waveforms in sleep mode.

In sleep mode, quiescent current is reduced to less than 40 µA when not switching. The DC sleep mode threshold can be calculated according to the equation below:

\[
I_{\text{Sleep}} = I_{\text{lim}} + 0.13 \mu \left[ \frac{V_{\text{in}} - V_{\text{out}}}{L} \right]^2 \times \left[ \frac{f_{\text{sw}} \times L}{D \times 2 \times (V_{\text{in}} - V_{\text{out}})} \right]
\]

where

- \( I_{\text{lim}} = I_{\text{lim}/16} \) (2.5A/16 typically) and \( D = \) duty cycle, defined as \( (V_{\text{out}} + V_{\text{diode}})/V_{\text{in}} \)

When load current increases above this limit, the LM26001B is forced back into PWM operation. The sleep mode threshold varies with frequency, inductance, and duty cycle as shown in Figure 17.

Figure 15. PWM Waveforms
1A Load, Vin = 12V

Figure 16. Sleep Mode Waveforms
25mA Load, Vin = 12V
FPWM

Pulling the FPWM pin high disables sleep mode and forces the LM26001B to always operate in PWM mode. Light load efficiency is reduced in PWM mode, but switching frequency remains stable. The FPWM pin can be connected to the VDD pin to pull it high. In FPWM mode, under light load conditions, the regulator operates in discontinuous conduction mode (DCM). In discontinuous conduction mode, current through the inductor starts at zero and ramps up to its peak, then ramps down to zero again. Until the next cycle, the inductor current remains at zero. At nominal load currents, in FPWM mode, the device operates in continuous conduction mode, where positive current always flows in the inductor. Typical discontinuous operation waveforms are shown below.

At very light load, in FPWM mode, the LM26001B may enter sleep mode. This is to prevent an over-voltage condition from occurring. However, the FPWM sleep threshold is much lower than in normal operation.

ENABLE

The LM26001B provides a shutdown function via the EN pin to disable the device when the output voltage does not need to be maintained. EN is an analog level input with typically 120 mV of hysteresis. The device is active when the EN pin is above 1.2V (typical) and in shutdown mode when EN is below this threshold. When EN goes high, the internal VDD regulator turns on and charges the VDD capacitor. When VDD reaches 3.9V (typical), the soft-start pin begins to source current. In shutdown mode, the VDD regulator shuts down and total quiescent current is reduced to 10 µA (typical). Because the EN pin sources 4.5 µA (typical) of pull-up current, this pin can be left open or connected to VIN for always-on operation. When open, EN will be pulled up to VIN.
SOFT-START

The soft-start feature provides a controlled output voltage ramp up at startup. This reduces inrush current and eliminates output overshoot at turn-on. The soft-start pin, SS, must be connected to GND through a capacitor. At power-on, enable, or UVLO recovery, an internal 2.2 µA (typical) current charges the soft-start capacitor. During soft-start, the error amplifier output voltage is controlled by both the soft-start voltage and the feedback loop. As the SS pin voltage ramps up, the duty cycle increases proportional to the soft-start ramp, causing the output voltage to ramp up. The rate at which the duty cycle increases depends on the capacitance of the soft-start capacitor. The higher the capacitance, the slower the output voltage ramps up. The soft-start capacitor value can be calculated with the following equation:

$$CSS = \frac{Iss \times tss}{1.234V}$$  \hspace{1cm} (2)

Where \(tss\) is the desired soft-start time and \(Iss\) is the soft-start source current. During soft-start, current limit and synchronization remain in effect, while sleep mode and frequency foldback are disabled. Soft-start mode ends when the SS pin voltage reaches 1.23V typical. At this point, output voltage control is transferred to the FB pin and the SS pin is discharged.

CURRENT LIMIT

The peak current limit is set internally by directly measuring peak inductor current through the internal switch. To ensure accurate current sensing, VIN should be bypassed with a minimum 1µF ceramic capacitor placed directly at the pin.

When the inductor current reaches the current limit threshold, the internal FET turns off immediately allowing inductor current to ramp down until the next cycle. This reduction in duty cycle corresponds to a reduction in output voltage.

The current limit comparator is disabled for less than 100ns at the leading edge for increased immunity to switching noise.

Because the current limit monitors peak inductor current, the DC load current limit threshold varies with inductance and frequency. Assuming a minimum current limit of 1.80A, maximum load current can be calculated as follows:

$$I_{load_{\text{max}}} = 1.80A - \frac{I_{ripple}}{2}$$

where

- \(I_{ripple}\) is the peak-to-peak inductor ripple current, calculated as

$$I_{ripple} = \frac{(Vin - Vout) \times Vout}{f_{sw} \times L \times Vin}$$  \hspace{1cm} (3)

To find the worst case (lowest) current limit threshold, use the maximum input voltage and minimum current limit specification.

During high over-current conditions, such as output short circuit, the LM26001B employs frequency foldback as a second level of protection. If the feedback voltage falls below the short circuit threshold of 0.9V, operating frequency is reduced, thereby reducing average switch current. This is especially helpful in short circuit conditions, when inductor current can rise very high during the minimum on-time. Frequency reduction begins at 20% below the nominal frequency setting. The minimum operating frequency in foldback mode is 71 kHz typical.

If the FB voltage falls below the frequency foldback threshold during frequency synchronized operation, the SYNC function is disabled. Operating frequency versus FB voltage in short circuit conditions is shown in the Typical Performance Characteristics section.

In conditions where the on time is close to minimum (less than 200nsec typically), such as high input voltage and high switching frequency, the current limit may not function properly. This is because the current limit circuit cannot reduce the on-time below minimum which prevents entry into frequency foldback mode. There are two ways to ensure proper current limit and foldback operation under high input voltage conditions. First, the operating frequency can be reduced to increase the nominal on time. Second, the inductor value can be increased to slow the current ramp and reduce the peak over-current.
FREQUENCY ADJUSTMENT AND SYNCHRONIZATION

The switching frequency of the LM26001B can be adjusted between 150 kHz and 500 kHz using a single external resistor. This resistor is connected from the FREQ pin to ground as shown in the Typical Application Circuit. The resistor value can be calculated with the following empirically derived equation:

$$R_{\text{FREQ}} = (6.25 \times 10^{-10}) \times f_{\text{SW}}^{1.042}$$  \hspace{1cm} (4)

The switching frequency can also be synchronized to an external clock signal using the SYNC pin. The SYNC pin allows the operating frequency to be varied above and below the nominal frequency setting. The adjustment range is from 30% above nominal to 20% below nominal. External synchronization requires a 1.2V (typical) peak signal level at the SYNC pin. The FREQ resistor must always be connected to initialize the nominal operating frequency. The operating frequency is synchronized to the falling edge of the SYNC input. When SYNC goes low, the high-side switch turns on. This allows any duty cycle to be used for the sync signal when synchronizing to a frequency higher than nominal. When synchronizing to a lower frequency, however, there is a minimum duty cycle requirement for the SYNC signal, given in the equation below:

$$\text{Sync}_\text{Dmin} \geq 1 - \frac{f_{\text{sync}}}{f_{\text{nom}}}$$  \hspace{1cm} (5)

Where $f_{\text{nom}}$ is the nominal switching frequency set by the FREQ resistor, and $f_{\text{sync}}$ is a square wave. If the SYNC pin is not used, it must be pulled low for normal operation. A 10kΩ pull-down resistor is recommended to protect against a missing sync signal. Although the LM26001B is designed to operate at up to 500 kHz, maximum load current may be limited at higher frequencies due to increased temperature rise. See the Thermal Considerations section.

VBIAS

The VBIAS pin is used to bypass the internal regulator which provides the bias voltage to the LM26001B. When the VBIAS pin is connected to a voltage greater than 3V, the internal regulator automatically switches over to the VBIAS input. This reduces the current into VIN ($I_q$) and increases system efficiency. Using the VBIAS pin has the added benefit of reducing power dissipation within the device.

For most applications where $3V < \text{Vout} < 10V$, VBIAS can be connected to Vout. If not used, VBIAS should be tied to GND.

If VBIAS drops below 2.9V (typical), the device automatically switches over to supply the internal bias voltage from Vin.

Total device input current is the sum of $I_q$, gate drive current, and VBIAS current, plus some negligible current into the FB pin. Total minimum input supply current can be calculated as shown below:

$$\text{input} = I_q + I_{\text{QG}} + \left( I_{\text{BIAS}} \times D \right)_{\text{eff}}$$

where

- $I_{\text{QG}}$ is the gate drive current, calculated as $I_{\text{QG}} = (4.6 \times 10^{-5}) \times f_{\text{SW}}$  \hspace{1cm} (6)
Total supply input current varies according to load, system efficiency, and operating frequency. To calculate minimum input current during sleep mode, use $I_{\text{q\_Sleep\_VB}}$ and $I_{\text{BIAS\_SLEEP}}$.

For input current in PWM mode, use the same equation, with $I_{\text{q\_PWM\_VB}}$ and $I_{\text{BIAS\_PWM}}$.

If VBIAS is connected to ground, use the same equation with the Ibias term eliminated and either $I_{\text{q\_Sleep\_VDD}}$ or $I_{\text{q\_PWM\_VDD}}$.

**LOW VIN OPERATION AND UVLO**

The LM26001B is designed to remain operational during short line transients when input voltage may drop as low as 3.0V. Minimum nominal operating input voltage is 4.0V. Below this voltage, switch $R_{\text{DS\_ON}}$ increases, due to the lower gate drive voltage from VDD. The minimum voltage required at VDD is approximately 3.5V for normal operation within specification.

VDD can also be used as a pull-up voltage for functions such as PGOOD and FPWM. Note that if VDD is used externally, the pin is not recommended for loads greater than 1 mA.

If the input voltage approaches the nominal output voltage, the duty cycle is maximized to hold up the output voltage. In this mode of operation, once the duty cycle reaches its maximum, the LM26001B can skip a maximum of seven off pulses, effectively increasing the duty cycle and thus minimizing the dropout from input to output. Typical off-pulse skipping waveforms are shown below.

![Off-pulse Skipping Waveforms](image)

**Figure 20. Off-pulse Skipping Waveforms**

$V_{\text{in}} = 3.5V$, $V_{\text{nom}} = 3.3V$, $f_{\text{nom}} = 305kHz$

UVLO is sensed at both VIN and VDD, and is activated when either voltage falls below 2.9V (typical). Although VDD is typically less than 200mV below VIN, it will not discharge through VIN. Therefore when the VIN voltage drops rapidly, VDD may remain high, especially in sleep mode. For fast line voltage transients, using a larger capacitor at the VDD pin can help to hold off a UVLO shutdown by extending the VDD discharge time. By holding up VDD, a larger cap can also reduce the $R_{\text{DS\_ON}}$ (and dropout voltage) in low VIN conditions. Alternately, under heavy loading the VDD voltage can fall several hundred mV below VIN. In this case, UVLO may be triggered by VDD even though the VIN voltage is above the UVLO threshold.

When UVLO is activated the LM26001B enters a standby state in which VDD remains charged. As input voltage and VDD voltage rise above 3.9V (typical) the device will restart from softstart mode.

**PGOOD**

A power good pin, PGOOD, is available to monitor the output voltage status. The pin is internally connected to an open drain MOSFET, which remains open while the output voltage is within operating range. PGOOD goes low (low impedance to ground) when the output falls below 85% of nominal or EN is pulled low. When the output voltage returns to within 92% of nominal, as measured at the FB pin, PGOOD returns to a high state. For improved noise immunity, there is a 5us delay between the PGOOD threshold and the PGOOD pin going low.
EXAMPLE CIRCUIT

Figure 21 shows a complete typical application schematic. The components have been selected based on the design criteria given in the following sections.

Figure 21. Example Circuit
1.5A Max, 305 kHz

SETTING OUTPUT VOLTAGE

The output voltage is set by the ratio of a voltage divider at the FB pin as shown in the Typical Application Circuit. The resistor values can be determined by the following equation:

\[ R_2 = \frac{R_1}{\left(\frac{V_{out}}{V_{fb}} - 1\right)} \]

where

- \( V_{fb} = 1.234V \) typically

A maximum value of 150kΩ is recommended for the sum of \( R_1 \) and \( R_2 \).

As input voltage decreases towards the nominal output voltage, the LM26001B can skip up to seven off-pulses as described in the Low Vin Operation section. In low output voltage applications, if the on-time reaches \( T_{on_{\text{MIN}}} \), the device will skip on-pulses to maintain regulation. There is no limit to the number of pulses that are skipped. In this mode of operation, however, output ripple voltage may increase slightly.

INDUCTOR

The output inductor should be selected based on inductor ripple current. The amount of inductor ripple current compared to load current, or ripple content, is defined as \( I_{\text{ripple}}/I_{\text{load}} \). Ripple content should be less than 40%.

Inductor ripple current, \( I_{\text{ripple}} \), can be calculated as shown below:

\[ I_{\text{ripple}} = \frac{(V_{in} - V_{out}) \times V_{out}}{f_{sw} \times L \times V_{in}} \]

Larger ripple content increases losses in the inductor and reduces the effective current limit.

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current limit threshold.

Remember that inductor value also affects the sleep mode threshold as shown in Figure 17.
When choosing the inductor, the saturation current rating must be higher than the maximum peak inductor current and the RMS current rating should be higher than the maximum load current. Peak inductor current, $I_{\text{peak}}$, is calculated as:

$$I_{\text{peak}} = I_{\text{load}} + \frac{I_{\text{ripple}}}{2} \quad (9)$$

For example, at a maximum load of 1.5A and a ripple content of 33%, peak inductor current is equal to 1.75A which is safely below the minimum current limit of 1.80A. By increasing the inductor size, ripple content and peak inductor current are lowered, which increases the current limit margin.

The size of the output inductor can also be determined using the desired output ripple voltage, $V_{\text{rip}}$. The equation to determine the minimum inductance value based on $V_{\text{rip}}$ is as follows:

$$L_{\text{MIN}} = \frac{(V_{\text{in}} - V_{\text{out}}) \times V_{\text{out}} \times R_{\text{e}}}{V_{\text{in}} \times f_{\text{sw}} \times V_{\text{rip}}}$$

where
- $R_{\text{e}}$ is the ESR of the output capacitors
- $V_{\text{rip}}$ is a peak-to-peak value \( \quad (10) \)

This equation assumes that the output capacitors have some amount of ESR. It does not apply to ceramic output capacitors.

If this method is used, ripple content should still be verified to be less than 40%.

**OUTPUT CAPACITOR**

The primary criterion for selecting an output capacitor is equivalent series resistance, or ESR.

ESR ($R_{\text{e}}$) can be selected based on the requirements for output ripple voltage and transient response. Once an inductor value has been selected, ripple voltage can be calculated for a given $R_{\text{e}}$ using the equation above for $L_{\text{MIN}}$. Lower ESR values result in lower output ripple.

$R_{\text{e}}$ can also be calculated from the following equation:

$$R_{\text{e,MAX}} = \frac{\Delta V_{t}}{\Delta I_{t}}$$

where
- $\Delta V_{t}$ is the allowed voltage excursion during a load transient
- $\Delta I_{t}$ is the maximum expected load transient \( \quad (11) \)

If the total ESR is too high, the load transient requirement cannot be met, no matter how large the output capacitance.

If the ESR criteria for ripple voltage and transient excursion cannot be met, more capacitors should be used in parallel.

For non-ceramic capacitors, the minimum output capacitance is of secondary importance, and is determined only by the load transient requirement.

If there is not enough capacitance, the output voltage excursion will exceed the maximum allowed value even if the maximum ESR requirement is met. The minimum capacitance is calculated as follows:

$$C_{\text{MIN}} = \frac{L \times (\Delta V_{t} - \sqrt{(\Delta V_{t})^2 - (\Delta I_{t} \times R_{e})^2})}{V_{\text{out}} \times R_{e}^2} \quad (12)$$

It is assumed the total ESR, $R_{\text{e}}$, is no greater than $R_{\text{e,MAX}}$. Also, it is assumed that $L$ has already been selected. Generally speaking, the output capacitance requirement decreases with $R_{\text{e}}$, $\Delta I_{t}$, and $L$. A typical value greater than 100 µF works well for most applications.
INPUT CAPACITOR

In a switching converter, very fast switching pulse currents are drawn from the input rail. Therefore, input capacitors are required to reduce noise, EMI, and ripple at the input to the LM26001B. Capacitors must be selected that can handle both the maximum ripple RMS current at highest ambient temperature as well as the maximum input voltage. The equation for calculating the RMS input ripple current is shown below:

$$I_{\text{rms}} = \frac{I_{\text{load}} \times \sqrt{V_{\text{out}} \times (V_{\text{in}} - V_{\text{out}})}}{V_{\text{in}}}$$  \hspace{1cm} (13)

For noise suppression, a ceramic capacitor in the range of 1.0 µF to 10 µF should be placed as close as possible to the VIN pin.

A larger, high ESR input capacitor should also be used. This capacitor is recommended for damping input voltage spikes during power on and for holding up the input voltage during transients. In low input voltage applications, line transients may fall below the UVLO threshold if there is not enough input capacitance. Both tantalum and electrolytic type capacitors are suitable for the bulk capacitor. However, large tantalums may not be available for high input voltages and their working voltage must be derated by at least 2X.

BOOTSTRAP

The drive voltage for the internal switch is supplied via the BOOT pin. This pin must be connected to a ceramic capacitor, Cboot, from the switch node, shown as C4 in the typical application. The LM26001B provides the VDD voltage internally, so no external diode is needed. A minimum value of 0.1 µF is recommended for Cboot. Smaller values may result in insufficient hold up time for the drive voltage and increased power dissipation.

During low Vin operation, when the on-time is extended, the bootstrap capacitor is at risk of discharging. If the Cboot capacitor is discharged below approximately 2.5V, the LM26001B enters a high frequency re-charge mode. The Cboot cap is re-charged via the LG synchronous FET shown in the Block Diagram. Switching returns to normal when the Cboot cap has been recharged.

CATCH DIODE

When the internal switch is off, output current flows through the catch diode. Alternately, when the switch is on, the diode sees a reverse voltage equal to Vin. Therefore, the important parameters for selecting the catch diode are peak current and peak inverse voltage. The average current through the diode is given by:

$$I_{\text{AVE}} = I_{\text{load}} \times (1-D)$$  \hspace{1cm} (14)

Where D is the duty cycle, defined as Vout/Vin. The catch diode conducts the largest currents during the lowest duty cycle. Therefore ID_{AVE} should be calculated assuming maximum input voltage. The diode should be rated to handle this current continuously. For over-current or short circuit conditions, the catch diode should be rated to handle peak currents equal to the peak current limit.

The peak inverse voltage rating of the diode must be greater than maximum input voltage.

A Schottky diode must be used. It's low forward voltage maximizes efficiency and BOOT voltage, while also protecting the SW pin against large negative voltage spikes.

COMPENSATION

The purpose of loop compensation is to ensure stable operation while maximizing dynamic performance. Stability can be analyzed with loop gain measurements, while dynamic performance is analyzed with both loop gain and load transient response. Loop gain is equal to the product of control-output transfer function (power stage) and the feedback transfer function (the compensation network).

For stability purposes, our target is to have a loop gain slope that is -20dB /decade from a very low frequency to beyond the crossover frequency. Also, the crossover frequency should not exceed one-fifth of the switching frequency, i.e. 60 kHz in the case of 300 kHz switching frequency.

For dynamic purposes, the higher the bandwidth, the faster the load transient response. A large DC gain means high DC regulation accuracy (i.e. DC voltage changes little with load or line variations). To achieve this loop gain, the compensation components should be set according to the shape of the control-output bode plot. A typical plot is shown in Figure 22 below.
The control-output transfer function consists of one pole (fp), one zero (fz), and a double pole at fn (half the switching frequency).

Referring to Figure 22, the following should be done to create a -20dB /decade roll-off of the loop gain:

1. Place a pole at 0Hz (fpc)
2. Place a zero at fp (fzc)
3. Place a second pole at fz (fpc1)

The resulting feedback (compensation) bode plot is shown below in Figure 23. Adding the control-output response to the feedback response will then result in a nearly continuous -20db/decade slope.

The control-output corner frequencies can be determined approximately by the following equations:

\[
\begin{align*}
fz &= \frac{1}{2\pi \times Re \times Co} \\
fp &= \frac{1}{10 \times \pi \times Ro \times Co} + \frac{0.5}{2 \times \pi \times L \times fsw \times Co} \\
fn &= \frac{fsw}{2}
\end{align*}
\]

where

- Co is the output capacitance
- Ro is the load resistance
- Re is the output capacitor ESR
- fsw is the switching frequency

Figure 22. Control-Output Transfer Function

Figure 23. Feedback Transfer Function
The effects of slope compensation and current sense gain are included in this equation. However, the equation is an approximation intended to simplify loop compensation calculations. To derive the exact transfer function, use 0.2V/V sense amp gain and 36mVp-p slope compensation.

Since \( f_p \) is determined by the output network, it shifts with loading. Determine the range of frequencies (\( f_{p_{\text{min}}/\text{max}} \)) across the expected load range. Then determine the compensation values as described below and shown in Figure 24.

![Figure 24. Compensation Network](image)

1. The compensation network automatically introduces a low frequency pole (\( f_{p_{\text{c}}} \)), which is close to 0Hz.

2. Once the \( f_p \) range is determined, \( R_5 \) should be calculated using:

\[
R_5 = \frac{B}{g_m} \times \left( \frac{R_1 + R_2}{R_2} \right)
\]

where

- \( B \) is the desired feedback gain in V/V between \( f_p \) and \( f_z \)
- \( g_m \) is the transconductance of the error amplifier

A gain value around 10dB (3.3V/v) is generally a good starting point. Bandwidth increases with increasing values of \( R_5 \).

3. Next, place a zero (\( f_{z_{\text{c}}} \)) near \( f_p \) using \( C_8 \). \( C_8 \) can be determined with the following equation:

\[
C_8 = \frac{1}{2 \times \pi \times f_{P_{\text{MAX}}} \times R_5}
\]

The selected value of \( C_8 \) should place \( f_{z_{\text{c}}} \) within a decade above or below \( f_{p_{\text{MAX}}} \), and not less than \( f_{p_{\text{MIN}}} \). A higher \( C_8 \) value (closer to \( f_{p_{\text{MIN}}} \)) generally provides a more stable loop, but too high a value will slow the transient response time. Conversely, a smaller \( C_8 \) value will result in a faster transient response, but lower phase margin.

4. A second pole (\( f_{p_{c1}} \)) can also be placed at \( f_z \). This pole can be created with a single capacitor, \( C_9 \). The minimum value for this capacitor can be calculated by:

\[
C_9 = \frac{1}{2 \times \pi \times f_z \times R_5}
\]

\( C_9 \) may not be necessary in all applications. However, if the operating frequency is being synchronized below the nominal frequency, \( C_9 \) is recommended. Although it is not required for stability, \( C_9 \) is very helpful in suppressing noise.

A phase lead capacitor can also be added to increase the phase and gain margins. The phase lead capacitor is most helpful for high input voltage applications or when synchronizing to a frequency greater than nominal. This capacitor, shown as \( C_{10} \) in Figure 24, should be placed in parallel with the top feedback resistor, \( R_1 \). \( C_{10} \) introduces an additional zero and pole to the compensation network. These frequencies can be calculated as shown below:

\[
f_{z_{\text{ff}}} = \frac{1}{2 \times \pi \times R_1 \times C_{10}}
\]
A phase lead capacitor will boost loop phase around the region of the zero frequency, \( f_{zff} \). \( f_{zff} \) should be placed somewhat below the \( f_{pz1} \) frequency set by C9. However, if C10 is too large, it will have no effect.

**PCB Layout**

Good board layout is critical for switching regulators such as the LM26001B. First, the ground plane area must be sufficient for thermal dissipation purposes, and second, appropriate guidelines must be followed to reduce the effects of switching noise.

Switch mode converters are very fast switching devices. In such devices, the rapid increase of input current combined with parasitic trace inductance generates unwanted \( \frac{L}{dI/dt} \) noise spikes at the SW node and also at the VIN node. The magnitude of this noise tends to increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI), and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise.

The current sensing circuit in current mode devices can be easily affected by switching noise. This noise can cause duty cycle jitter which leads to increased spectral noise. Although the LM26001B has 100ns blanking time at the beginning of every cycle to ignore this noise, some noise may remain after the blanking time. Following the important guidelines below will help minimize switching noise and its effect on current sensing.

The switch node area should be as small as possible. The catch diode, input capacitors, and output capacitors should be grounded to a large ground plane, with the bulk input capacitor grounded as close as possible to the catch diode anode. Additionally, the ground area between the catch diode and bulk input capacitor is very noisy and should be somewhat isolated from the rest of the ground plane.

A ceramic input capacitor must be connected as close as possible to the VIN pin and grounded close to the GND pin. Often this capacitor is most easily located on the bottom side of the pcb. If placement close to the GND pin is not practical, the ceramic input capacitor can also be grounded close to the catch diode ground. The above layout recommendations are illustrated below in **Figure 25**.

![Figure 25. Example PCB Layout](image)

It is a good practice to connect the EP, GND pin, and small signal components (COMP, FB, FREQ) to a separate ground plane, shown in **Figure 25** as EP GND, and in the schematics as a signal ground symbol. Both the exposed pad and the GND pin must be connected to ground. This quieter plane should be connected to the high current ground plane at a quiet location, preferably near the Vout ground as shown by the dashed line in **Figure 25**.

The EP GND plane should be made as large as possible, since it is also used for thermal dissipation. Several vias can be placed directly below the EP to increase heat flow to other layers when they are available. The recommended via hole diameter is 0.3mm.

The trace from the FB pin to the resistor divider should be short and the entire feedback trace must be kept away from the inductor and switch node. See Application Note **AN-1229** for more information regarding PCB layout for switching regulators.
Thermal Considerations and TSD

Although the LM26001B has a built-in current limit, at ambient temperatures above 80°C, device temperature rise may limit the actual maximum load current. Therefore, temperature rise must be taken into consideration to determine the maximum allowable load current.

Temperature rise is a function of the power dissipation within the device. The following equations can be used to calculate power dissipation (PD) and temperature rise, where total PD is the sum of FET switching losses, FET DC losses, drive losses, Iq, and VBIAS losses:

\[ PD_{TOTAL} = P_{swAC} + P_{swDC} + P_{QG} + P_{Iq} + P_{VBIAS} \]  

\[ P_{swAC} = Vin \times I_{load} \times f_{sw} \times \left( \frac{Vin \times 10^{-9}}{1.33} \right) \]  

\[ P_{swDC} = D \times I_{load}^2 \times (0.2 + 0.00065 \times (T_j - 25)) \]  

\[ P_{QG} = Vin \times 4.6 \times 10^{-9} \times f_{sw} \]  

\[ P_{Iq} = Vin \times Iq \]  

\[ P_{VBIAS} = Vbias \times I_{VBIAS} \]

Given this total power dissipation, junction temperature can be calculated as follows:

\[ T_j = T_a + (PD_{TOTAL} \times \theta_{JA}) \]

where

- \( \theta_{JA} = 38°C/W \) (typically) when using a multi-layer board with a large copper plane area

\( \theta_{JA} \) varies with board type and metallization area.

To calculate the maximum allowable power dissipation, assume \( T_j = 125°C \). To ensure that junction temperature does not exceed the maximum operating rating of 125°C, power dissipation should be verified at the maximum expected operating frequency, maximum ambient temperature, and minimum and maximum input voltage. The calculated maximum load current is based on continuous operation and may be exceeded during transient conditions.

If the power dissipation remains above the maximum allowable level, device temperature will continue to rise. When the junction temperature exceeds its maximum, the LM26001B engages Thermal Shut Down (TSD). In TSD, the part remains in a shutdown state until the junction temperature falls to within normal operating limits. At this point, the device restarts in soft-start mode.
## REVISION HISTORY

<table>
<thead>
<tr>
<th>Changes from Revision A (April 2013) to Revision B</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed layout of National Data Sheet to TI format</td>
<td>21</td>
</tr>
</tbody>
</table>

Copyright © 2007–2013, Texas Instruments Incorporated

Product Folder Links: **LM26001B**
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Top-Side Markings (4)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM26001BMH/NOPB</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>16</td>
<td>92</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>L26001 BMH</td>
<td></td>
</tr>
<tr>
<td>LM26001BMHX/NOPB</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>16</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>L26001 BMH</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD:** The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS):** TI’s terms “Lead-Free” or “Pb-Free” mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) **MSL, Peak Temp.** – The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

![Diagram of reel dimensions](image)

### TAPE DIMENSIONS

![Diagram of tape dimensions](image)

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>Dimension designed to accommodate the component width</td>
</tr>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

![Diagram of quadrant assignments](image)

*All dimensions are nominal.

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM26001BMHX/NOPB</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>16</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.95</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM26001BMHX/NOPB</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>16</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
5. Features may not be present.

PowerPAD is a trademark of Texas Instruments.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/sma002) and SLMA004 (www.ti.com/lit/sma004).
9. Size of metal pad may vary due to creepage requirement.
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.
Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI’s published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and/or implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, “Designers”) understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers’ applications and compliance of their applications (and of all TI products used in or for Designers’ applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI’s provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, “TI Resources”) are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer’s company) agrees to use any particular TI Resource solely for the purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designers are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY TECHNOLOGICAL, PATENT, COPYRIGHT, MASK WORK, SEMICONDUCTOR PATENT, TRADE SECRETS, OR ANY OTHER PROPERTY RIGHTS OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL Faults. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NONINFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designers may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designers fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.