LM2660 Switched Capacitor Voltage Converter

1 Features
• Inverts or Doubles Input Supply Voltage
• Narrow SOIC and VSSOP Packages
• 6.5-Ω Typical Output Resistance
• 88% Typical Conversion Efficiency at 100 mA
• Selectable Oscillator Frequency: 10 kHz/80 kHz
• Optional External Oscillator Input

2 Applications
• Laptop Computers
• Cellular Phones
• Medical Instruments
• Operational Amplifier Power Supplies
• Interface Power Supplies
• Handheld Instruments

3 Description
The LM2660 CMOS charge-pump voltage converter is a versatile unregulated switched capacitor inverter or doubler. Operating from a wide 1.5-V to 5.5-V supply voltage, the LM2660 uses two low-cost capacitors to provide 100 mA of output current without the cost, size and EMI related to inductor-based converters. With an operating current of only 120 µA and operating efficiency greater than 90% at most loads, the LM2660 provides ideal performance for battery-powered systems. LM2660 devices can be operated directly in parallel to lower output impedance, thus providing more current at a given voltage.

The FC (frequency control) pin selects between a nominal 10-kHz or 80-kHz oscillator frequency. The oscillator frequency can be lowered by adding an external capacitor to the OSC pin. Also, the OSC pin may be used to drive the LM2660 with an external clock up to 150 kHz. Through these methods, output ripple frequency and harmonics may be controlled.

Additionally, the LM2660 may be configured to divide a positive input voltage precisely in half. In this mode, input voltages as high as 11 V may be used.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2660</td>
<td>SOIC (8)</td>
<td>4.90 mm x 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>VSSOP (8)</td>
<td>3.00 mm x 3.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

![Simplified Schematic Diagram]
# Table of Contents

1 Features ......................................................... 1  
2 Applications .................................................. 1  
3 Description ................................................... 1  
4 Revision History .............................................. 2  
5 Pin Configuration and Functions ....................... 3  
6 Specifications ................................................. 4  
   6.1 Absolute Maximum Ratings ......................... 4  
   6.2 Handling Ratings ....................................... 4  
   6.3 Recommended Operating Conditions .............. 4  
   6.4 Thermal Information ................................... 4  
   6.5 Electrical Characteristics ......................... 5  
   6.6 Typical Characteristics ............................. 6  
7 Parameter Measurement Information .................. 8  
   7.1 Test Circuits ............................................. 8  
8 Detailed Description ....................................... 9  
   8.1 Overview ............................................... 9  
   8.2 Functional Block Diagram ......................... 9  
   8.3 Feature Description ................................. 9  
   8.4 Device Functional Modes ......................... 10  
9 Application and Implementation ....................... 11  
   9.1 Application Information ......................... 11  
   9.2 Typical Applications ............................. 11  
10 Power Supply Recommendations ....................... 16  
11 Layout ..................................................... 17  
   11.1 Layout Guidelines .................................. 17  
   11.2 Layout Example .................................... 17  
12 Device and Documentation Support ................. 18  
   12.1 Device Support ..................................... 18  
   12.2 Trademarks ......................................... 18  
   12.3 Electrostatic Discharge Caution ............... 18  
   12.4 Glossary ............................................. 18  
13 Mechanical, Packaging, and Orderable Information 19  

# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## Changes from Revision D (May 2013) to Revision E

<table>
<thead>
<tr>
<th>Changes</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Added Device Information and Handling Rating tables, Feature Description, Device Functional Modes, Application and Implementation, Power Supply Recommendations, Layout, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information sections; moved some curves to Application Curves section</td>
<td></td>
</tr>
</tbody>
</table>

## Changes from Revision C (May 2013) to Revision D

<table>
<thead>
<tr>
<th>Changes</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed layout of National Data Sheet to TI format</td>
<td>15</td>
</tr>
</tbody>
</table>
## 5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN NUMBER</th>
<th>NAME</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FC</td>
<td>Input</td>
<td>Frequency control for internal oscillator:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>FC = open, f&lt;sub&gt;OSC&lt;/sub&gt; = 10 kHz (typ); Same as inverter.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>FC = V+, f&lt;sub&gt;OSC&lt;/sub&gt; = 80 kHz (typ);</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>FC has no effect when OSC pin is driven externally.</td>
</tr>
<tr>
<td>2</td>
<td>CAP+</td>
<td>Power</td>
<td>Connect this pin to the positive terminal of charge-pump capacitor.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground</td>
<td>Power supply ground input.</td>
</tr>
<tr>
<td>4</td>
<td>CAP−</td>
<td>Power</td>
<td>Connect this pin to the negative terminal of charge-pump capacitor.</td>
</tr>
<tr>
<td>5</td>
<td>OUT</td>
<td>Power</td>
<td>Negative voltage output.</td>
</tr>
<tr>
<td>6</td>
<td>LV</td>
<td>Input</td>
<td>Low-voltage operation input. Tie LV to GND when input voltage is less than 3.5 V. Above 3.5 V, LV can be connected to GND or left open. When driving OSC with an external clock, LV must be connected to GND. LV must be tied to OUT.</td>
</tr>
<tr>
<td>7</td>
<td>OSC</td>
<td>Input</td>
<td>Oscillator control input. OSC is connected to an internal 15-pF capacitor. An external capacitor can be connected to slow the oscillator. Also, an external clock can be used to drive OSC. Same as inverter except that OSC cannot be driven by an external clock.</td>
</tr>
<tr>
<td>8</td>
<td>V+</td>
<td>Power</td>
<td>Power supply positive voltage input. Positive voltage output.</td>
</tr>
</tbody>
</table>

![SOIC (D) and VSSOP (DGK) 8 Pin Top View](image)
6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V+ to GND, or GND to OUT)</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>LV</td>
<td>(OUT − 0.3 V) to (GND + 3 V)</td>
<td>V</td>
</tr>
<tr>
<td>FC, OSC</td>
<td>The least negative of (OUT − 0.3 V) or (V+ − 6 V) to (V+ + 0.3 V)</td>
<td>V</td>
</tr>
<tr>
<td>V+ and OUT continuous output current</td>
<td>120</td>
<td>mA</td>
</tr>
<tr>
<td>Output short-circuit duration to GND (^{(2)})</td>
<td>1</td>
<td>second</td>
</tr>
<tr>
<td>Power dissipation SOIC (D)(^{(3)})</td>
<td>735</td>
<td>mW</td>
</tr>
<tr>
<td>Power dissipation VSSOP (DGK)(^{(3)})</td>
<td>500</td>
<td>mW</td>
</tr>
<tr>
<td>Lead temperature (soldering, 10 seconds)</td>
<td>300</td>
<td>°C</td>
</tr>
<tr>
<td>Operating junction temperature</td>
<td>−40</td>
<td>85</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) OUT may be shorted to GND for one second without damage. However, shorting OUT to V+ may damage the device and should be avoided. Also, for temperatures above 85°C, OUT must not be shorted to GND or V+, or device may be damaged.

(3) The maximum allowable power dissipation is calculated by using \( P_{\text{DMAX}} = (T_{\text{JMAX}} − T_A)/R_{\theta \text{JA}} \), where \( T_{\text{JMAX}} \) is the maximum junction temperature, \( T_A \) is the ambient temperature, and \( R_{\theta \text{JA}} \) is the junction-to-ambient thermal resistance of the specified package.

6.2 Handling Ratings

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( T_{\text{stg}} )</td>
<td>Storage temperature range</td>
<td>−65</td>
</tr>
<tr>
<td>( V_{\text{ESD}} )</td>
<td>Electrostatic discharge</td>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(^{(1)})</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+ (supply voltage)</td>
<td>Inverter, LV = Open</td>
<td>3.5</td>
<td>5.5</td>
</tr>
<tr>
<td></td>
<td>Inverter, LV = GND</td>
<td>1.5</td>
<td>5.5</td>
</tr>
<tr>
<td></td>
<td>Doubler, LV = OUT</td>
<td>2.5</td>
<td>5.5</td>
</tr>
<tr>
<td>Junction temperature (( T_J ))</td>
<td>−40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>LM2660</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{\theta \text{JA}} )</td>
<td>Junction-to-ambient thermal resistance</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
6.5 Electrical Characteristics

Limits in for typical (TYP) values are for $T_J = 25^\circ C$, and limits in for minimum (MIN) and maximum (MAX) values apply over the full operating temperature range; $V_+ = 5V$, FC = Open, $C_1 = C_2 = 150 \mu F$, unless otherwise specified in the Test Conditions. (1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_+$ Supply voltage</td>
<td>$R_L = 1k$</td>
<td>3.5</td>
<td>5.5</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Inverter, $LV = Open$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Inverter, $LV = GND$</td>
<td>1.5</td>
<td>5.5</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Doubler, $LV = OUT$</td>
<td>2.5</td>
<td>5.5</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$I_Q$ Supply current</td>
<td>No Load</td>
<td>0.12</td>
<td>0.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$LV = Open$</td>
<td>1</td>
<td>3</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_L$ Output current</td>
<td>$T_A \leq 85^\circ C$, $OUT \leq -4 , V$</td>
<td>100</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_A &gt; 85^\circ C$, $OUT \leq -3.8 , V$</td>
<td>100</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$R_{OUT}$ Output resistance$^{(2)}$</td>
<td>$I_L = 100 , mA$</td>
<td>$T_A \leq 85^\circ C$</td>
<td>6.5</td>
<td>10</td>
<td>$\Omega$</td>
</tr>
<tr>
<td></td>
<td>$T_A &gt; 85^\circ C$</td>
<td>12</td>
<td></td>
<td>$\Omega$</td>
<td></td>
</tr>
<tr>
<td>$f_{OSC}$ Oscillator frequency</td>
<td>OSC = Open</td>
<td>FC = Open</td>
<td>5</td>
<td>10</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>FC = $V_+$</td>
<td>40</td>
<td>80</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>$f_{SW}$ Switching frequency$^{(3)}$</td>
<td>OSC = Open</td>
<td>FC = Open</td>
<td>2.5</td>
<td>5</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>FC = $V_+$</td>
<td>20</td>
<td>40</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>$I_{OSC}$ OSC input current</td>
<td>FC = Open</td>
<td>±2</td>
<td>$\mu A$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>FC = $V_+$</td>
<td>±16</td>
<td></td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$P_{EFF}$ Power efficiency</td>
<td>$R_L (1k)$ between $V_+$ and $OUT$</td>
<td>96%</td>
<td>98%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_L (500)$ between GND and OUT</td>
<td>92%</td>
<td>96%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_L = 100 , mA$ to GND</td>
<td>88%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DEFF}$ Voltage conversion efficiency</td>
<td>No Load</td>
<td>99%</td>
<td>99.96%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) In the test circuit, capacitors $C_1$ and $C_2$ are 0.2-Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.

(2) Specified output resistance includes internal switch resistance and capacitor ESR.

(3) The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2f_{SW}$. 
### 6.6 Typical Characteristics

(Circuit of Figure 12)

- **Figure 1. Supply Current vs Supply Voltage**
- **Figure 2. Supply Current vs Oscillator Frequency**
- **Figure 3. Output Source Resistance vs Supply Voltage**
- **Figure 4. Output Source Resistance vs Temperature**
- **Figure 5. Output Voltage Drop vs Load Current**
- **Figure 6. Output Voltage vs Oscillator Frequency**
Typical Characteristics (continued)

(Circuit of Figure 12)

**Figure 7. Oscillator Frequency vs External Capacitance**

**Figure 8. Oscillator Frequency vs Supply Voltage**

\((F_c = V^+)\)

**Figure 9. Oscillator Frequency vs Supply Voltage**

\((F_c = \text{Open})\)

**Figure 10. Oscillator Frequency vs Temperature**

\((F_c = V^+)\)

**Figure 11. Oscillator Frequency vs Temperature**

\((F_c = \text{Open})\)
7 Parameter Measurement Information

7.1 Test Circuits

Figure 12. LM2660 Test Circuit
8 Detailed Description

8.1 Overview
The LM2660 contains four large CMOS switches which are switched in a sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 13 illustrates the voltage conversion scheme. When \( S_1 \) and \( S_3 \) are closed, \( C_1 \) charges to the supply voltage \( V+ \). During this time interval switches \( S_2 \) and \( S_4 \) are open. In the second time interval, \( S_1 \) and \( S_3 \) are open and \( S_2 \) and \( S_4 \) are closed, \( C_1 \) is charging \( C_2 \). After a number of cycles, the voltage across \( C_2 \) will be pumped to \( V+ \). Since the anode of \( C_2 \) is connected to ground, the output at the cathode of \( C_2 \) equals \(- (V+)\) assuming no load on \( C_2 \), no loss in the switches, and no ESR in the capacitors. In reality, the charge transfer efficiency depends on the switching frequency, the on-resistance of the switches, and the ESR of the capacitors.

![Figure 13. Voltage Inverting Principle](image)

8.2 Functional Block Diagram

8.3 Feature Description
8.3.1 Changing Oscillator Frequency
The internal oscillator frequency can be selected using the Frequency Control (FC) pin. When FC is open, the oscillator frequency is 10 kHz; when FC is connected to \( V+ \), the frequency increases to 80 kHz. A higher oscillator frequency allows smaller capacitors to be used for equivalent output resistance and ripple, but increases the typical supply current from 0.12 mA to 1 mA.

The oscillator frequency can be lowered by adding an external capacitor between OSC and GND. (See Typical Characteristics.) Also, in the inverter mode, an external clock that swings within 100 mV of \( V+ \) and GND can be used to drive OSC. Any CMOS logic gate is suitable for driving OSC. LV must be grounded when driving OSC. The maximum external clock frequency is limited to 150 kHz.

The switching frequency of the converter (also called the charge pump frequency) is half of the oscillator frequency.

---

**NOTE**

OSC cannot be driven by an external clock in the voltage-doubling mode.
Table 1. LM2660 Oscillator Frequency Selection

<table>
<thead>
<tr>
<th>FC</th>
<th>OSC</th>
<th>OSCILLATOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open</td>
<td>Open</td>
<td>10 kHz</td>
</tr>
<tr>
<td>V+</td>
<td>Open</td>
<td>80 kHz</td>
</tr>
<tr>
<td>Open or V+</td>
<td>External Capacitor</td>
<td>See Typical Characteristics</td>
</tr>
<tr>
<td>N/A</td>
<td>External Clock</td>
<td>External Clock</td>
</tr>
<tr>
<td></td>
<td>(inverter mode only)</td>
<td>Frequency</td>
</tr>
</tbody>
</table>

8.4 Device Functional Modes

When $V_+$ is applied to the LM2660, the device becomes enabled and will operate in which ever configuration the device is placed (inverter, doubler, etc.).
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM2660 CMOS charge-pump voltage converter is a versatile unregulated switched capacitor inverter or doubler. Operating from a wide 1.5 V to 5.5 V supply voltage, the LM2660 uses two low-cost capacitors to provide 100 mA of output current without the cost, size and EMI related to inductor-based converters. With an operating current of only 120 µA and operating efficiency greater than 90% at most loads, the LM2660 provides ideal performance for battery-powered systems. LM2660 devices can be operated directly in parallel to lower output impedance, thus providing more current at a given voltage.

9.2 Typical Applications

9.2.1 Voltage Inverter

9.2.1.1 Design Requirements

The main application of LM2660 is to generate a negative supply voltage. The voltage inverter circuit uses only two external capacitors as shown in Figure 14. The range of the input supply voltage is 1.5 V to 5.5 V. For a supply voltage less than 3.5V, the LV pin must be connected to ground to bypass the internal regulator circuitry. This gives the best performance in low voltage applications. If the supply voltage is greater than 3.5 V, LV may be connected to ground or left open. The choice of leaving LV open simplifies the direct substitution of the LM2660 for the LMC7660 Switched Capacitor Voltage Converter.

9.2.1.2 Detailed Design Procedure

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistor. The voltage source equals \(-V_+\). The output resistance \(R_{out}\) is a function of the ON resistance of the internal MOS switches, the oscillator frequency, and the capacitance and ESR of \(C_1\) and \(C_2\). A good approximation is:

\[
R_{out} \approx 2R_{SW} + \frac{2}{f_{osc} x C_1} + 4 \times ESR_{C1} + ESR_{C2}
\]

where

- \(R_{SW}\) is the sum of the ON resistance of the internal MOS switches shown in Figure 13.

High value, low ESR capacitors will reduce the output resistance. Instead of increasing the capacitance, the oscillator frequency can be increased to reduce the \(2/(f_{osc} x C_1)\) term. Once this term is trivial compared with \(R_{SW}\) and ESRs, further increasing in oscillator frequency and capacitance will become ineffective.

The peak-to-peak output voltage ripple is determined by the oscillator frequency, and the capacitance and ESR of the output capacitor \(C_2\):

\[
V_{ripple} = \frac{i_L}{r_{osc} x C_2} + 2 \times i_L \times ESR_{C2}
\]

Again, using a low ESR capacitor will result in lower ripple.
Typical Applications (continued)

9.2.1.2.1 Capacitor Selection

The output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

\[
\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{I_L^2 R_L}{I_L^2 R_L + I_L^2 R_{\text{out}} + I_Q(V+)}
\]

where

- \( I_Q(V+) \) is the quiescent power loss of the IC device, and
- \( I_L^2 R_{\text{out}} \) is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

Since the switching current charging and discharging \( C_1 \) is approximately twice as the output current, the effect of the ESR of the pumping capacitor \( C_1 \) is multiplied by four in the output resistance. The output capacitor \( C_2 \) is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. However, the ESR of \( C_2 \) directly affects the output voltage ripple. Therefore, low ESR capacitors (Table 2) are recommended for both capacitors to maximize efficiency, reduce the output voltage drop and voltage ripple. For convenience, \( C_1 \) and \( C_2 \) are usually chosen to be the same.

The output resistance varies with the oscillator frequency and the capacitors. In Figure 15, the output resistance vs. oscillator frequency curves are drawn for three different tantalum capacitors. At very low frequency range, capacitance plays the most important role in determining the output resistance. Once the frequency is increased to some point (such as 20 kHz for the 150 \( \mu F \) capacitors), the output resistance is dominated by the ON resistance of the internal switches and the ESRs of the external capacitors. A low value, smaller size capacitor usually has a higher ESR compared with a bigger size capacitor of the same type. For lower ESR, use ceramic capacitors.

![Figure 15. Output Source Resistance vs Oscillator Frequency](image)

**Table 2. Low ESR Capacitor Manufacturers**

<table>
<thead>
<tr>
<th>MANUFACTURER</th>
<th>CAPACITOR TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nichicon Corp.</td>
<td>PL, PF series, through-hole aluminum electrolytic</td>
</tr>
<tr>
<td>AVX Corp.</td>
<td>TPS series, surface-mount tantalum</td>
</tr>
<tr>
<td>Sprague</td>
<td>593D, 594D, 595D series, surface-mount tantalum</td>
</tr>
<tr>
<td>Sanyo</td>
<td>OS-CON series, through-hole aluminum electrolytic</td>
</tr>
</tbody>
</table>
9.2.1.2.2 Paralleling Devices

Any number of LM2660s can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor $C_1$, while only one output capacitor $C_{out}$ is needed as shown in Figure 16. The composite output resistance is:

$$R_{out} = \frac{R_{out \text{ of each LM2660}}}{\text{Number of Devices}}$$  \hspace{1cm} (4)

![Figure 16. Lowering Output Resistance By Paralleling Devices](image)

9.2.1.2.3 Cascading Devices

Cascading the LM2660s is an easy way to produce a greater negative voltage (as shown in Figure 17). If $n$ is the integer representing the number of devices cascaded, the unloaded output voltage $V_{out}$ is $(-nV_{in})$. The effective output resistance is equal to the weighted sum of each individual device:

$$R_{out} = nR_{out\_1} + \frac{n}{2}R_{out\_2} + \cdots + R_{out\_n}$$  \hspace{1cm} (5)

A three-stage cascade circuit shown in Figure 18 generates $-3V_{in}$ from $V_{in}$.

Cascading is also possible when devices are operating in doubling mode. In Figure 19, two devices are cascaded to generate $3V_{in}$.

An example of using the circuit in Figure 18 or Figure 19 is generating $+15V$ or $-15V$ from a $+5V$ input.

Note that, the number of $n$ is practically limited since the increasing of $n$ significantly reduces the efficiency and increases the output resistance and output voltage ripple.

![Figure 17. Increasing Output Voltage by Cascading Devices](image)
9.2.1.2.4 Regulating $V_{OUT}$

It is possible to regulate the output of the LM2660 by use of a low dropout regulator (such as LP2951). The whole converter is depicted in Figure 20. This converter can give a regulated output from $-1.5$ V to $-5.5$ V by choosing the proper resistor ratio:

$$V_{out} = V_{ref} \left( 1 + \frac{R_1}{R_2} \right)$$

where

- $V_{ref} = 1.235$ V

The error flag on pin 5 of the LP2951 goes low when the regulated output at pin 4 drops by about 5%. The LP2951 can be shutdown by taking pin 3 high.
Also, as shown in Figure 21 by operating LM2660 in voltage doubling mode and adding a linear regulator (such as LP2981) at the output, we can get +5 V output from an input as low as +3 V.

![Figure 21. Generating +5 V from +3 V Input Voltage](image)

**9.2.1.3 Application Curves**

![Figure 22. Efficiency vs Load Current](image) ![Figure 23. Efficiency vs Oscillator Frequency](image)

**9.2.2 Positive Voltage Doubler**

![Figure 24. LM2660 Voltage Doubler](image)

**9.2.2.1 Design Requirements**

The LM2660 can operate as a positive voltage doubler (as shown in the Figure 24). The doubling function is achieved by reversing some of the connections to the device. The input voltage is applied to the GND pin with an allowable voltage from 2.5 V to 5.5 V. The V+ pin is used as the output. The LV pin and OUT pin must be connected to ground. The OSC pin can not be driven by an external clock in this operation mode. The unloaded output voltage is twice of the input voltage and is not reduced by the diode D1’s forward drop.
9.2.2.2 **Detailed Design Procedure**

The Schottky diode D₁ is only needed for start-up. The internal oscillator circuit uses the V+ pin and the LV pin (connected to ground in the voltage doubler circuit) as its power rails. Voltage across V+ and LV must be larger than 1.5 V to insure the operation of the oscillator. During start-up, D₁ is used to charge up the voltage at V+ pin to start the oscillator; also, it protects the device from turning-on its own parasitic diode and potentially latching-up. Therefore, the Schottky diode D₁ should have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning-on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than 10V/ms, a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.

9.2.2.3 **Application Curves**

See [Application Curves](#) in the [Voltage Inverter](#) section.

10 **Power Supply Recommendations**

The LM2660 is designed to operate from as an inverter over an input voltage supply range between 1.5 V and 5.5 V when the LV pin is grounded. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LM2660 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.
11 Layout

11.1 Layout Guidelines

The high switching frequency and large switching currents of the LM2660 make the choice of layout important. The following steps should be used as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range:

- Place \( C_{\text{IN}} \) on the top layer (same layer as the LM2660) and as close to the device as possible. Connecting the input capacitor through short, wide traces to both the \( V^+ \) and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the \( V^+ \) line.

- Place \( C_{\text{OUT}} \) on the top layer (same layer as the LM2660) and as close as possible to the OUT and GND pin. The returns for both \( C_{\text{IN}} \) and \( C_{\text{OUT}} \) should come together at one point, as close to the GND pin as possible. Connecting \( C_{\text{OUT}} \) through short, wide traces reduce the series inductance on the \( V_{\text{OUT}} \) and GND pins that can corrupt the \( V_{\text{OUT}} \) and GND lines and cause excessive noise in the device and surrounding circuitry.

- Place \( C_1 \) on the top layer (same layer as the LM2660) and as close to the device as possible. Connect the flying capacitor through short, wide traces to both the CAP+ and CAP– pins.

11.2 Layout Example

Figure 25. LM2660 Layout Example
12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI's publication of information regarding third-party products or services does not constitute an endorsement regarding the suitability of such products or services or a warranty, representation or endorsement of such products or services, either alone or in combination with any TI product or service.

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — Ti Glossary.

This glossary lists and explains terms, acronyms, and definitions.
13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2660-MWC</td>
<td>ACTIVE</td>
<td>WAFERSALE</td>
<td>YS</td>
<td>0</td>
<td>1</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>Call TI</td>
<td>Level-1-NA-UNLIM</td>
<td>-40 to 85</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LM2660M</td>
<td>NRND</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>95</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 85</td>
<td>LM26 60M</td>
<td></td>
</tr>
<tr>
<td>LM2660M/NOPB</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>95</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LM26 60M</td>
<td></td>
</tr>
<tr>
<td>LM2660MM/NOPB</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>S01A</td>
<td></td>
</tr>
<tr>
<td>LM2660MX/NOPB</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>LM26 60M</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI’s terms “Lead-Free” or “Pb-Free” mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines “Green” to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2660MM/NOPB</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>1000</td>
<td>178.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>LM2660MX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.5</td>
<td>5.4</td>
<td>2.0</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.

- **P1**: Pitch between successive cavity centers.
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2660MM/NOPB</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>1000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>LM2660MX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.

4. This dimension does not include interlead flash.

5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
DGK (S--PDSO--G8)  PLASTIC SMALL--OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-167 variation AA, except interlead flash.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated