1 Features
- Doubles Input Supply Voltage
- SOT-23 6-Pin Package
- 20-Ω Typical Output Impedance
- 90% Typical Conversion Efficiency at 20 mA
- 0.1-µA Typical Shutdown Current

2 Applications
- Cellular Phones
- Pagers
- PDAs
- Operational Amplifier Power Supplies
- Interface Power Supplies
- Handheld Instruments

3 Description
The LM2765 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of 1.8 V to 5.5 V. Two low-cost capacitors and a diode are used in this circuit to provide up to 20 mA of output current.

The LM2765 operates at 50-kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 130 µA (operating efficiency greater than 90% with most loads) and 0.1-µA typical shutdown current, the LM2765 provides ideal performance for battery powered systems. The device is manufactured in a 6-pin SOT-23 package.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2765</td>
<td>SOT-23 (6)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2013) to Revision D

Page

• Added Pin Configuration and Functions section, ESD Rating table, Feature Description, Device Functional Modes, Application and Implementation, Power Supply Recommendations, Layout, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information sections; change pin name "VOUT" to "OUT" .................................................. 1
• Added top nav icon for TI design .......................... 1
• Changed $R_{\theta JA}$ value from 210°C/W to 185.2°C/W; add additional thermal values ........................................... 4

Changes from Revision B (May 2013) to Revision C

Page

• Changed layout of National Semiconductor data sheet to TI format .......................................................... 12
## 5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>NO.</th>
<th>NAME</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V+</td>
<td>Power</td>
<td>Power supply positive voltage input</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground</td>
<td>Power supply ground input</td>
</tr>
<tr>
<td>3</td>
<td>CAP−</td>
<td>Power</td>
<td>Connect this pin to the negative terminal of the charge-pump capacitor.</td>
</tr>
<tr>
<td>4</td>
<td>SD</td>
<td>Input</td>
<td>Shutdown control pin; tie this pin to ground in normal operation.</td>
</tr>
<tr>
<td>5</td>
<td>OUT</td>
<td>Power</td>
<td>Positive voltage output</td>
</tr>
<tr>
<td>6</td>
<td>CAP+</td>
<td>Power</td>
<td>Connect this pin to the positive terminal of the charge-pump capacitor.</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)\(^{(2)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V+ to GND or V+ to OUT)</td>
<td>5.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>SD</td>
<td>(GND − 0.3 V)</td>
<td>(V+ + 0.3 V)</td>
<td></td>
</tr>
<tr>
<td>OUT continuous output current</td>
<td>40</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Output short-circuit duration to GND(^{(3)})</td>
<td>1</td>
<td>sec</td>
<td></td>
</tr>
<tr>
<td>Continuous power dissipation ((T_A = 25°C))(^{(4)})</td>
<td>600</td>
<td>mW</td>
<td></td>
</tr>
<tr>
<td>(T_{J\text{-MAX}}) (^{(4)})</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

\(^{(3)}\) OUT may be shorted to GND for one second without damage. However, shorting OUT to V+ may damage the device and must be avoided. Also, for temperatures above 85°C, OUT must not be shorted to GND or V+, or device may be damaged.

\(^{(4)}\) The maximum allowable power dissipation is calculated by using \(P_{D\text{-MAX}} = (T_{J\text{-MAX}} - T_A)/R_{ jeśliA}\), where \(T_{J\text{-MAX}}\) is the maximum junction temperature, \(T_A\) is the ambient temperature, and \(R_{ jeśliA}\) is the junction-to-ambient thermal resistance of the specified package.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)}) Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Machine model</td>
<td>200</td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient temperature</td>
<td>−40</td>
<td>85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Junction temperature</td>
<td>−40</td>
<td>100</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>LM2765</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{ JeśliA}) Junction-to-ambient thermal resistance</td>
<td>185.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{ JeśliC(top)}) Junction-to-case (top) thermal resistance</td>
<td>131.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{ JeśliB}) Junction-to-board thermal resistance</td>
<td>34.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>(ψ_{JT}) Junction-to-top characterization parameter</td>
<td>21.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>(ψ_{JB}) Junction-to-board characterization parameter</td>
<td>34.1</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Submit Documentation Feedback
Product Folder Links: LM2765
6.5 Electrical Characteristics

MIN and MAX limits apply over the full operating temperature range. Unless otherwise specified: $T_J = 25^\circ C$, $V_+ = 5 \, V$, $C_1 = C_2 = 3.3 \, \mu F$.$(1)$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_+$ Supply voltage</td>
<td></td>
<td>1.8</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_Q$ Supply current</td>
<td>No load</td>
<td></td>
<td>130</td>
<td>450</td>
<td>\mu A</td>
</tr>
<tr>
<td>$I_{SD}$ Shutdown supply current</td>
<td>$T_A = 85^\circ C$</td>
<td>0.1</td>
<td>0.5</td>
<td></td>
<td>\mu A</td>
</tr>
<tr>
<td>$V_{SD}$ Shutdown pin input voltage</td>
<td>Shutdown mode</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Normal operation</td>
<td></td>
<td>0.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_L$ Output current</td>
<td>$2.5 , V \leq V_{IN} \leq 5.5 , V$</td>
<td>20</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$1.8 , V \leq V_{IN} \leq 2.5 , V$</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{OUT}$ Output resistance$(2)$</td>
<td>$I_L = 20 , mA$</td>
<td>20</td>
<td>40</td>
<td></td>
<td>\Omega</td>
</tr>
<tr>
<td>$f_{OSC}$ Oscillator frequency</td>
<td>See$(3)$</td>
<td>40</td>
<td>100</td>
<td>200</td>
<td>kHz</td>
</tr>
<tr>
<td>$f_{SW}$ Switching frequency</td>
<td>See$(3)$</td>
<td>20</td>
<td>50</td>
<td>100</td>
<td>kHz</td>
</tr>
<tr>
<td>$P_{EFF}$ Power efficiency</td>
<td>$R_L , (1 , k\Omega)$ between GND and OUT</td>
<td>92%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OEFF}$ Voltage conversion efficiency</td>
<td>No load</td>
<td>99.96%</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) In the test circuit, capacitors $C_1$ and $C_2$ are 3.3-\mu F, 0.3-\Omega maximum ESR capacitors. Capacitors with higher ESR increase output resistance, reduce output voltage, and efficiency.

(2) Specified output resistance includes internal switch resistance and capacitor ESR. See the details in Application and Implementation for simple negative voltage converter.

(3) The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2f_{SW}$.

6.6 Typical Characteristics

(Circuit of Test Circuit, $V_{IN} = 5 \, V$, $T_A = 25^\circ C$ unless otherwise specified)
Typical Characteristics (continued)

(Circuit of Test Circuit, \(V_{IN} = 5V\), \(T_A = 25°C\) unless otherwise specified)

**Figure 3. Output Resistance vs Supply Voltage**

**Figure 4. Output Resistance vs Temperature**

**Figure 5. Output Voltage vs Load Current**

**Figure 6. Switching Frequency vs Supply Voltage**

**Figure 7. Switching Frequency vs Temperature**

**Figure 8. Output Ripple vs Load Current**
7 Parameter Measurement Information

7.1 Test Circuit

* $C_{IN}$, $C_1$, and $C_2$ are 3.3 $\mu$F OS-CON capacitors.

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8 Detailed Description

8.1 Overview
The LM2765 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of 1.8 V to 5.5 V. Two low-cost capacitors and a diode (needed during start-up) are used in this circuit to provide up to 20 mA of output current.

8.2 Functional Block Diagram

8.3 Feature Description

8.3.1 Circuit Description
The LM2765 contains four large CMOS switches which are switched in a sequence to double the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 9 shows the voltage conversion scheme. When S<sub>2</sub> and S<sub>4</sub> are closed, C<sub>1</sub> charges to the supply voltage V+. During this time interval, switches S<sub>1</sub> and S<sub>3</sub> are open. In the next time interval, S<sub>2</sub> and S<sub>4</sub> are open; at the same time, S<sub>1</sub> and S<sub>3</sub> are closed, the sum of the input voltage V+ and the voltage across C<sub>1</sub> gives the 2 V+ output voltage when there is no load. The output voltage drop when a load is added is determined by the parasitic resistance (R<sub>ds(on)</sub> of the MOSFET switches and the ESR of the capacitors) and the charge transfer loss between capacitors. See Application and Implementation for more details.

8.4 Device Functional Modes

8.4.1 Shutdown Mode
A shutdown (SD) pin is available to disable the device and reduce the quiescent current to 1 µA. In normal operating mode, the SD pin is connected to ground. The device can be brought into the shutdown mode by applying to the SD pin a voltage greater than 40% of the V+ pin voltage.

Figure 9. Voltage Doubling Principle
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM2765 provides a simple and efficient means of creating an output voltage level equal to twice that of the input voltage. Without the need of an inductor, the application solution size can be reduced versus the magnetic DC-DC converter solution.

9.2 Typical Applications

9.2.1 Voltage Doubler

The main application of the LM2765 is to double the input voltage. The range of the input supply voltage is 1.8 V to 5.5 V.

![Figure 10. Voltage Doubler](image)

9.2.1.1 Design Requirements

Example requirements for LM2765 device applications:

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>1.8 V to 5.5 V</td>
</tr>
<tr>
<td>Output current</td>
<td>0 mA to 20 mA</td>
</tr>
<tr>
<td>Boost switching frequency</td>
<td>20 kHz</td>
</tr>
</tbody>
</table>
9.2.1.2 Detailed Design Requirements

9.2.1.2.1 Positive Voltage Doubler

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals 2 V+. The output resistance $R_{OUT}$ is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, the capacitance and equivalent series resistance (ESR) of $C_1$ and $C_2$. Since the switching current charging and discharging $C_1$ is approximately twice as the output current, the effect of the ESR of the pumping capacitor $C_1$ will be multiplied by four in the output resistance. The output capacitor $C_2$ is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts when in the output resistance. A good approximation of $R_{OUT}$ is:

$$R_{OUT} \approx 2R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4ESR_{C1} + ESR_{C2}$$

where

- $R_{SW}$ is the sum of the ON resistance of the internal MOSFET switches shown in Figure 9. $R_{SW}$ is typically 8 Ω for the LM2765. (1)

The peak-to-peak output voltage ripple is determined by the oscillator frequency, the capacitance and ESR of the output capacitor $C_2$:

$$V_{RIPPLE} = \frac{I_L}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C2}$$

High capacitance, low-ESR capacitors can reduce both the output resistance and the voltage ripple.

The Schottky diode $D_1$ is only needed for start-up. The internal oscillator circuit uses the OUT pin and the GND pin. Voltage across OUT and GND must be larger than 1.8 V to insure the operation of the oscillator. During start-up, $D_1$ is used to charge up the voltage at the OUT pin to start the oscillator; also, it protects the device from turning-on its own parasitic diode and potentially latching-up. Therefore, the Schottky diode $D_1$ must have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning-on. A Schottky diode such as 1N5817 can be used for most applications. If the input voltage ramp is less than 10 V/ms, a smaller Schottky diode such as MBR0520LT1 can be used to reduce the circuit size.

9.2.1.2.2 Capacitor Selection

As discussed in Positive Voltage Doubler, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{I_L^2R_L}{I_L^2R_L + I_L^2R_{OUT} + I_Q(V+)}$$

where

- $I_Q(V+)$ is the quiescent power loss of the device; and
- $I_L^2R_{OUT}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs. (3)

The selection of capacitors is based on the specifications of the dropout voltage (which equals $I_{OUT}R_{OUT}$), the output voltage ripple, and the converter efficiency. Low ESR capacitors are recommended to maximize efficiency, reduce the output voltage drop and voltage ripple.

9.2.1.2.3 Paralleling Devices

Any number of LM2765 devices can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor $C_1$, while only one output capacitor, $C_{OUT}$, is required as shown in Figure 11. The composite output resistance is:

$$R_{OUT} = R_{OUT} \text{ of each LM2765} / \text{number of devices}$$

(4)
9.2.1.2.4 Cascading Devices

Cascading the LM2765 devices is an easy way to produce a greater voltage (a two-stage cascade circuit is shown in Figure 12).

The effective output resistance is equal to the weighted sum of each individual device, shown in Equation 5:

$$R_{OUT} = 1.5 \times R_{OUT_1} + R_{OUT_2}$$  \hspace{1cm} (5)

Note that the increasing of the number of cascading stages is practically limited since it significantly reduces the efficiency, increases the output resistance and output voltage ripple.

9.2.1.2.5 Regulating $V_{OUT}$

It is possible to regulate the output of the LM2765 by use of a low dropout regulator (such as LP2980-5.0). The whole converter is depicted in Figure 13.

A different output voltage is possible by use of LP2980-3.3, LP2980-3.0, or LP2980-ADJ.

Note that the following conditions must be satisfied simultaneously for worst-case design:

$$2V_{in_{min}} > V_{out_{min}} + V_{drop_{max}} (LP2980) + I_{out_{max}} \times R_{out_{max}} (LM2765)$$  \hspace{1cm} (6)

$$2V_{in_{max}} < V_{out_{max}} + V_{drop_{min}} (LP2980) + I_{out_{min}} \times R_{out_{min}} (LM2765)$$  \hspace{1cm} (7)
9.2.1.3 Application Curve

![Application Curve Graph]

Figure 14. Efficiency vs Load Current

10 Power Supply Recommendations

The LM2765 is designed to operate from as an inverter over an input voltage supply range between 1.8 V and 5.5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.
11 Layout

11.1 Layout Guidelines

The high switching frequency and large switching currents of the LM2765 make the choice of layout important. Use the following steps as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range.

- Place $C_{IN}$ on the top layer (same layer as the LM2765) and as close as possible to the device. Connecting the input capacitor through short, wide traces to both the $V+$ and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the $V+$ line.

- Place $C_{OUT}$ on the top layer (same layer as the LM2765) and as close as possible to the OUT and GND pin. The returns for both $C_{IN}$ and $C_{OUT}$ must come together at one point, as close as possible to the GND pin. Connecting $C_{OUT}$ through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the $V_{OUT}$ and GND lines and cause excessive noise in the device and surrounding circuitry.

- Place C1 on the top layer (same layer as the LM2765 device) and as close as possible to the device. Connect the flying capacitor through short, wide traces to both the CAP+ and CAP– pins.

11.2 Layout Example

Figure 15. Typical Layout for LM2765
12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer
TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2765M6X/NOPB</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>S15B</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2765M6X/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.

A0 - Dimension designed to accommodate the component width
B0 - Dimension designed to accommodate the component length
K0 - Dimension designed to accommodate the component thickness
W - Overall width of the carrier tape
P1 - Pitch between successive cavity centers
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2765M6X/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.