1 Features
- Doubles Input Supply Voltage
- SOT-23 5-Pin Package
- 20-Ω Typical Output Impedance
- 96% Typical Conversion Efficiency at 15 mA

2 Applications
- Cellular Phones
- Pagers
- PDAs, Organizers
- Operational Amplifier Power Suppliers
- Interface Power Suppliers
- Handheld Instruments

3 Description
The LM2767 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of 1.8 V to 5.5 V. Two low-cost capacitors and a diode are used in this circuit to provide at least 15 mA of output current.

The LM2767 operates at 11-kHz switching frequency to avoid audio voice-band interference. With an operating current of only 40 µA (operating efficiency greater than 90% with most loads), the LM2767 provides ideal performance for battery-powered systems. The device is manufactured in a 5-pin SOT-23 package.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2767</td>
<td>SOT-23 (5)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
Table of Contents

1 Features ................................................................. 1
2 Applications ............................................................ 1
3 Description ............................................................. 1
4 Revision History ........................................................ 2
5 Pin Configuration and Functions ...................................... 3
6 Specifications .......................................................... 4
   6.1 Absolute Maximum Ratings ........................................ 4
   6.2 ESD Ratings ........................................................... 4
   6.3 Recommended Operating Conditions ......................... 4
   6.4 Thermal Information ............................................... 4
   6.5 Electrical Characteristics ........................................ 5
   6.6 Typical Characteristics .......................................... 6
7 Parameter Measurement Information ................................. 7
   7.1 Test Circuit .......................................................... 7
8 Detailed Description .................................................. 8
   8.1 Overview ............................................................ 8
   8.2 Functional Block Diagram ....................................... 8
8.3 Feature Description ................................................. 8
8.4 Device Functional Modes .......................................... 8
9 Application and Implementation ..................................... 9
   9.1 Application Information ......................................... 9
   9.2 Typical Application .............................................. 9
10 Power Supply Recommendations ................................... 13
11 Layout ................................................................. 13
   11.1 Layout Guidelines .............................................. 13
   11.2 Layout Example ................................................ 13
12 Device and Documentation Support ................................. 14
   12.1 Device Support .................................................. 14
   12.2 Community Resources ......................................... 14
   12.3 Trademarks ...................................................... 14
   12.4 Electrostatic Discharge Caution ............................. 14
   12.5 Glossary ........................................................ 14
13 Mechanical, Packaging, and Orderable Information ............. 14

4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2013) to Revision D Page

• Added Device Information and Pin Configuration and Functions sections, ESD Rating table, Feature Description, Device Functional Modes, Application and Implementation, Power Supply Recommendations, Layout, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information sections ................................................. 1

Changes from Revision B (May 2013) to Revision C Page

• Changed layout of National Data Sheet to TI format .......................................................... 12
5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VOUT</td>
<td>Power</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>CAP-</td>
<td>Power</td>
</tr>
<tr>
<td>4</td>
<td>V+</td>
<td>Power</td>
</tr>
<tr>
<td>5</td>
<td>CAP+</td>
<td>Power</td>
</tr>
</tbody>
</table>

Pin Functions
6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)(\(^{(2)}\))

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V+ to GND, or V+ to (V_{OUT}))</td>
<td>5.8</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OUT}) continuous output current</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>Output short-circuit duration to GND(^{(3)})</td>
<td>1</td>
<td>sec</td>
</tr>
<tr>
<td>Continuous power dissipation ((T_A = 25°C))(^{(4)})</td>
<td>400</td>
<td>mW</td>
</tr>
<tr>
<td>(T_{J\text{Max}})(^{(4)})</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>−65 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions**. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/ Distributors for availability and specifications.

(3) \(V_{OUT}\) may be shorted to GND for one second without damage. For temperatures above 85°C, \(V_{OUT}\) must not be shorted to GND or device may be damaged.

(4) The maximum allowable power dissipation is calculated by using \(P_{DMAX} = (T_{J\text{Max}} - T_A)/R_{\theta JA}\), where \(T_{J\text{Max}}\) is the maximum junction temperature, \(T_A\) is the ambient temperature, and \(R_{\theta JA}\) is the junction-to-ambient thermal resistance of the specified package.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±2000</td>
</tr>
<tr>
<td>Machine model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±200</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction temperature</td>
<td>−40</td>
<td>100</td>
<td>°C</td>
</tr>
<tr>
<td>Ambient temperature</td>
<td>−40</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>Lead temperature (soldering, 10 sec.)</td>
<td>240</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>LM2767</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{\theta JA}) Junction-to-ambient thermal resistance</td>
<td>210</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the **Semiconductor and IC Package Thermal Metrics** application report, SPRA953.
6.5 Electrical Characteristics

Unless otherwise specified, typical limits are for $T_J = 25^\circ$C, minimum and maximum limits apply over the full operating temperature range: $V_+ = 5$ V, $C_1 = C_2 = 10 \mu$F.\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_+$ Supply voltage</td>
<td></td>
<td>1.8</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_Q$ Supply current</td>
<td>No load</td>
<td>40</td>
<td></td>
<td>90</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_L$ Output current</td>
<td>$1.8 \text{ V} \leq V_+ \leq 5.5 \text{ V}$</td>
<td>15</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$R_{OUT}$ Output resistance(^{(2)})</td>
<td>$I_L = 15 \text{ mA}$</td>
<td>20</td>
<td></td>
<td>40</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$f_{OSC}$ Oscillator frequency</td>
<td>See(^{(3)})</td>
<td>8</td>
<td></td>
<td>22</td>
<td>kHz</td>
</tr>
<tr>
<td>$f_{SW}$ Switching frequency</td>
<td>See(^{(3)})</td>
<td>4</td>
<td></td>
<td>11</td>
<td>kHz</td>
</tr>
<tr>
<td>$P_{EFF}$ Power efficiency</td>
<td>$R_L (5 \text{ k}\Omega) \text{ between } \text{GND and OUT}$</td>
<td>98%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OEFF}$ Voltage conversion efficiency</td>
<td>$I_L = 15 \text{ mA to GND}$</td>
<td></td>
<td></td>
<td>96%</td>
<td></td>
</tr>
</tbody>
</table>

(1) In the test circuit, capacitors $C_1$ and $C_2$ are $10-\mu$F, 0.3-$\Omega$ maximum ESR capacitors. Capacitors with higher ESR may increase output resistance, and reduce output voltage and efficiency.

(2) Specified output resistance includes internal switch resistance and capacitor ESR. See the details in Application and Implementation for positive voltage doubler.

(3) The output switches operate at one half of the oscillator frequency, $f_{OSC} = 2 \times f_{SW}$.
### 6.6 Typical Characteristics

(Circuit of Figure 9, $V_{IN} = 5$ V, $T_A = 25\degree C$ unless otherwise specified).

<table>
<thead>
<tr>
<th>Figure 1. Supply Current vs Supply Voltage</th>
<th>Figure 2. Output Resistance vs Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Supply Current vs Supply Voltage" /></td>
<td><img src="image2" alt="Output Resistance vs Capacitance" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Figure 3. Output Resistance vs Supply Voltage</th>
<th>Figure 4. Output Resistance vs Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image3" alt="Output Resistance vs Supply Voltage" /></td>
<td><img src="image4" alt="Output Resistance vs Temperature" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Figure 5. Output Voltage vs Load Current</th>
<th>Figure 6. Switching Frequency vs Supply Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image5" alt="Output Voltage vs Load Current" /></td>
<td><img src="image6" alt="Switching Frequency vs Supply Voltage" /></td>
</tr>
</tbody>
</table>
Typical Characteristics (continued)

(Circuit of Figure 9, \( V_{IN} = 5 \) V, \( T_A = 25^\circ\)C unless otherwise specified).

![Switching Frequency vs Temperature](image1)

![Output Ripple vs Load Current](image2)

Figure 7. Switching Frequency vs Temperature

Figure 8. Output Ripple vs Load Current

7 Parameter Measurement Information

7.1 Test Circuit

![LM2767 Test Circuit](image3)

\( * \) \( C_{IN}, C_1, \) and \( C_2 \) are 10 \( \mu \)F OS-CON capacitors.

Figure 9. LM2767 Test Circuit
8 Detailed Description

8.1 Overview
The LM2767 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of 1.8 V to 5.5 V. Two low-cost capacitors and a diode (needed during start-up) are used in this circuit.

8.2 Functional Block Diagram

8.3 Feature Description
The LM2767 contains four large CMOS switches which are switched in a sequence to double the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 11 illustrates the voltage conversion scheme. When S₂ and S₄ are closed, C₁ charges to the supply voltage V+. During this time interval, switches S₁ and S₃ are open. In the next time interval, S₂ and S₄ are open; at the same time, S₁ and S₃ are closed, the sum of the input voltage V+ and the voltage across C₁ gives the 2V+ output voltage when there is no load. The output voltage drop when a load is added is determined by the parasitic resistance (R_{ds(on)} of the MOSFET switches and the ESR of the capacitors) and the charge transfer loss between capacitors. Details are discussed in Application and Implementation.

8.4 Device Functional Modes
The LM2767 is always enabled when power is applied to the V+ pin (1.8 V ≤ V_{IN} ≤ 5.5 V). To disable the part, power must be removed.
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The LM2767 provides a simple and efficient means of creating an output voltage level equal to twice that of the input voltage. Without the need of an inductor, the application solution size can be reduced versus the magnetic DC-DC converter solution.

9.2 Typical Application
The main application of the LM2767 is to double the input voltage. The range of the input supply voltage is 1.8 V to 5.5 V.

Figure 10. LM2767 Typical Application

9.2.1 Design Requirements
For typical switched-capacitor voltage converter applications, use the parameters listed in Table 1.

Table 1. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum input voltage</td>
<td>1.8 to 5.5 V</td>
</tr>
<tr>
<td>Output current (minimum)</td>
<td>15 mA</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>11 kHz (typical)</td>
</tr>
</tbody>
</table>

9.2.2 Detailed Design Procedure

9.2.2.1 Positive Voltage Doubler

Figure 11. Voltage Doubling Principle
The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals 2 V+ . The output resistance $R_{\text{out}}$ is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, and the capacitance and ESR of $C_1$ and $C_2$. Because the switching current charging and discharging $C_1$ is approximately twice the output current, the effect of the ESR of the pumping capacitor $C_1$ is multiplied by four in the output resistance. The output capacitor $C_2$ is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. A good approximation of $R_{\text{out}}$ is:

$$R_{\text{OUT}} \approx 2R_{\text{SW}} + \frac{2}{f_{\text{OSC}}} \times \frac{I_L}{C_1} + 4E_{\text{SRC1}} + E_{\text{SRC2}}$$

where

- $R_{\text{SW}}$ is the sum of the ON resistance of the internal MOSFET switches shown in Figure 11.

The peak-to-peak output voltage ripple is determined by the oscillator frequency as well as the capacitance and ESR of the output capacitor $C_2$:

$$V_{\text{RIPPLE}} = \frac{I_L}{f_{\text{OSC}}} \times C_2 + 2 \times I_L \times E_{\text{SRC2}}$$

High capacitance, low ESR capacitors can reduce both the output resistance and the voltage ripple.

The Schottky diode $D_1$ is only needed to protect the device from turning on its own parasitic diode and potentially latching up. During start-up, $D_1$ also quickly charges up the output capacitor to $V_{\text{IN}}$ minus the diode drop thereby decreasing the start-up time. Therefore, the Schottky diode $D_1$ must have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than 10 V/ms, a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.

### 9.2.2.2 Capacitor Selection

As discussed in Positive Voltage Doubler, the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$\eta = \frac{P_{\text{OUT}}}{P_{\text{IN}}} = \frac{l_i^2 R_L}{l_i^2 R_L + l_i^2 R_{\text{OUT}} + I_Q(V+)}$$

where

- $I_Q(V+)$ is the quiescent power loss of the device; and
- $l_i^2 R_{\text{out}}$ is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

The selection of capacitors is based on the allowable voltage drop (which equals $I_{\text{out}} R_{\text{out}}$), and the desired output voltage ripple. Low-ESR capacitors (Table 2) are recommended to maximize efficiency, reduce the output voltage drop and voltage ripple.

<table>
<thead>
<tr>
<th>MANUFACTURER</th>
<th>PHONE</th>
<th>WEBSITE</th>
<th>CAPACITOR TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nichicon Corp.</td>
<td>(847)-843-7500</td>
<td><a href="http://www.nichicon.com">www.nichicon.com</a></td>
<td>PL &amp; PF series, through-hole aluminum electrolytic</td>
</tr>
<tr>
<td>AVX Corp.</td>
<td>(843)-448-9411</td>
<td><a href="http://www.avxcorp.com">www.avxcorp.com</a></td>
<td>TPS series, surface-mount tantalum</td>
</tr>
<tr>
<td>Sprague</td>
<td>(207)-324-4140</td>
<td><a href="http://www.vishay.com">www.vishay.com</a></td>
<td>593D, 594D, 595D series, surface-mount tantalum</td>
</tr>
<tr>
<td>Sanyo</td>
<td>(619)-661-6835</td>
<td><a href="http://www.sanyovideo.com">www.sanyovideo.com</a></td>
<td>OS-CON series, through-hole aluminum electrolytic</td>
</tr>
<tr>
<td>Murata</td>
<td>(800)-831-9172</td>
<td><a href="http://www.murata.com">www.murata.com</a></td>
<td>Ceramic chip capacitors</td>
</tr>
<tr>
<td>Taiyo Yuden</td>
<td>(800)-348-2496</td>
<td><a href="http://www.t-yuden.com">www.t-yuden.com</a></td>
<td>Ceramic chip capacitors</td>
</tr>
<tr>
<td>Tokin</td>
<td>(408)-432-8020</td>
<td><a href="http://www.tokin.com">www.tokin.com</a></td>
<td>Ceramic chip capacitors</td>
</tr>
</tbody>
</table>
9.2.2.3 Paralleling Devices

Any number of LM2767 devices can be paralleled to reduce the output resistance. Because there is no closed loop feedback, as found in regulated circuits, stable operation is assured. Each device must have its own pumping capacitor \( C_1 \), while only one output capacitor \( C_{OUT} \) is needed as shown in Figure 12. The composite output resistance is:

\[
R_{OUT} = \frac{R_{OUT\_1}}{\text{Number of Devices}}
\]

\[(4)\]

![Figure 12. Lowering Output Resistance by Paralleling Devices](image)

9.2.2.4 Cascading Devices

Cascading the several LM2767 devices is an easy way to produce a greater voltage (a two-stage cascade circuit is shown in Figure 13).

The effective output resistance is equal to the weighted sum of each individual device:

\[
R_{OUT} = 1.5 R_{OUT\_1} + R_{OUT\_2}
\]

\[(5)\]

Note that increasing the number of cascading stages is practically limited because it significantly reduces the efficiency, increases the output resistance and output voltage ripple.

![Figure 13. Increasing Output Voltage By Cascading Devices](image)

9.2.2.5 Regulating \( V_{OUT} \)

It is possible to regulate the output of the LM2767 by use of a low dropout regulator (such as LP2980-5.0). The whole converter is depicted in Figure 14.

A different output voltage is possible by use of LP2980-3.3, LP2980-3.0, or LP2980-ADJ.

The following conditions must be satisfied simultaneously for worst case design:

\[
2V_{IN\_MIN} > V_{OUT\_MIN} + V_{DROP\_MAX\ (LP2980)} + I_{OUT\_MAX \times R_{OUT\_MAX}}
\]

\[
2V_{IN\_MAX} < V_{OUT\_MAX} + V_{DROP\_MIN\ (LP2980)} + I_{OUT\_MIN \times R_{OUT\_MIN}}
\]

\[(6)\] \[(7)\]
9.2.3 Application Curve

Figure 14. Generate a Regulated 5-V From 3-V Input Voltage

Figure 15. Efficiency vs Load Current
10 Power Supply Recommendations

The LM2767 is designed to operate from as an inverter over an input voltage supply range from 1.8 V and 5.5 V. This input supply must be well-regulated and capable to supply the required input current. If the input supply is located far from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

Use the following steps as a reference to ensure the device is stable across its intended operating voltage and current range.

- Place CIN on the top layer (same layer as the LM2767) and as close to the device as possible. Connecting the input capacitor through short, wide traces to both the V+ and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the V+ line.
- Place COUT on the top layer (same layer as the LM2767) and as close as possible to the OUT and GND pin. The returns for both CIN and COUT must come together at one point, as close to the GND pin as possible. Connecting COUT through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the VOUT and GND lines and cause excessive noise in the device and surrounding circuitry.
- Place C1 on the top layer (same layer as the LM2767 device) and as close to the device as possible. Connect the flying capacitor through short, wide traces to both the CAP+ and CAP– pins.

11.2 Layout Example

![LM2767 Layout Example](image-url)
12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI's publication of information regarding third-party products or services does not constitute an endorsement regarding the suitability of such products or services or a warranty, representation or endorsement of such products or services, either alone or in combination with any TI product or service.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community  *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support  *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary.*
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM2767M5</td>
<td>NRND</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 85</td>
<td>S17B</td>
<td>Samples</td>
</tr>
<tr>
<td>LM2767M5/NOPB</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>S17B</td>
<td>Samples</td>
</tr>
<tr>
<td>LM2767M5X/NOPB</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>S17B</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### REEL DIMENSIONS

- **Reel Diameter**: 178.0 mm
- **Reel Width (W1)**: 8.4 mm
- **A0**: 3.2 mm
- **B0**: 3.2 mm
- **K0**: 1.4 mm
- **P1**: 4.0 mm
- **W**: 8.0 mm
- **Pin 1 Quadrant**: Q3

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Sprocket Holes**
- **User Direction of Feed**
- **Pocket Quadrants**

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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www.ti.com 20-Dec-2016
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*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7. Board assembly site may have different recommendations for stencil design.
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